SynQor

Advancing The Power Curve

Input System Instability

Application Note PQ-00-05-1 Rev. 01 - 5/16/00

Summary:

This application note details the condition of input system instability that can occur because a dc/dc converter appears incrementally as a negative resistance load. The note provides an understanding of why this instability arises, and shows the preferred solution for correcting it.

Introduction

In a distributed power architecture (DPA), a voltage source provides power over a bus to multiple dc/dc converters. At low frequencies a converter can appear, incrementally, as a negative resistance load, which can interact with the reactance of the bus (including any filter elements that have been added to the input of the converter), causing an unstable condition. The converter will then operate improperly, and may damage itself and its load. A power system engineer must ensure this "system instability" does not occur.

Avoiding system instability is a straightforward process. We simply need to add positive resistance in the external input filter to counteract the negative resistance of the dc/dc converter. The question is “how much positive resistance is required?”.

Background

Many published papers address the topic of system instability (*see references*). Most articles specify that to guarantee system stability the magnitude of the source impedance, Z_S, should be small compared to the magnitude of the converter's input impedance, Z_I (*Figure 1*). Because the external input filter impedance usually dominates the source impedance, this $|Z_S| << |Z_I|$ requirement becomes a constraint on the design of the filter.

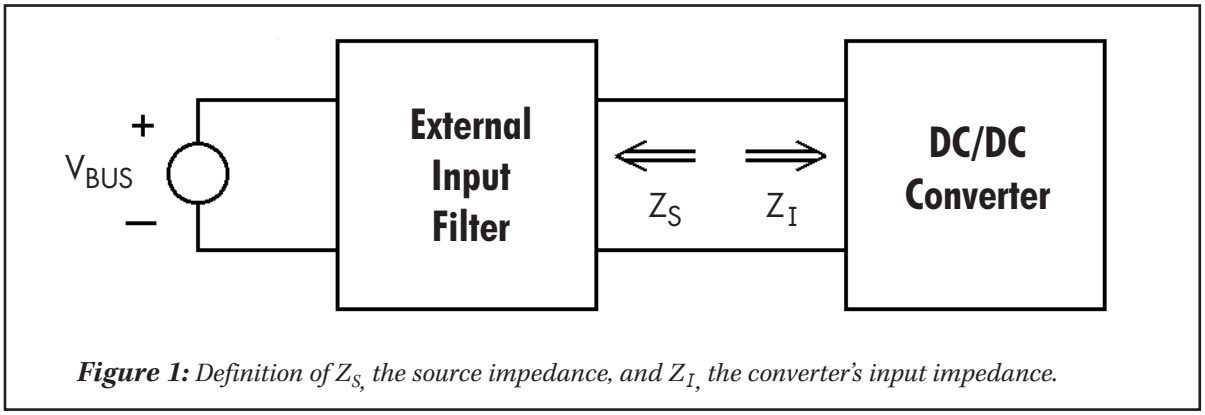

Figure 1: *Definition of Z_S, the source impedance, and Z_I, the converter's input impedance.*

Although the $|Z_S| << |Z_I|$ requirement is a relatively well known "rule of thumb" in the industry, it is not always easy to implement. One reason is that very few dc/dc converter vendors provide $|Z_I|$ in their data sheets, which forces the designer to make complicated measurements to determine the value. Also, in achieving a satisfactory level of stability it is not clear how much smaller $|Z_S|$ must be compared to $|Z_I|$.

Nevertheless, most power system engineers successfully create stable distributed power systems by placing a relatively large electrolytic capacitor across the input terminals of each dc/dc converter. The Equivalent Series Resistance of this capacitor provides the positive resistance needed to compensate for the destabilizing effects

of the converter's negative resistance.

Incremental Input Impedance, Z_I

To understand why the capacitor solution works, it is useful to review why a dc/dc converter appears incrementally as a negative resistor at its input terminals.

A dc/dc converter is designed to hold its output voltage constant no matter how its input voltage varies. Given a constant load current, the power drawn from the input bus is therefore also constant. If the input voltage increases by some factor, the input current will decrease by this same factor to keep the power level constant.

In incremental terms, a positive incremental change in the input voltage results in a negative incremental change in the input current, causing the converter to look like a negative resistor at its input terminals. The value of this negative resistance depends on the operating point of the converter according to:

$$R_N = - \left(\frac{V_{IN}}{I_{IN}} \right) \qquad (1)$$

Where:

R_N = Negative resistance
V_{IN} = Voltage input to the dc/dc converter
I_{IN} = Input current to the dc/dc converter

Note that at full load and at the lowest input voltage the magnitude of R_N is the smallest (we will use this fact later). For example, a $3.3V_{OUT}$, 30A half-brick converter that is 90% efficient (because it uses synchronous rectifiers) will draw an input current of about 3A when its input voltage is 36V. Under this condition R_N = -12Ω. At the nominal input voltage of 48V, the full-load input current is only 2.3A and R_N = -21Ω.

Also, note that the converter's input impedance, Z_I, appears as a negative resistance only at low frequencies. At higher frequencies the impedance is influenced by the converter's own internal filter elements and the limited bandwidth of its feedback loop.

Figure 2 shows $|Z_I|$ versus frequency for SynQor's $48V_{IN}$, $3.3V_{OUT}$, 30A dc/dc converter. As can be seen, at low frequencies $|Z_I|$ is resistive (actually, we need to look at the phase of Z_I, which is -180° at low frequencies, to see that it is negative). Around 1 kHz the magnitude starts to roll off with a slope of -20dB per decade. We can model this as a capacitor C in parallel with R_N. Similarly, a more complex circuit can model the resonant dynamics that show up around 20 kHz in the plot of $|R_N|$. For this discussion, however, we will just use the simple $R_N C$ model.

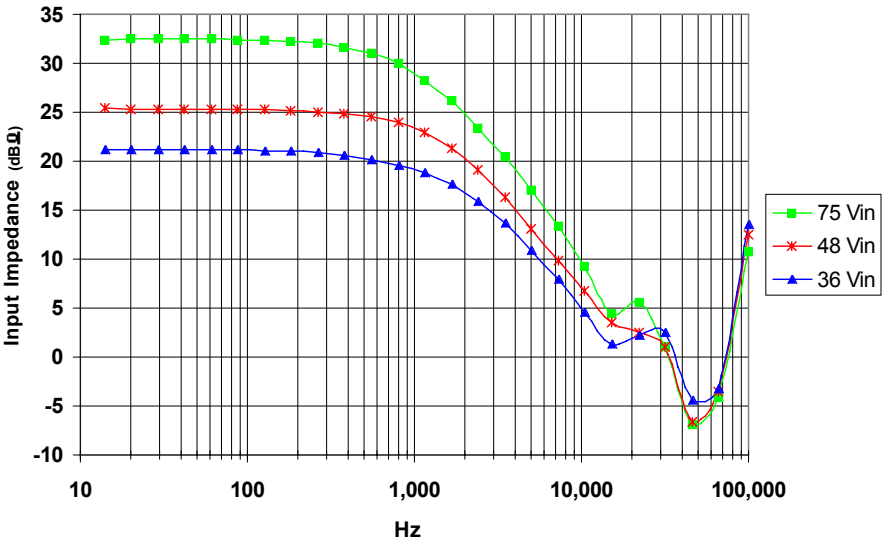

Figure 2: *Input impedance ($Z_I = V_{IN}/I_{IN}$) for minimum, nominal, and maximum input voltage at full rate power for $3.3V_{OUT}$, 30A half-brick dc/dc converter.*

Origin of the $|Z_S| << |Z_I|$ Rule

For a given dc/dc converter we can determine important frequency-dependent functions such as loop transmission, input and output impedance, and input voltage ripple rejection when the converter is connected to a true voltage source. When we connect this same converter to a source having impedance Z_S, all of these functions are multiplied by the following factor:

$$\frac{Z_I}{(Z_I + Z_S)} = \frac{1}{\left(1 + \frac{Z_S}{Z_I}\right)} \quad (2)$$

If $|Z_S| << |Z_I|$ for all frequencies, this factor is approximately unity and the effect on the converter's performance is negligible. To ensure stability, however, the poles of this factor must lie in the left-hand plane. The $|Z_S| << |Z_I|$ requirement is more than sufficient for this to be true.

Notice that the factor given above is simply the voltage divider effect of the source impedance interacting with the converter's input impedance. We can therefore determine the poles of this factor by looking at the poles of the circuit formed by the source impedance and the input impedance. We will use this analysis method below.

One Approach to System Stability

Figure 3 shows a converter with a very simple external filter composed of an inductor, L, and a series resistor, R_P. The purpose of R_P is to counteract the converter's negative input resistor R_N, which can be modeled from this point forward as $-|R_N|$. The combined filter/converter-input circuit, is a second-order equation as follows:

$$s^2LC + s\left(\frac{L}{-|R_N|} + R_P C\right) + \left(1 - \frac{R_P}{|R_N|}\right) = 0 \quad (3)$$

The poles of this equation will be in the left-hand plane if all the coefficients have the same sign, which results in the following two constraints for R_P:

$$R_P < |R_N| \quad (4)$$

$$R_P > \frac{L}{(C|R_N|)} \quad (5)$$

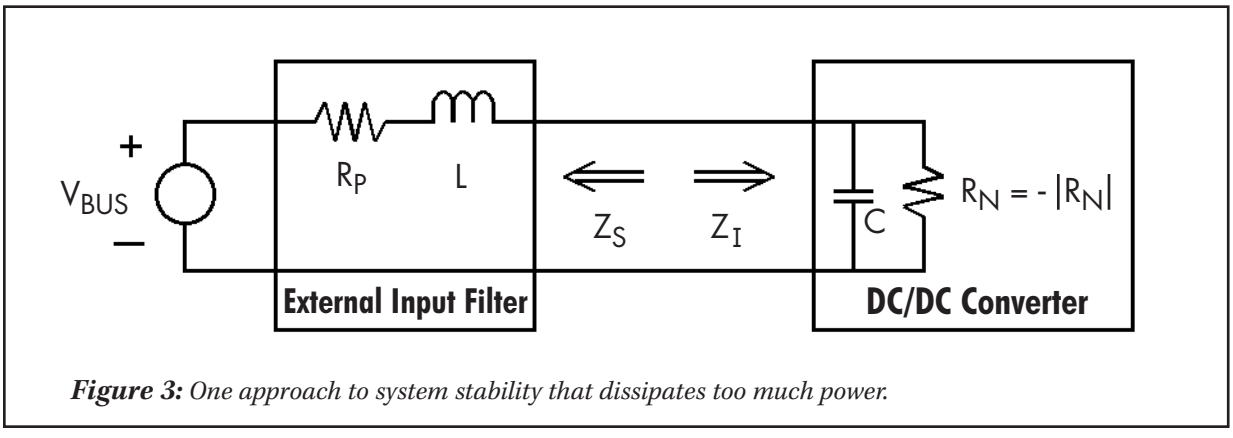

Figure 3: *One approach to system stability that dissipates too much power.*

From these we can derive the additional constraint:

$$|R_N|^2 > \frac{L}{C} \qquad (6)$$

In all three inequalities, the most constraining condition is where $|R_N|$ is smallest, when the converter is drawing full power from its lowest input voltage.

There is still a lot of flexibility for the power system engineer in these constraints. Of course, the need to reduce ripple currents on the bus, as well as the size and cost of the filter elements, place other important constraints on L and C.

However, once the values for L, C, R_P and $|R_N|$ are known, the relative stability of the system can be analyzed by plugging the numbers into Equation (3) and finding the pole locations. From this information, the system's damping ratio can be determined.

As an example, consider the $3.3V_{OUT}$, 30A converter mentioned above where the minimum value of $|R_N|$ is 12Ω. Assume L = 10μH and C = 6.6μF. With these numbers we must choose R_P < 12Ω and R_P > 0.13Ω.

To limit its dissipation, we want to make R_P as small as possible. But choosing a value of 1Ω (which will provide a damping ratio of only about 0.35), means that R_P will still dissipate 5.3W at full load when the input voltage is 48V, and 9W with a 36V input. From both efficiency and thermal viewpoints, this is too much dissipation.

This simple approach to adding positive resistance to the input filter is therefore not the preferred method. However, the above analysis technique was helpful because it gave us a more circuit-oriented way of thinking about the system stability problem.

The Normal Approach to System Stability

The alternative input filter design shown in *Figure 4* is the one most commonly used by power system engineers. In this filter C_{BIG} and R_P represent an electrolytic capacitor and its Equivalent Series Resistance (ESR). What's important here is that the electrolytic capacitor provides a positive resistance in the filter circuit that does not dissipate dc power. Resistor R_P does not carry the converter's dc input current, nor does it withstand the converter's dc input voltage.

To find out how large R_P must be to ensure a stable system, we first find the characteristic equation of the complete network shown in *Figure 4*. In this case, the equation is third-order:

$$s^3LC_{BIG}CR_P + s^2L\left[C_{BIG}\left(1 - \frac{R_P}{|R_N|}\right) + C\right] + s\left(\frac{L}{-|R_N|} + R_PC_{BIG}\right) + 1 = 0 \qquad (7)$$

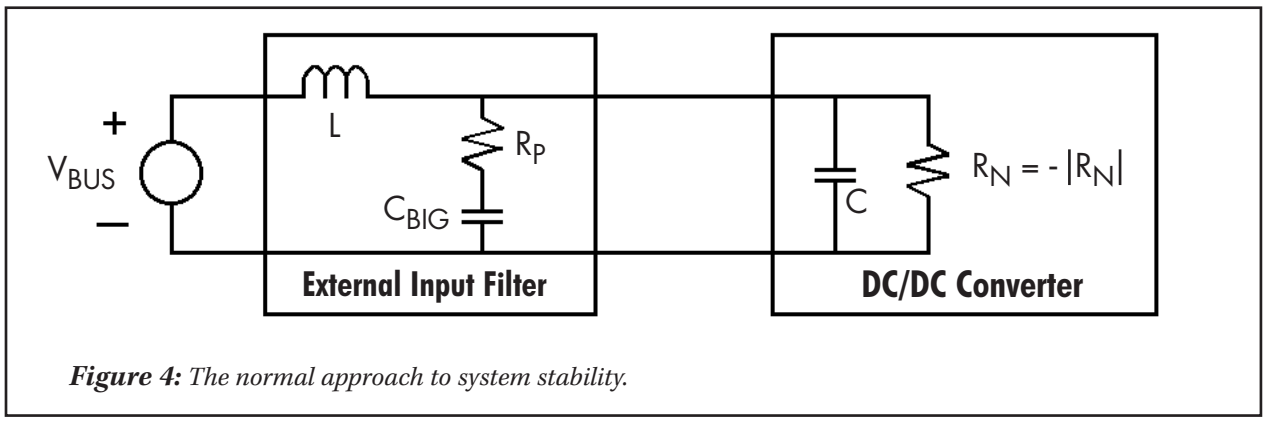

Figure 4: *The normal approach to system stability.*

A necessary, but not sufficient condition for this third-order system to be stable is that the coefficients of this equation all have the same sign, yielding the following three constraints:

$$R_P < |R_N|\left(1 + \frac{C}{C_{BIG}}\right) \tag{8}$$

$$R_P > \frac{L}{(C_{BIG}|R_N|)} \tag{9}$$

$$|R_N|^2 > \frac{L}{(C_{BIG} + C)} \tag{10}$$

Furthermore, but without going into the derivation here, these three constraints become sufficient for stability if $C_{BIG} >> C$. A factor of five between these two capacitance values is usually enough for this fourth constraint.

Continuing our example of a $3.3V_{OUT}$, 30A converter with a minimum value for $|R_N|$ of 12Ω, assume that L = 10µH, C = 6.6µF, and C_{BIG} = 33µF. The range for R_P that will give a stable system is $0.025\Omega < R_P < 14.4\Omega$.

Fortunately, the ESR of a typical electrolytic capacitor falls well within this range. For instance, one vendor's 33µF, 100V part has an ESR of 0.6Ω. With this value for R_P, the three poles of the characteristic equation given above occur at ($\varpi = -2\pi \times 39$kHz) and ($\varpi = -2\pi \times 3.7$kHz ± $j2\pi \times 8.1$kHz). The damping ratio of the two complex, lower frequency poles is $\zeta = \cos(\tan^{-1}(8.1/3.7)) = 0.42$. (Several math software packages and scientific calculators are readily available for finding the roots of a characteristic equation.)

Let us look at these results another way. Remembering that $C_{BIG} >> C$, the total circuit of *Figure 4* can be studied over two frequency ranges: a high frequency range where C_{BIG} can be considered a short-circuit, and a low frequency range where C can be considered an open-circuit.

In the high frequency range, R_P is in parallel with R_N. To get a net positive resistance, we must choose $R_P < |R_N|$, which is essentially the constraint of Equation (8).

In the low frequency range, the sub-network is again second-order. In analyzing this network to find its characteristic equation, we must choose $R_P > L/(C_{BIG}|R_N|)$ for it to be stable. This is the constraint in Equation (9).

Furthermore, using the example numbers, the low-frequency sub-network has two complex poles essentially equal to the complex poles found for the entire network. Therefore, it is with this low-frequency sub-network that we can easily determine the stability of the overall network.

Summary

One straight forward, intuitive way to understand how to stabilize a distributed power supply system is to study the circuit formed by the source impedance and the converter's incremental input impedance. If this circuit is stable, the system is stable.

References:

1. Middlebrook, R.D., "Input Filter Considerations in Design and Application of Switching Regulators," IEEE IAS Annual Meeting, 1976.
2. Feng, X. et al, "Individual Load Impedance Specification for a Stable DC Distributed Power System," IEEE APEC Record, 1999.
3. Erickson, R.W., "Optimal Single Resistor Damping of Input Filters," IEEE APEC Record, 1999.

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