Comparison of PWM Voltage and Current Mode Control Schemes vs. Improved Hysteretic Mode Control in Switch Mode Power Supplies (SMPS)

Marcus Zimnik

Texas Instruments, Inc.
Haggertystrasse 1, D-85356 Freising
Phone: +49 8161 / 80-3839 Fax: +49 8161 / 80-4523 Email: m-zimnik@ti.com

Abstract: **Different control schemes PWM voltage and current mode control as well as hysteretic control are discussed in terms of load transient response. A hysteretic mode controller circuit will be shown and compared to a voltage mode PWM controller circuit. Measurement results from these circuits complement the paper.**

1. Introduction:

High current low output voltage applications emerge daily with the introduction of new generation DSPs, microprocessors and data communication systems. At the same time operating frequencies of those processors are rising. Powering these devices requires power supplies that are able to handle the high dI/dt rates of up to 150A/µs, i.e. power supplies have to have a very fast transient response. One way to achieve these requirements is to increase the switching frequency of the power converter. This increases switching and magnetic losses. Conventional control schemes like PWM voltage mode and current mode control are often too slow to respond to very fast transients. Improved hysteretic control can provide a solution to this issue.
The paper starts with a review of the small signal bandwidth of the voltage mode and current mode controlled converter and what the limiting factors for the maximum achievable small signal bandwidth of those control schemes are. Large signal bandwidth of a converter is always *less than or equal* to small-signal bandwidth, because before the converter's loop can run into some nonlinearity, it first has to respond, and the response is set by the small-signal bandwidth.

2. Small Signal Transfer Function of a Voltage Mode Buck Converter:

Voltage-mode control is used for a long time in the first switching regulator designs. Voltage mode has a single voltage feedback path, with pulse width modulation performed by comparing the voltage error signal with a constant ramp waveform. Figure 1 shows the basic configuration.

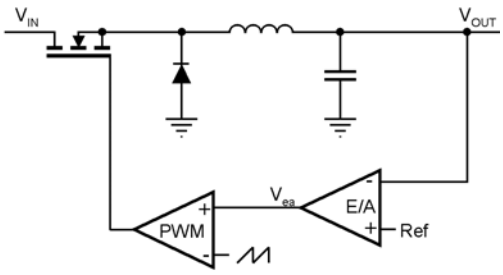

Figure 1: Voltage Mode Control

The control to output gain of a continuous inductor current buck operated in voltage mode is:

$$\frac{v_{out}}{v_{ea}} = \frac{V_{ea}}{V_s} H_e(s)$$

$$H_e(s) = \frac{1 + s/\omega_z}{1 + (s/\omega_o)/Q + (s/\omega_o)^2} \qquad (1)$$

$$\omega_o = \frac{1}{\sqrt{LC}}$$

$$\omega_z = \frac{1}{R_{ESR} C}$$

$$Q = \frac{R_{out}}{\omega_o L}$$

V_s = sawtooth ramp amplitude at '-' input of PWM comparator

Voltage mode control has a double-pole output filter. There is an abrupt 180° phase lag at filter resonance which will cause ringing and instability if not compensated This requires either a dominant-pole low frequency roll-off at the error amplifier or at least one added zero in the compensation. The typical compensation network for a voltage mode controlled buck converter is shown in figure 2.

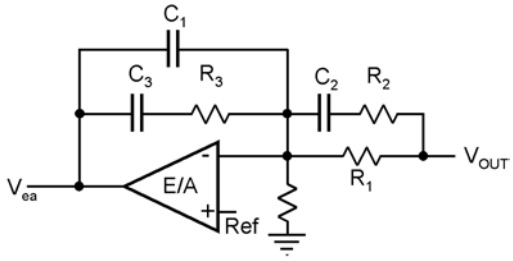

Figure 2: Typical Compensation Network for a Voltage - Mode Controller

This looks quite complicated and so does the transfer function of this compensation network. Assuming $R_1>>R_2$ & $C_3>>C_1$, the simplified transfer function becomes:

$$H_{ea}(s)=\left(\frac{1}{sR_1C_3}\right)\cdot\left[\frac{(1+sR_3C_3)\cdot(1+sC_2R_1)}{(1+sR_3C_1)\cdot(1+sC_2R_2)}\right]$$

3. Small Signal Transfer Function of a Peak Current Mode Buck Converter:

The peak current mode control method uses two control loops - an inner, current control loop, and an outer loop for voltage mode control. Figure 3 shows a buck converter using current mode control.

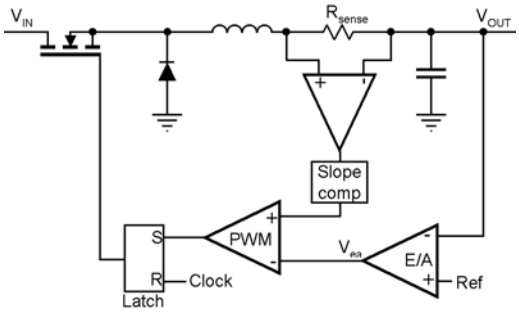

Figure 3: Peak Current Mode Control

When the switching transistor is on, current through R_{sense} is proportional to the upward ramping filter inductor current. When the ramp voltage V_s reaches V_{ea} (the amplified output voltage error), the switching transistor turns off. Thus, the outer voltage control loop defines the level at which the inner loop regulates peak current through the switch and through the inductor.

The control to output gain of a continuous inductor current buck operated in current-mode is:

$$\frac{v_{out}}{v_{ea}}=KR_{out}H_e(s)$$

$$K=\frac{\max I_L}{\max V_{ea}}$$

$$H_e(s)=\frac{1+s/\omega_z}{1+(s/\omega_p)}$$

$$\omega_p=\frac{1}{R_{out}C}$$

$$\omega_z=\frac{1}{R_{ESR}C}$$

Current-mode control eliminates the inductor pole and 2nd order characteristic because the inner current control loop includes the output filter inductor. The outer voltage control loop then has only the single pole of the output filter capacitor and load resistance. The typical compensation network for a current-mode controlled converter is shown in figure 4.

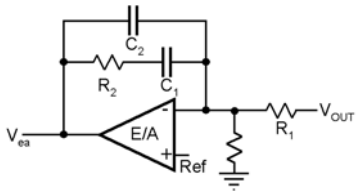

Figure 4: Typical Compensation Network for a Current – Mode Controller

The compensation network for current mode control looks much easier than for voltage-mode control and so does the transfer function. Since C_2 is generally much smaller than C_1 and often not used, the transfer function can be simplified and written as:

$$H_{ea}(s)=\frac{1+sR_2C_1}{sR_1C_1}$$

4. NO Small Signal Transfer Function for a Hysteretic Controller:

Hysteretic control (or two-state, bang-bang, ripple regulator, free-running regulator) is the simplest control approach, which has been used for a long time. This is probably the earliest controller or regulator. With progressing semiconductor-manufacturing technology, significant improvements in the comparator stage, the heart of the hysteretic controller have been made. That brought hysteretic control back to new attention.

A hysteretic controller is a self-oscillation circuit that regulates output voltage by keeping it within a hysteresis window set by a reference voltage regulator and a comparator. An example of a buck converter using a hysteretic controller is shown in Figure 5.

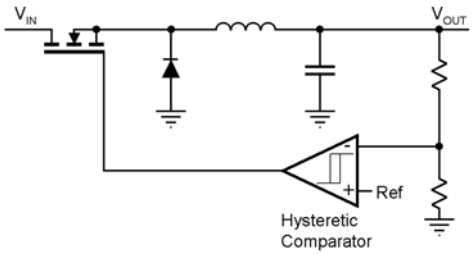

Figure 5: Hysteretic Mode control

Unlike the previously described control approaches, hysteretic mode control doesn't have a feedback loop that requires compensation.

5. Small Signal Bandwidth Constraints of Current Mode Control and Voltage Mode Control:

The first three paragraphs of this chapter apply to any control schemes that require a feedback loop with compensation. The maximum crossover frequency, i.e. the bandwidth of the small signal compensation network is limited by several factors.

The first limiting factor is simply the sampling theorem. It says that it is not possible to transmit information at any frequency greater than half the sampling frequency. In a switch mode power supply the sampling frequency is the switching frequency. So for example, the *theoretical maximum* bandwidth one can achieve with a 2MHz-switching converter is 1MHz. This would result in a *theoretical minimum* transient response of 1µs to a load step.

[9] states that a system becomes unstable when the compensation frequency exceeds $f_s/(2\pi D)$ with Duty cycle greater than 0.5. At $f_c = f_s/(2\pi D)$, the system response becomes maximally fast.

At $f_c = f_s/(2\pi D)$ the error amplifier gain may be high enough to cause the amplifier output ripple voltage to drive the error amplifier into saturation, necessitating a further reduction in f_c.

The following limits apply especially to voltage – mode.
Voltage mode control has a double-pole output filter. This requires either a dominant-pole low frequency roll-off at the error amplifier or at least one added zero in the compensation. This means a lot of error amplifier gain-bandwidth and large compensation capacitors with time constant in the order of milliseconds are required. This makes it hard to get high gain bandwidth.

Other difficulties are that capacitive loading and the ESR of the output cap affects compensation.

The closed-loop gain in voltage mode will change with the output voltage. But this also forces a reduction in bandwidth. This can be a problem since today's microprocessors require changing supply voltages depending on the required computation power.

Another thing to consider in the design of the compensation network is the transient response vs. the damping factor. In equation (1), the Q-factor appears in the transfer function H(s). High Q-poles lead to overshoot and ringing. In most power applications, overshoot is unacceptable. So the Q-factor must be sufficiently low, often 0.5 or less, corresponding to a phase margin of at least 76°. But with very low Q, the low-frequency pole leads to a slow step response.

All this things limit the maximum bandwidth of a voltage mode controller feedback network. In many voltage mode controlled applications, the crossover frequency is therefore chosen to be a 4^{th} to 6^{th} of the switching frequency. This means in return that it takes at least 4 to 6 switching periods until the control loop *realizes* a change in output voltage. After this, it takes another few switching cycles to react to the output load transient. All this yields to a slow transient response when the controller is operated in voltage mode. The only way to improve the transient response is to increase the switching frequency and with it the bandwidth of the compensation network.

For current mode many of those restrictions don't apply. The current mode control to output function incorporates only a single pole with 90° phase lag. This makes current mode control inherently stable without additional compensation; it is easy to get high loop gain and excellent small signal dynamic performance.
Current-mode control provides also freedom from the effects of variable capacitive loading and faster recovery from overload and.
There's no 2^{nd} order characteristic in the transfer function, and therefore no Q-factor. Thus, high Q-poles can't lead to overshoot and ringing.

6. Large Signal Characteristics of Current Mode Control, Voltage Mode Control and Hysteretic Control:

Compensation relates to the small signal disturbance. If a disturbance is large, such as output load steps, the system response will be determined by nonlinear aspects, such as Op-amp slew rate or rail voltages, or maximum and minimum achievable duty cycles, etc. But as mentioned already in the introduction, large signal bandwidth of a converter is always *less than or equal* to small-signal bandwidth, because before the converter's loop can run into some nonlinearity, it first has to respond, and the response is set by the small-signal bandwidth.

The phase margin provided by the compensation network also relates to the transient response. Lower phase margins like 45°, give good transient response at the expense of peaking of the closed-loop transfer function and output impedance. Higher phase margins, like 75°, give flat closed-loop transfer functions and minimum peaking of

output impedance, but at the expense of speed and settling time.

When looking into continuous mode circuits the large filter inductance values make it impossible for the inductor current to follow rapid changes in load regardless of the control method. The rate of change of inductor current depends on the excess volt-seconds available when the duty cycle is at its maximum limit. It may take up to 10 or 20 switching periods for the inductor current to follow a step change from half to full load, especially at low V_{in}. This limitation in the slew rate of inductor current causes the power supply output voltage to go out of regulation temporarily. The error amplifier is driven into the stops, causing the voltage control loop to become temporarily open until after the inductor current reaches the new load current level. During this time, the error amplifier is driven into its bounds (max. V_{ea}). The voltage at the inverting input is no longer held equal to V_{ref}, and C_2 and C_3 in the voltage mode compensation network in figure 2 will charge to abnormal voltage levels. When the inductor current reaches the new value and the loop is again able do resume functioning, the error voltage on C_2 causes a corresponding error in V_{out}. So C_2 in the voltage mode compensation network severely impairs large signal transient performance. In other words, the compensation necessary for good small-signal performance with voltage mode control causes poor large-signal performance, i.e. large output glitches that take a long time to recover.
For both voltage mode and current mode control, the integrating capacitor is present in the feedback loop (C1 in figure 2 for voltage mode and C2 in figure 4 for current mode). This integrating capacitor limits the slew rate of the error amplifier output and therefore limits the response time of the error amplifier to large signal output errors.
Even though the integrating capacitor is present in the current mode control error amplifier, its value is less than one tenth the value and time constant of the 2 capacitors necessary with the voltage mode control error amplifier. This small capacitor cancels rapidly as soon as the inductor current reaches the new value of load current.
Therefore, current mode control can adapt quicker to load changes than voltage mode can.

With voltage mode, any change in line or load current must first be sensed as an output change and then corrected by the feedback loop. This results in slow response. Voltage feed-forward eliminates the effects of line voltage variations. Voltage feed-forward is accomplished by making the slope of the ramp waveform proportional to the input voltage. This provides a corresponding and correcting duty cycle modulation with no action needed by the feedback loop. The result is a constant control loop gain and instantaneous response to line voltage changes.
In current mode the voltage feed-forward characteristic is inherent on how current mode works. A line voltage change immediately causes a correcting duty cycle modulation with no action needed by the voltage loop.

Many of the above-described problems are not present in hysteretic mode control. Even though the inductor current cannot keep up here with large step changes in load current as well, the excess volt-seconds available are not limited by maximum duty cycle. Hysteretic control has a duty cycle range that covers the entire range from zero to one. It does not have any restrictions on conduction interval of power switches that most of the other control approaches have. This decreases the recovery time after a load current transient occurred.
Also hysteretic control doesn't require any compensation. This means that the error signal will not be delayed by any loop compensation components. It also doesn't have all the drawbacks with charging and discharging compensation capacitors to abnormal voltage levels and the time delays that are associated with it.
Due to its operating principle, hysteretic control reacts on the load current transient in the same switching cycle that the transient occurs. Its transient response time depends only on delays in the hysteretic comparator and drive circuitry.
Hysteretic control has the drawback that the switching frequency depends on the output filter characteristics, input and output voltage, hysteresis window, and internal delays. A simplified equation for the switching frequency is [8]

$$f_s \cong \frac{V_{out} \cdot (V_{in} - V_{out}) \cdot R_{ESR}}{V_{in} \cdot L \cdot \text{Hysteresis window}}$$

7. Improved Hysteretic Mode Control [8]

One can see from the switching frequency equation that the switching frequency is proportional to the output capacitors ESR. This means that using an ideal capacitor with very low ESR (like connecting many ceramic capacitors in parallel) is a problem because the operating frequency becomes relatively low. With some additional circuitry the dependence of the switching frequency of the output capacitors' ESR can be eliminated. This yields to an improved version of the classical hysteretic controller as shown in Figure 6. The additional R_{add} – C_{add} circuitry is added to the buck regulator. R_{add} is connected between the input of the hysteresis comparator and the midpoint of the power switches. C_{add} is connected between the input of the comparator and ground.

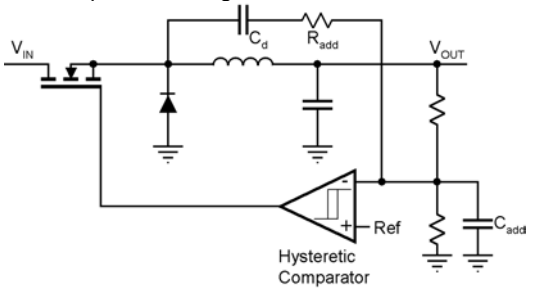

Figure 6: Buck Converter with Improved Hysteretic Control

This R_{add} – C_{add} circuitry forms an additional ramp signal through the input of the hysteretic comparator. The two signals are summed together at the comparator input of - the ramp signal from R_{add} – C_{add} circuitry and the signal from the output voltage of the converter. With proper selection of R_{add} and C_{add} the amplitude of the additional ramp signal is greater than the output ripple of the converter. Then the switching frequency depends on R_{add} – C_{add} values only and is independent of the output filter characteristics including the ESR, ESL, and C of the output capacitor. The simplified equation for the switching frequency of the modified controller is

$$f_s = \frac{1}{T_s}$$

$$T_s = \frac{V_{in} \cdot R_{add} \cdot C_{add} \cdot \text{Hysteresis window}}{V_{ref} \cdot (V_{in} - V_{ref})} + T_{Delay} \cdot \left(2 + \frac{V_{ref}}{V_{in} - V_{ref}} + \frac{V_{in} - V_{ref}}{V_{ref}}\right)$$

T_{Delay} characterizes comparator and drive circuitry delays.

C_d is brought in series with R_{add} to avoid that the output voltage is depended on the DC level at the junction of the Diode and the inductor. The DC decoupling capacitor is shown already in Figure. The value of this capacitor has to be much higher than C_{add}. With the decoupling capacitor C_d, the output voltage is defined by

$$V_{out} = V_{ref} \cdot \left(1 + \frac{R_1}{R_2}\right)$$

The switching frequency becomes independent on output capacitor characteristics, so high frequency, low-cost ceramic or film capacitors can be used while maintaining the same excellent load current transient response characteristics.

8. Experimental results

Measurements on voltage mode controller

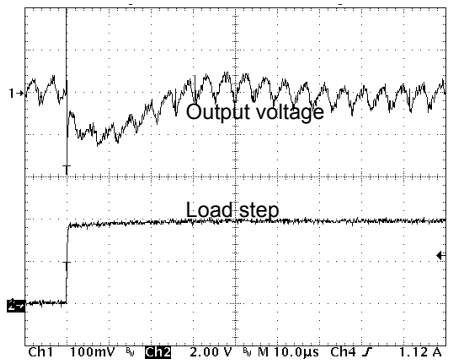

Figure 7: 50% load-step response of Voltage Mode Controller

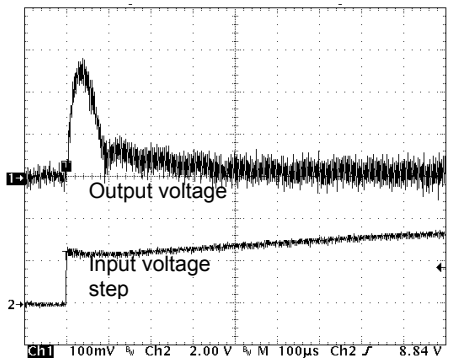

Figure 8: Voltage Mode Controller output voltage at a 50% line input voltage step and 10% nominal output load

Measurements on hysteretic controller

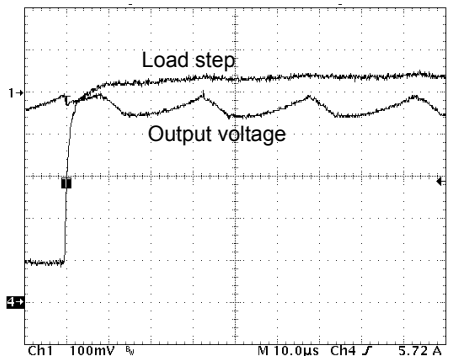

Figure 9: 50% load-step response of Hysteretic Controller

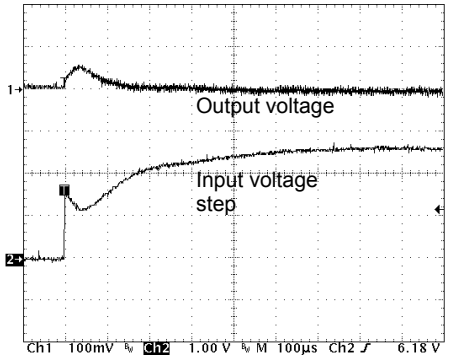

Figure 10: Hysteretic Controller output voltage at a 50% line input voltage step and 10% nominal output load

Measurements on improved hysteretic controller

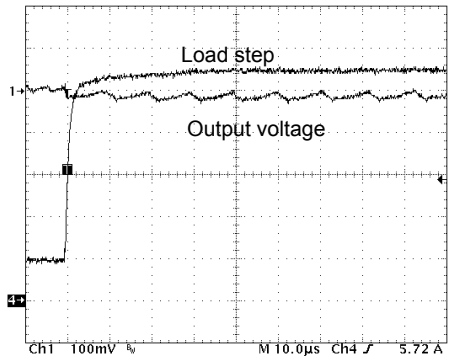

Figure 11: 50% load-step response of Improved Hysteretic Controller

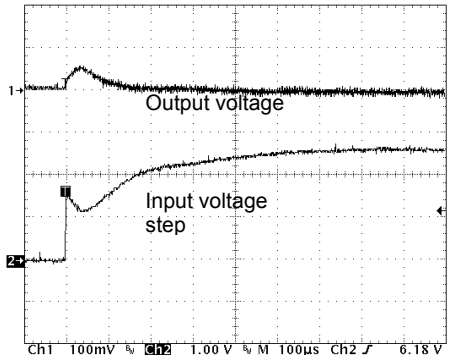

Figure 12: Improved Hysteretic Controller output voltage at a 50% line input voltage step and 10% nominal output load

9. Discussion of the experimental results:

Looking at figures 7, 9, and 11:
The load-step response of the voltage mode controller shows a significant drop in output voltage when the load-step occurs. It takes nearly 3 switching cycles until the control mechanism reacts to the step. After 8 switching periods (approx. 35µs), the output is in regulation again. The load-step responses of the hysteretic controllers show immediate response to the load-step within the same switching cycle. The improved hysteretic controller has about the 3rd the output voltage ripple of the normal hysteretic controller.

Now looking at screenshot figures 8, 10, 12:
When an input voltage step of 50% occurs, the tested voltage controller circuit overshoots the nominal output voltage by nearly 5.6% (figure 8). The time it needs to recover is about 300µs. Both hysteretic controllers overshoot the nominal output voltage only by around 1.7% (figures 10 and 12). At this point, there's no difference between the normal hysteretic controller and the improved hysteretic controller.

10. Conclusion:

Different control methods have been evaluated in terms of transient response time. Experimental results show that adding simple external circuitry improves standard hysteretic control. The improved version has lower output voltage ripple than standard hysteretic control while maintaining the same fast transient response.

11. References:

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[9] J. R. Wood, "Taking Account of Output Resistance and Crossover Frequency in Closed Loop Design," Powercon 10, pp. D4.1 – D4.16, March 1983