Power Converter Design Using the Saber Simulator

A Step-By-Step Guide to the Design of a

Two-Switch, Voltage-Mode, Forward Converter

Using the Saber Simulator

By
Steve Chwirka
Analogy, Inc.
Beaverton, Oregon
(503) 626-9700

Table of Content

1.0 Scope of Document

This engineering document will guide the reader through the step-by-step design of a two switch, voltage mode, forward power converter using the Saber Simulator. In the process, we will describe typical design considerations and problems and how to overcome them. Validation of each step in the design process will be performed using Saber.

2.0 Specifications

The following specifications will be used to design the power converter.

2.1 Input Specifications

Line Input			150 Vdc, ± 6 V
$P_{in}(max) = \frac{P_{out}(max)}{Eff}$		= 30/.85	35 Watts

2.2 Output Specifications

V_{out}	15Vdc
V_{out}(ripple)	≤ 25mV p-p
Iout	50mA to 2A
Iout(ripple)	≤100mA p-p
$P_{out}(max) = (15V)(2A)$	30 Watts

2.3 Other Specifications

Efficiency	≥ 85%
Switching Frequency	200KHz (derived)

3.0 Step-By-Step Design Process

This section details the steps necessary to design the power converter.

3.1 Open Loop Design

3.1.1 Define the Duty Cycle and Turns Ratio of the Transformer

The basic relationship in a forward converter is

$Vout \cong (Vin)(1 / n)(D)$ where

Vout =dc output voltage

n = turns ratio = n_p / n_s

D = duty cycle

Given that **Vout = 15VDC** and **Vin = 150 VDC**, we see that (1 / n)(D) must equal 0.1

i.e. 15 = (150)(.1)

The duty cycle of a forward converter should not exceed .5. Therefore we will choose a value which is between 0 and 0.5. In this example we choose **D = 0.3**, approximately the midpoint of the range.

Therefore we know (1 / n)(D) = .1

or 1 / n = .1 / D = .1 / .3 = 1/3

so **n = 3**

The next step is to define the maximum and nominal duty cycle which include the output diode losses. These values will be needed for future calculations.

$$Dmax = \frac{Vout}{(Vin_{(min)})(1/n)}$$

n = turns ration = np / ns = 3

$Vin_{(min)}$ = 144 (per specifications)

Vout = 15V + (output diode losses ≅ .85V) = 15.85V

∴ **Dmax = 15.85 / (144)(1/3) = .3302**

Note that this is less than .5, the maximum duty cycle allowed in a forward converter.

$$Dnom = \frac{Vout}{Vin_{(nom)})(1/n)}$$

$Vin_{(nom)} = 150Vdc$

∴ **Dnom = 15.85 / (150)(1/3) = .317**

Note that this is greater than .3 calculated earlier because it takes the output diode into account.

3.1.2 Design the Rectifier and Filter Capacitor (Optional Section)

Note: A full-wave bridge rectifier will be used to allow the design of a smaller filter capacitor.

FIGURE 1 shows the rectified waveform, the desired DC input voltage of 150VDC and the resulting input ripple voltage (Vr)

.

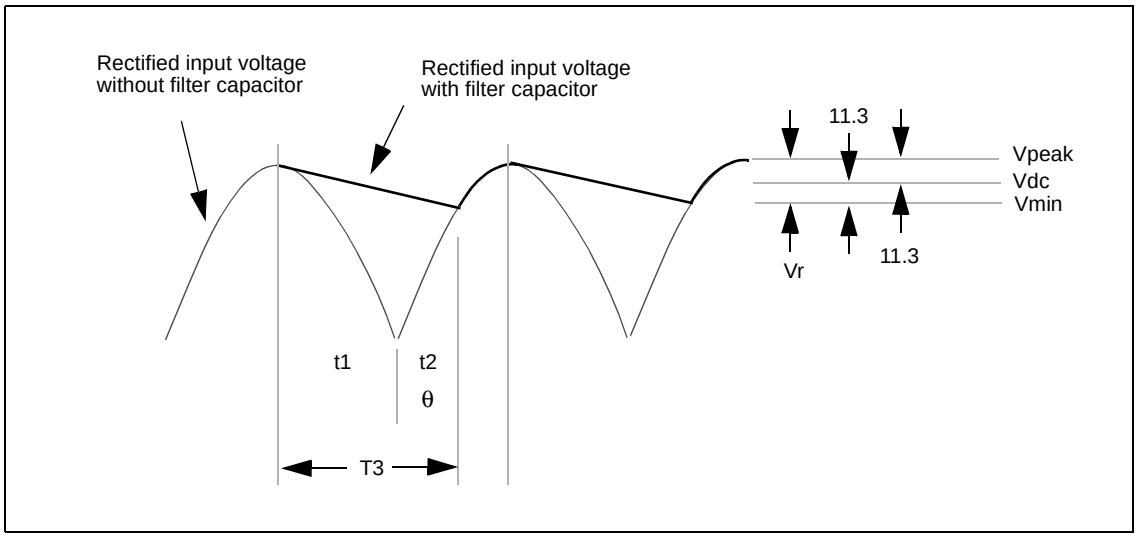


FIGURE 1 Filtering of Rectified Input Voltage

From FIGURE 1:

$Vpeak = Vin_{(ac)} / .707 = 115 / .707 = 162.7$

162.7 - (rectifier diode drops) ≅ 161.3V (where Vd ≅ .7)

$Vdc = 150$ V

$V_{min} = Vdc - (Vpeak - Vdc) = 150 - (161.3 - 150) = 138.7V$

The input filter capacitor value can be found in two ways

Input Capacitor Value - Method 1

$C = (I_{dc})(T3) / Vr$

$I_{dc} = Pin(max) / Vdc = 35W / 150V = .233A$

$Vr = (2)(Vpeak-Vdc) = (2)(11.3) = 22.6V$

T3 = Time the capacitor must deliver its energy to the circuit

Solving for T3:

$T3 = t1 + t2$

$t1 = (1/4)(1/f)$ where f = input frequency = 60Hz

$= (1/4)(1/60) = 4.166$ msec

Note: Most text books at this point assume that the input ripple is small and therefore that $t2 \cong t1$ which would yield

T3 = 4.166 msec + 4.166 msec = 8.33 msec

However, this is not the case in many designs. Therefore we need to use the following equations to calculate t2:

Referring to FIGURE 1:

$Vmin = Vpeak(Sin\theta)$

$$\theta = Sin^{-1}\left[\frac{Vmin}{Vpeak}\right]$$

$\theta = Sin^{-1}(138.7 / 161.3) = 59.3^o$

We know that $\dfrac{180^o}{(1/2)(1/f)} = \dfrac{\theta}{t2}$ where f = input freq = 60Hz

$$\therefore \quad t2 = \frac{(\theta)(1/2)(1/f)}{180^o} = (59.3)(1/2)(1/60) / 180^o$$

$t2 = 2.745$ msec

In other words:

$$t2 = \frac{\mathbf{Sin^{-1}\left[\frac{Vmin}{Vpeak}\right]\left[\frac{1}{2}\right]\left[\frac{1}{f}\right]}}{\mathbf{180^o}}$$

From input filter capacitor design equations we had

$C = (I_{dc})(T3)/ Vr$

$Vr = 22.6V$

$Idc = .233A$

$T3 = t1 + t2$

$t1 = 4.166$ msec

$t2 = 2.745$ msec

$\therefore$ $T3 = 4.166$ msec + 2.745 msec = 6.911 msec

Note the significant difference between 6.911 msec and the approximate calculation of 8.33 msec.

Final Calculation: C = (.233A)(6.9116 msec) / 22.6 V = 71.36 uF

Input Capacitor Value - Method 2

Using $E = CV^2 / 2$

$$C = \frac{(Pin_{(max)})(T3)}{(1/2)(Vpeak^2 - Vmin^2)}$$

$$= \frac{(35)(6.9116m)}{(1/2)(161.3^2 - 138.7^2)}$$

$= 71.36$ uF

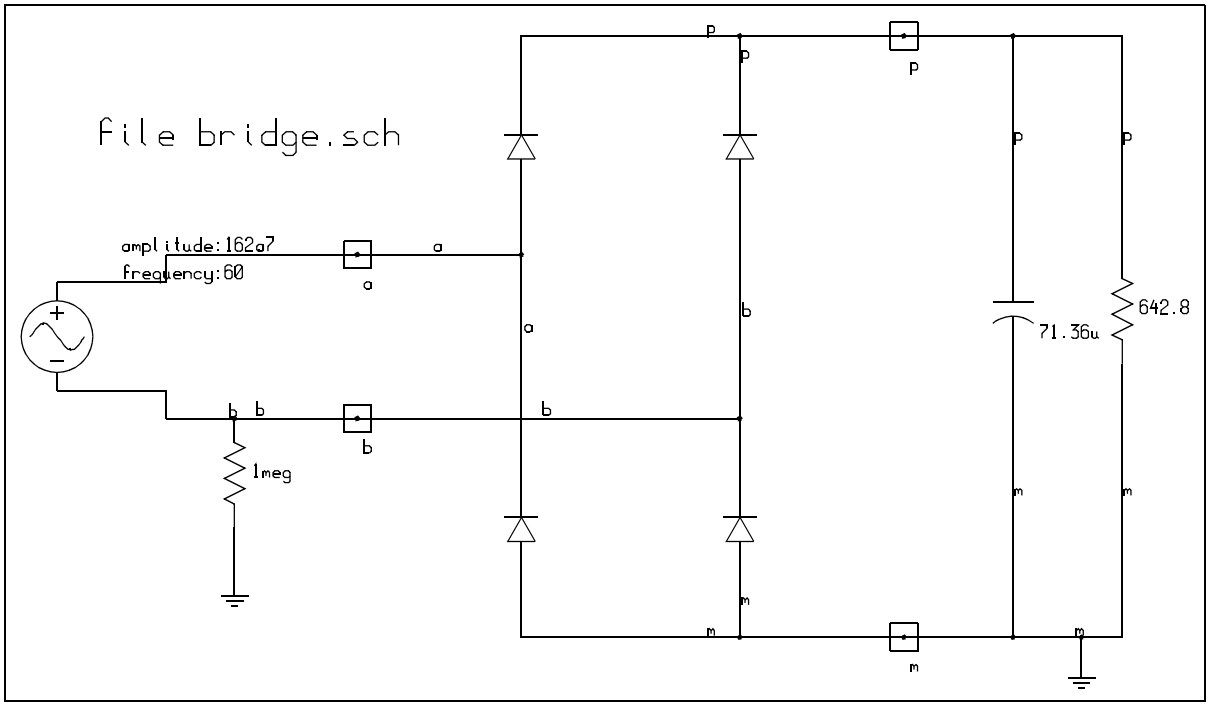


FIGURE 2 Circuit Used to Verify the Rectification and Filter Capacitance for a 35 Watt 115 Vac Input

Once the filter capacitor has been calculated, validate using the schematic shown in Figure 2.

This shows

- an input source:

  v.* m p = tran=(sin=(va=162.7, f=60))

  note: 115VAC / .707 = 162.7Vpeak
- filter capacitor with value of 71.36 uF as calculated
- load resistor which forces Pin(max) = 35W

  $P = V^2 / R \Rightarrow R = V^2 / P = (150)^2 / 35 = 642.8\Omega$

3.1.2.1 Validate the Rectifier and Filter Capacitor using Saber

View the results shown in Figure 3 and compare with the calculated values.

Note: Vpeak ≅ 161.3

Vmin ≅ 138.7

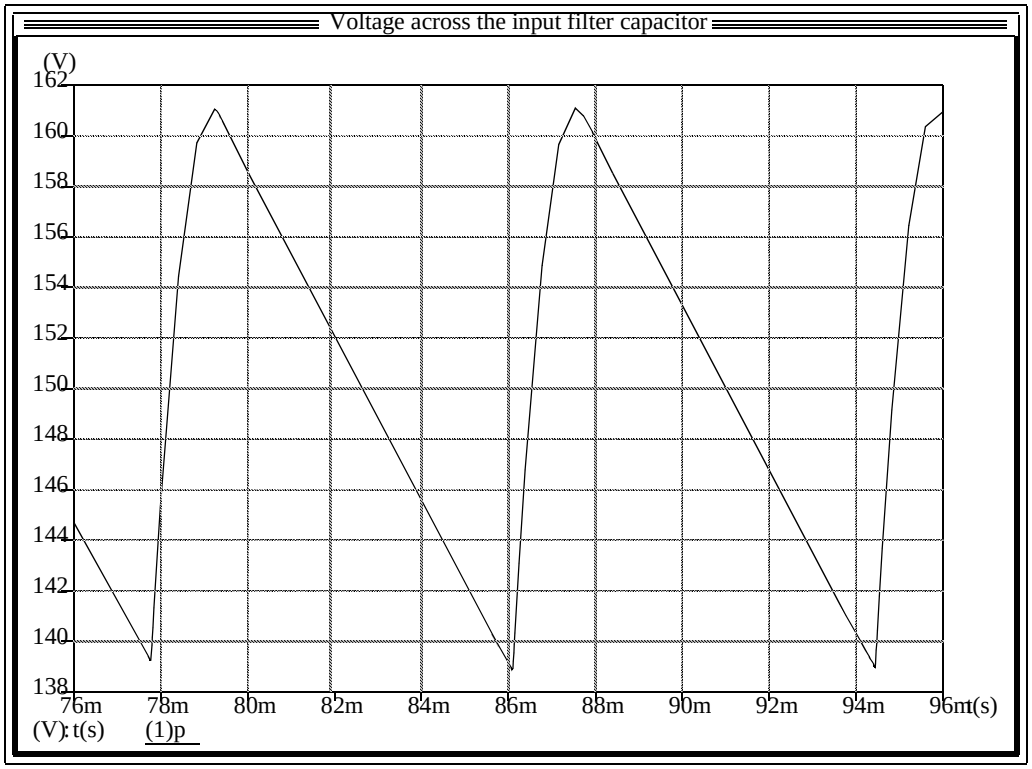


FIGURE 3 Voltage Across the Input Filter Capacitor

3.1.3 Output Filter Design

This section will describe the design of the output filter which consist of a 2-pole LC design. The output inductor will be calculated to limit the peak-to-peak ripple current, and the output capacitor will be calculated to limit the peak-to-peak output ripple voltage.

3.1.3.1 Inductor Design

The current waveform through the filter inductor is shown in Figure 4.

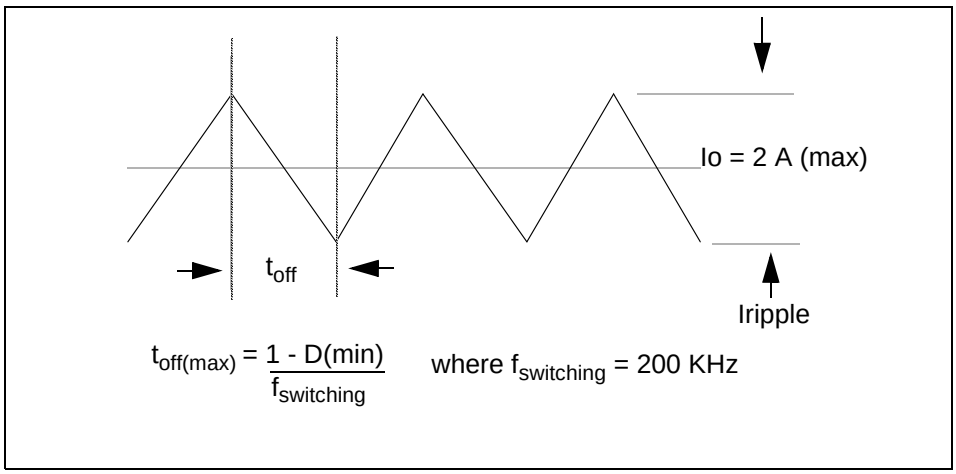


FIGURE 4 Current through the Filter Inductor

The allowed peak-to-peak current in the inductor is determined by the minimum load current specification. From the spec. we have Iout(min) = .05A. If the load current goes below .05A, the converter will go into discontinuous mode (the inductor current goes to zero). See Figure 5.

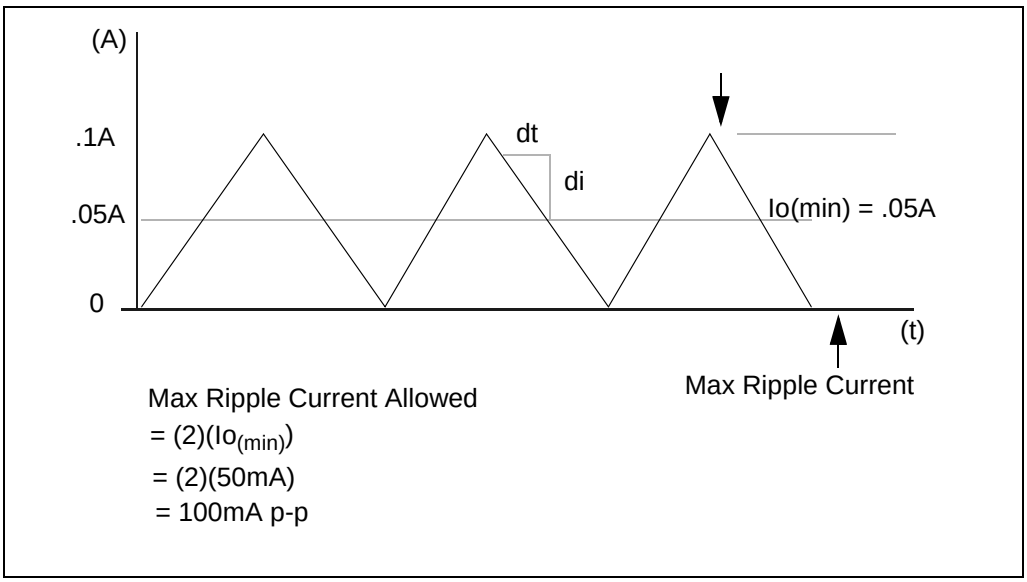


FIGURE 5 Current Through Filter Inductor

From Figure 4, it can be seen that the inductor's current decreases during the OFF time of the switch. In order to prevent discontinuous operation, the inductor current must not go to zero during this OFF time (at minimum load of .05A per the spec.)

Therefore the inductor will be sized to limit the peak-to-peak current to .1A p-p.

We know $V_L = L\ (di/dt)$

$L = V_L / (di/dt)$

where $V_L = 15V$

dt = max off time (see Figure 4)

$=(1 - Dmin) / (f_{switching})$

$= (1-0.3030) / 200KHz$

$\cong 3.5\ us$

di = .1A

$\therefore$ **L = 15 / (.1 / 3.5u)** $\cong$ **.53 mH**

3.1.3.2 Capacitor Design

The Vout(ripple) specification, along with the calculated ripple current coming through the inductor, determine the size of the output capacitor.

The following is used to calculate the capacitor value:

$$C = \frac{(1/8)\ Iripple}{(f)(Vripple)}$$

Iripple = .1A

f = 200KHz

Vripple = .025V (from spec)

$\therefore$ **C = (1/8) (.1) / (200K)(.025) = 2.5 uF**

Note that the ESR of the capacitor must not exceed:

$ESRmax = \Delta V / \Delta I = .025 / .1 = 0.25\Omega$

or the ripple voltage will increase.

3.1.4 Validate the Open Loop Design using Saber

Figure 6 shows the Open Loop configuration

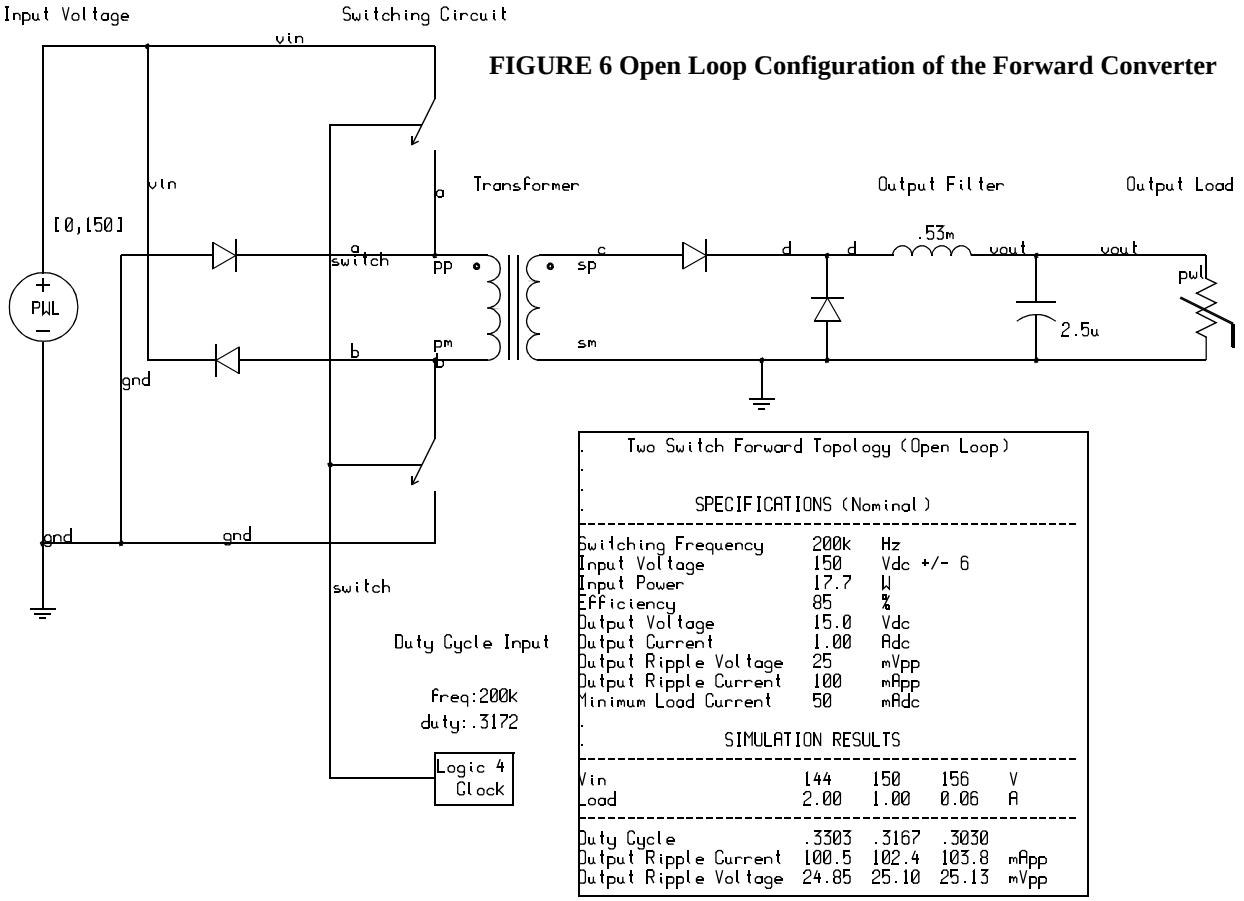


FIGURE 6 Open Loop Configuration of the Forward Converter

This is the Open Loop configuration of the Forward (two switch) converter. It is used to design the transformer's turns ratio and Inductance, the output filter, the Duty Cycle and switching frequency. The Open Loop design can then be simulated and validated to make sure the output voltage is correct based on a certain Duty Cycle, the output ripple voltage & ripple current are correct, etc.

Note: nominal values for input voltage = 150Vdc

max output current for load = 2A ($R_{load} = 7.5\Omega$)

duty cycle = nominal = .317

switching frequency = 200kHz

values for L, C, ESR

Run transient analysis

Check: with Vin = 150V, D = .317, n = 3, Vout should be 15V

I_L ripple should be .1A p-p

Vout ripple should be approx. .025V p-p

Figure 7 shows the results of the Open Loop simulation. Note that this validates the transformer's turns ratio, the output filter design, duty cycle, and switching frequency.

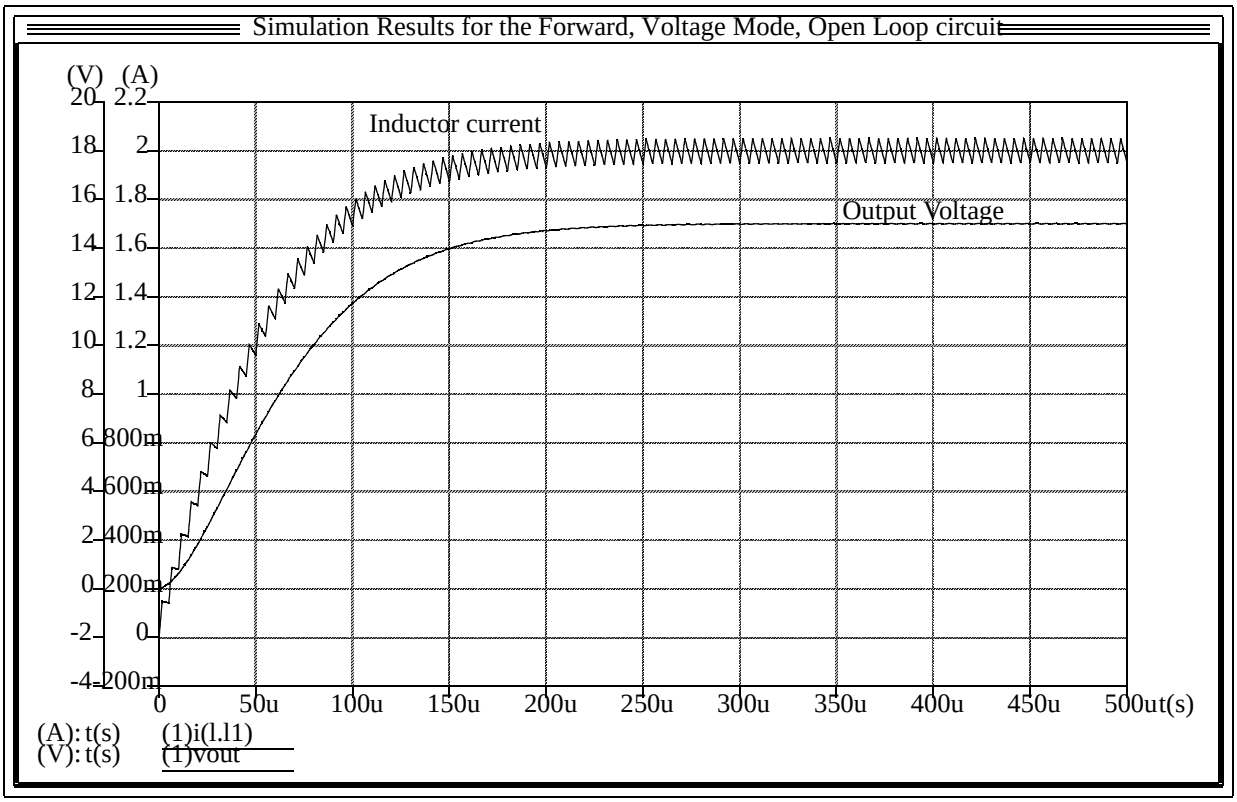


FIGURE 7 Open Loop Simulation Results

Figure 8 shows an expanded view of the inductor current and validates the ripple current (100mA p-p). Figure 9 shows an expanded view of the output voltage and validates the ripple voltage (25mV p-p)

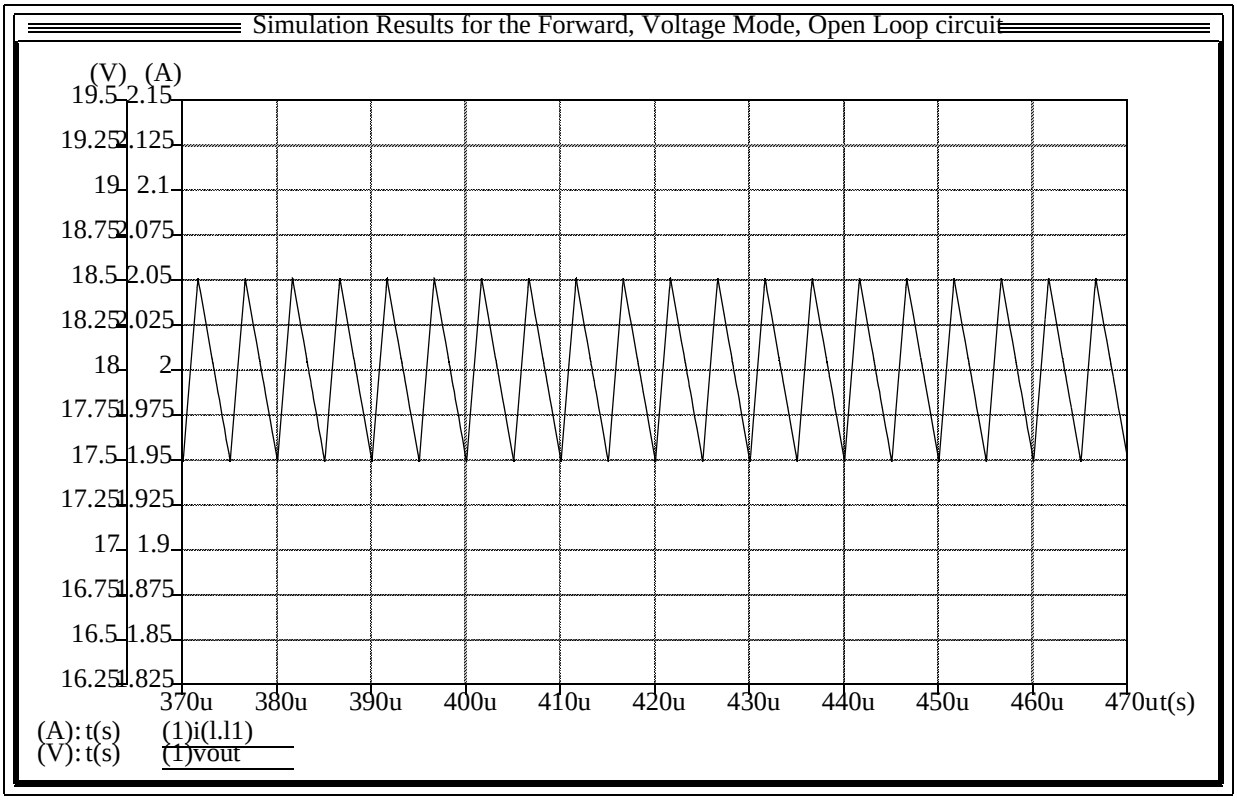


FIGURE 8 Inductor Ripple Current

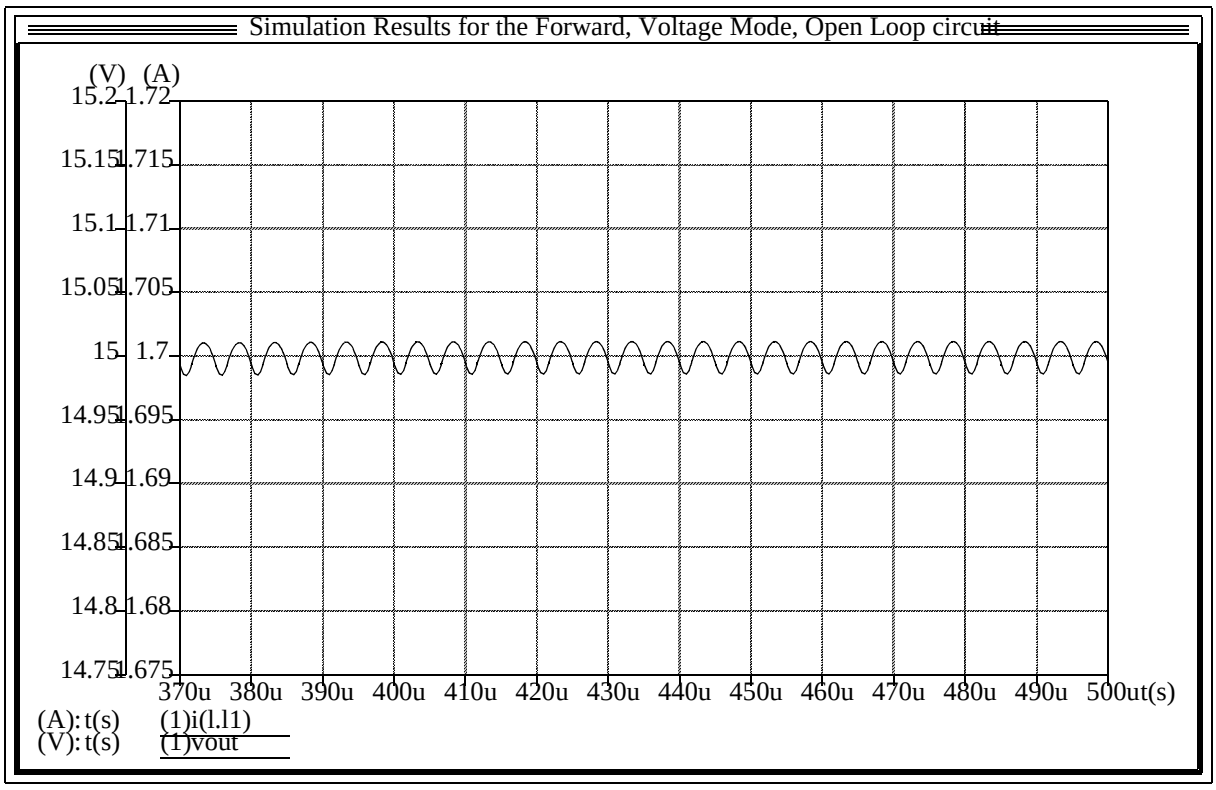
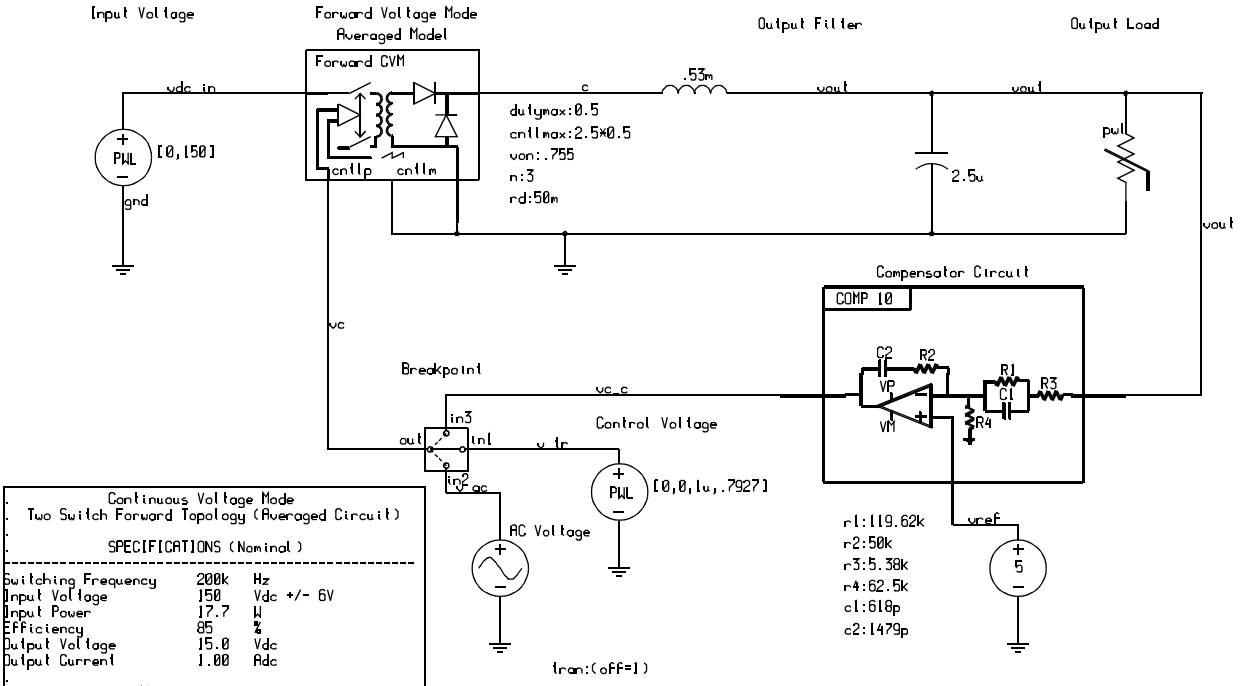


FIGURE 9 Output Ripple voltage

3.2 Compensator Design using an Averaged Model

The averaged circuit shown in Figure 10 lets you analyze the power supply without its switching circuitry. Using this averaged circuit, you can perform three types of simulations: an open-loop transient analysis, an open-loop small-signal AC analysis, and a closed-loop analysis. These simulations will provide the needed information to design and validate the compensation circuit.



Continuous Voltage Mode Two Switch Forward Topology (Averaged Circuit)				
SPECIFICATIONS (Nominal)				
Switching Frequency	200k	Hz		
Input Voltage	150	Vdc +/- 6V		
Input Power	17.7	W		
Efficiency	85	%		
Output Voltage	15.0	Vdc		
Output Current	1.00	Adc		
SIMULATION RESULTS				
Vin	144	150	156	V
Load	2.0	1.0	.06	A
Duty Cycle	.3303	.3161	.3030	

FIGURE 10 Averaged Configuration of the Forward Converter

This configuration is use to perform several simulations/analyses. The designer can first perform an open loop transient simulation to validate that the average model is providing the correct output voltage for a given control voltage. This transient simulation is also used to set up the operating point for the small signal AC simulation. The next simulation performed is a small signal ac to evaluate the "Control to Output" transfer function. The results are used to design the compensator circuit. Once the compensator circuit is designed, it can be included in another small signal ac simulation to validate the compensator and the feedback has the correct frequency response. The final simulation which can be done from this schematic is a closed loop transient analysis. This will validate that the closed loop circuit (using the averaged model) yields the correct control voltage and Duty cycle as expected by the designer.

To determine the control voltage for the input to the averaged model, the following control-to-output relationship for the forward converter is used:

$$V_{out} = \left(V_{in} \times \frac{1}{n} \times \frac{V_c}{V_{ramp}} \right) - V_d$$

where

$V_{out} = 15\,V$

$V_{in} = 150\,V$

$n = 3$

$V_{ramp} = 2.5\,V$

$V_d = 0.85\,V$

Rearrange the equation to determine the control voltage:

$$V_c = V_{ramp} \times n \times \frac{V_{out} + V_d}{V_{in}} = 0.7925$$

3.2.1 Validate the Averaged Model using Saber

Using the Saber simulator and the averaged circuit shown in Figure 10, an open-loop transient analysis is performed to verify the averaged model, and to set up the operating point for the small signal ac simulation. The results are plotted along with the results from the open loop circuit simulation and are both shown in Figure 11. Note the averaged model results track the switching circuit results very well.

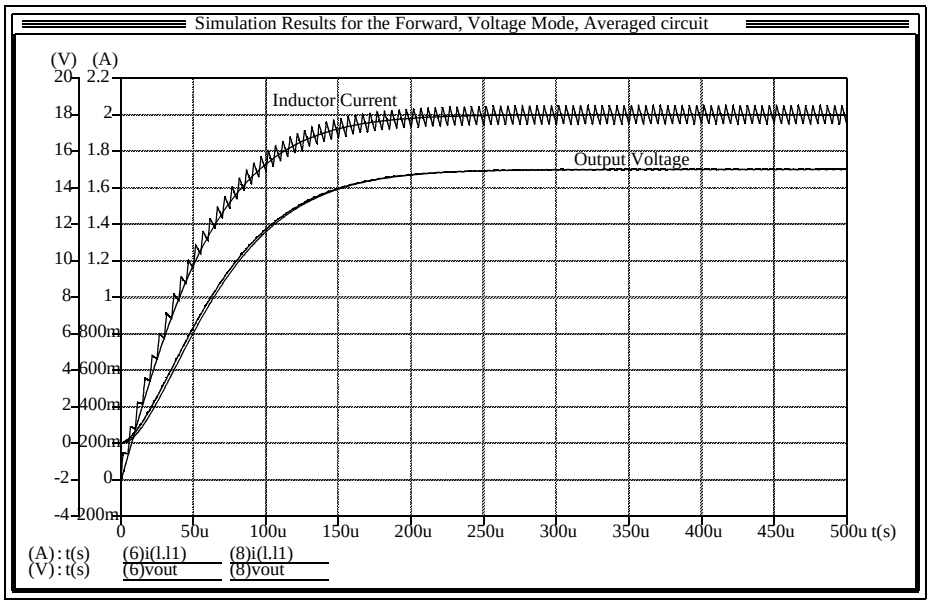


FIGURE 11 Averaged Model vs. Switching Circuit

Figure 12 shows the expanded view for the inductor current.

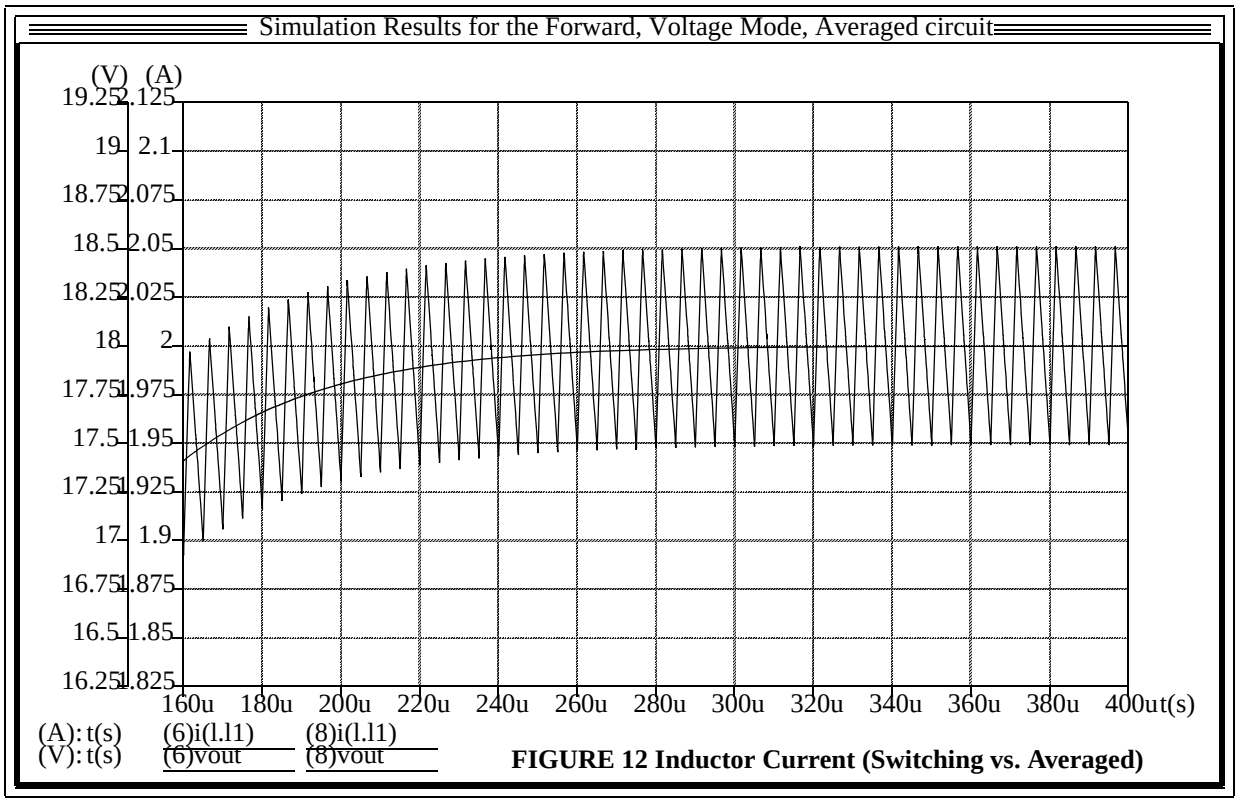


FIGURE 12 Inductor Current (Switching vs. Averaged)

Figure 13 shows the expanded view for the output voltage.

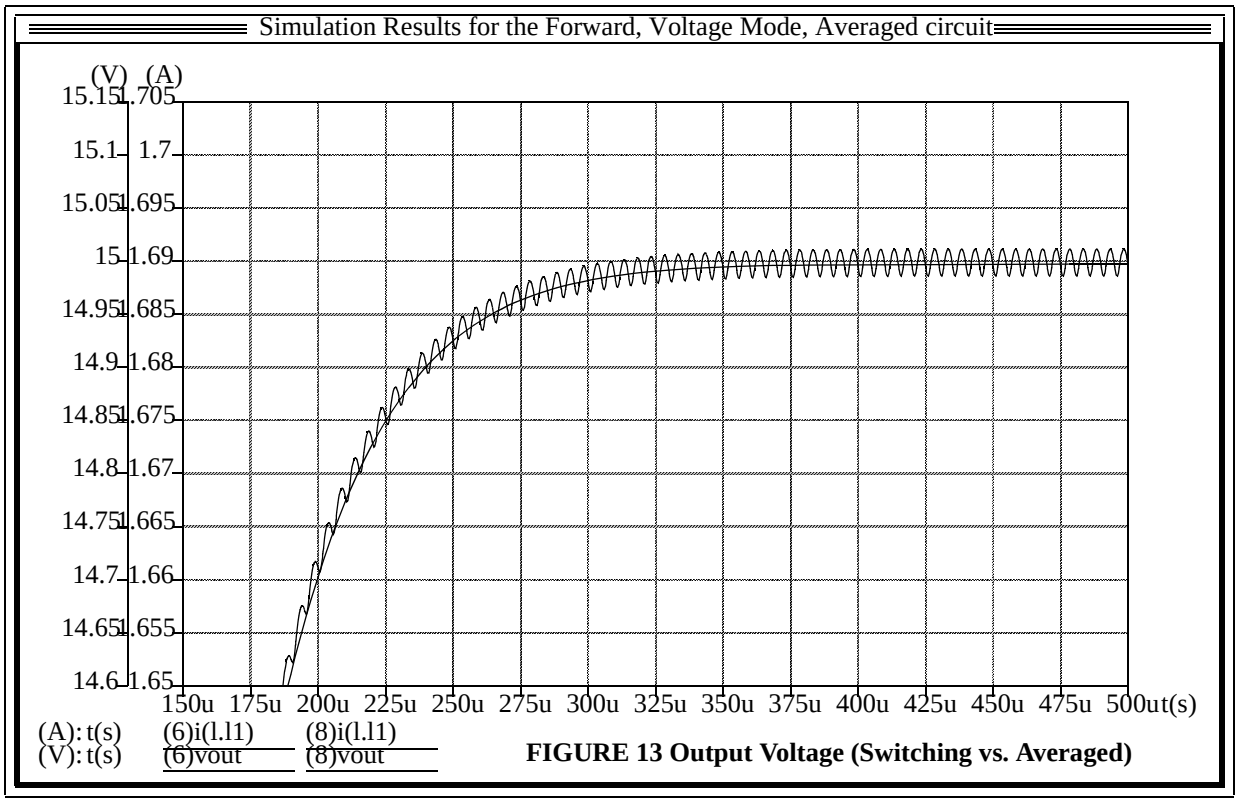


FIGURE 13 Output Voltage (Switching vs. Averaged)

3.2.2 Open-Loop AC Analysis

The next simulation performed using the averaged circuit is an open loop small signal ac analysis. The results are used to evaluate the control-to-output transfer function. This information is then used to design the compensator circuit. Figure 14 shows the frequency response of the control-to-output transfer function. It can be seen that the output filter yields a two pole roll off and a phase of close to 180 degrees:

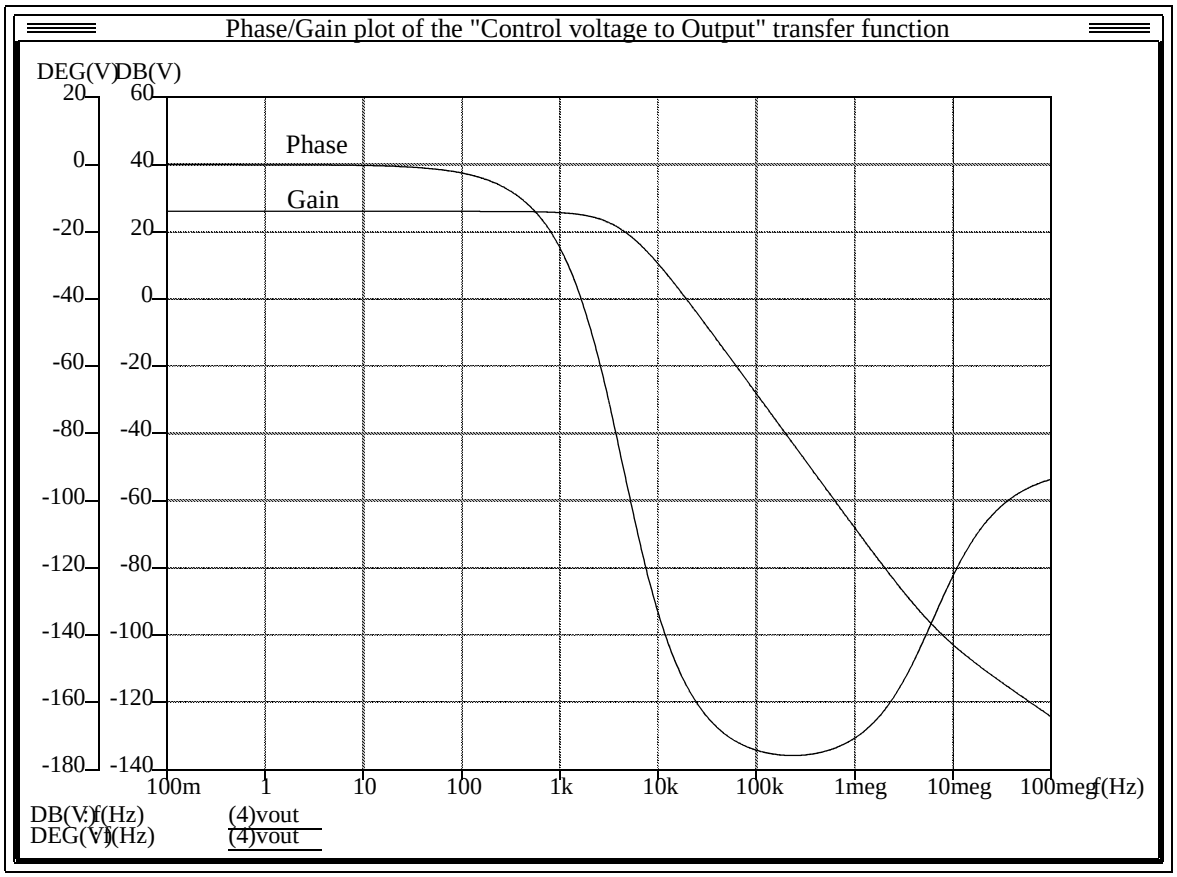


FIGURE 14 Phase/Gain plot of the Control-to-Output transfer function

3.2.3 Designing the Compensation Circuit

The compensator design will yield a 0dB crossover at approximately one quarter the switching frequency, and compensate the two-pole roll-off (180° phase) to approximate a single-pole roll-off (90° phase). The compensator will need two zeros to cancel out the effects of the two poles of the output filter. The frequency of the two zeros will be one-half the *resonant* frequency of the filter. The compensator will add in another pole at one-quarter the *switching* frequency, which cancels the effects of the ESR of the capacitor (zero). The approximate net results yield a single-pole roll-off at the crossover frequency.

Figure 15 shows the compensator circuit chosen .

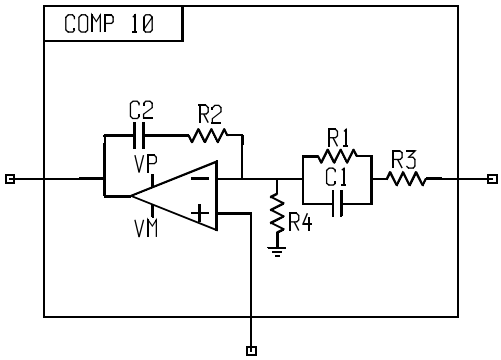


FIGURE 15 Type 10 Compensation Network

Find the desired break points for the above compensator

f_{z1} and f_{z2} = (1/2)(resonant freq of output filter)

$$\text{where } f_R = \frac{.159}{\sqrt{LC}} = \frac{.159}{\sqrt{(.53m)(2.5u)}} \cong 4.3 \text{ KHz}$$

$\therefore$ $f_{z1} = f_{z2}$ = (1/2)(4.3KHz) = 2.15 KHz

f_{p2} = (1/4)(switching freq) = (1/4)(200KHz) = 50 KHz

Calculate the values for R2 and R3 such that the high frequency gain at the desired crossover (50 KHz) yields an overall gain of 0 dB.

From the Bode plot of the open-loop circuit, it can be seen that to have a crossover (0 dB) at 50 KHz, there needs to be an additional 16.37 dB of gain. An additional 3 dB of gain is required since there will be a pole effect at 50 KHz (due to the pole of the integrator which is added via the compensator f_{p2}).

$\therefore$ R2 / R3 = (16.37 + 3) dB = 19.37 dB

where 19.37 dB = $\log^{-1}(19.37 / 20) = 9.3$

Choose R2 = 50K. We now have

50K / R3 = 9.3

R3 = 50K / 9.3 = 5.38K

The gain required at f_{z1} and f_{z2} is

$Av_{(2.15KHz)} = Av_{(50KHz)}(2.15K / 50K)$

= 9.3 (2.15K / 50K)

= .4

The gain at 2.15 KHz is determined by

$R2 / (R3 + R1)$

$\therefore \quad R2 / (R3 + R1) = .4$

$R1 = (R2 / .4) - R3$

$R2 = 50K$

$R3 = 5.28K$

$\therefore \quad$ **$R1 = (50K / .4) - 5.38K = 119.62K$**

The capacitors are calculated as follows

$$f_{z1} = f_{z2} = \frac{1}{2\Pi R_1 C_1} = \frac{1}{2\Pi R_2 C_2} = 2.15 \text{ KHz}$$

$$\therefore \quad \mathbf{C1} = \frac{.159}{(R_1)(f_{z1})} = \frac{.159}{(119.62K)(2.15K)} = \mathbf{618\ pF}$$

$$\mathbf{C2} = \frac{.159}{(R_2)(f_{z2})} = \frac{.159}{(50K)(2.15K)} = \mathbf{1479\ pF}$$

Calculate the value of R4, which provides a voltage divider for the 15V output. The reference voltage used is 5V, which means the value of R4 must be specified so that the 15V output is divided down to 5V:

$$15\left(\frac{R4}{R4 + (R3 + R1)}\right) = 5$$

Solving for R4 yields: **R4 = 62.5k**.

Therefore, final values for the compensator are:

R1	119.62k
R2	50k
R3	5.38k
R4	62.5k
C1	618 pF
C2	1479 pF

3.2.4 Validate the Compensator Design using Saber

With the compensator design complete, another small signal ac simulation is performed to validate circuit response. Figure 16 shows the results. Note the 0dB crossover is now at 50kHz and the phase margin is approximately 50°

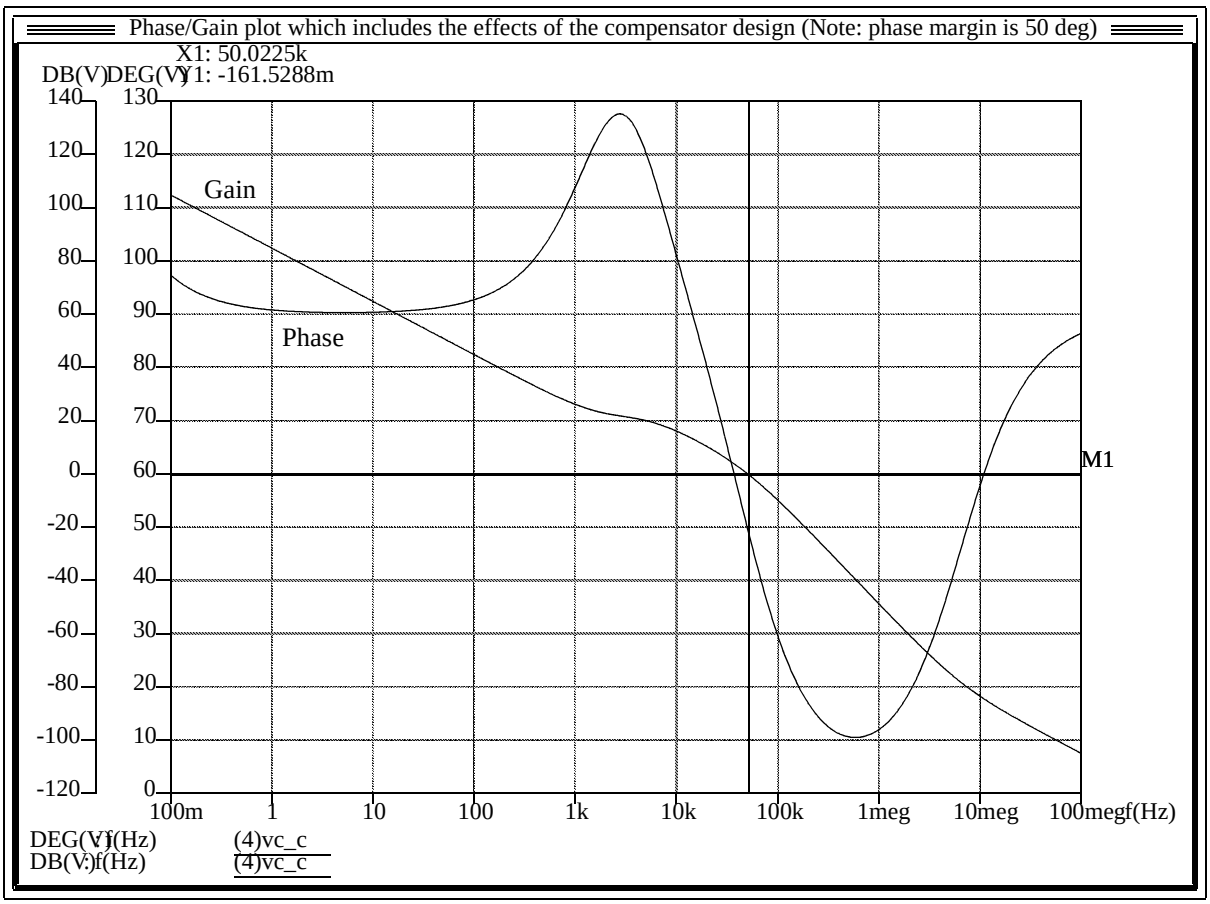


FIGURE 16 Phase/Gain plot (Post Compensator Design)

3.2.5 Validate the Closed Loop Parameters using Saber

Continuing to use the averaged circuit shown in Figure 10, the first closed-loop simulation is performed with the averaged model. This simulation validates the previous calculated parameters by having the system solve for them. Verify the following: (See Figures 17 & 18)

Vout	(should be 15 volts)
Vc (Control Voltage)	(should be approximately .7925)
Duty Cycle	(should be approximately .317)

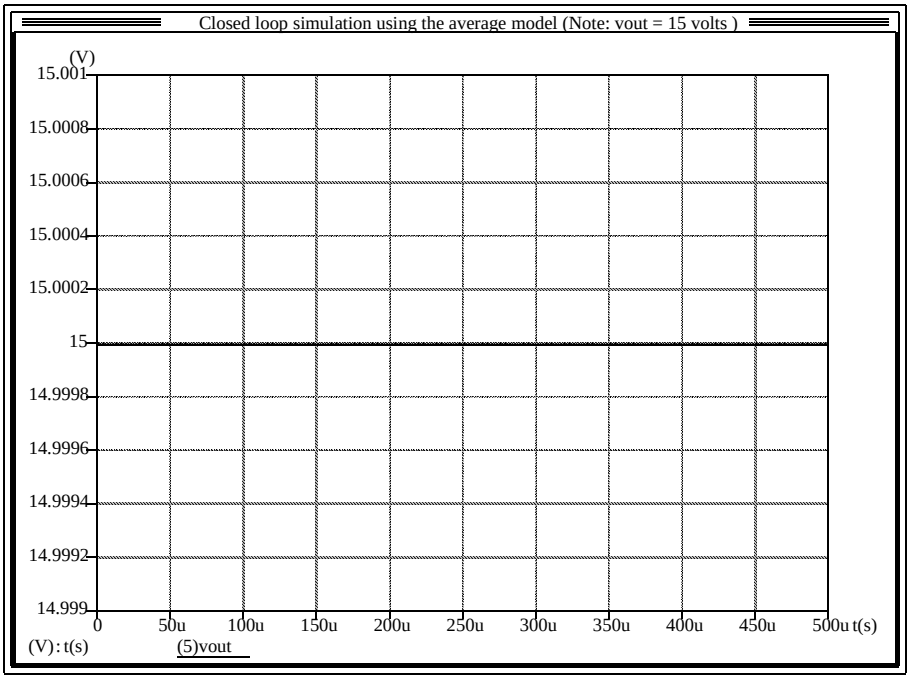


FIGURE 17 Output Voltage

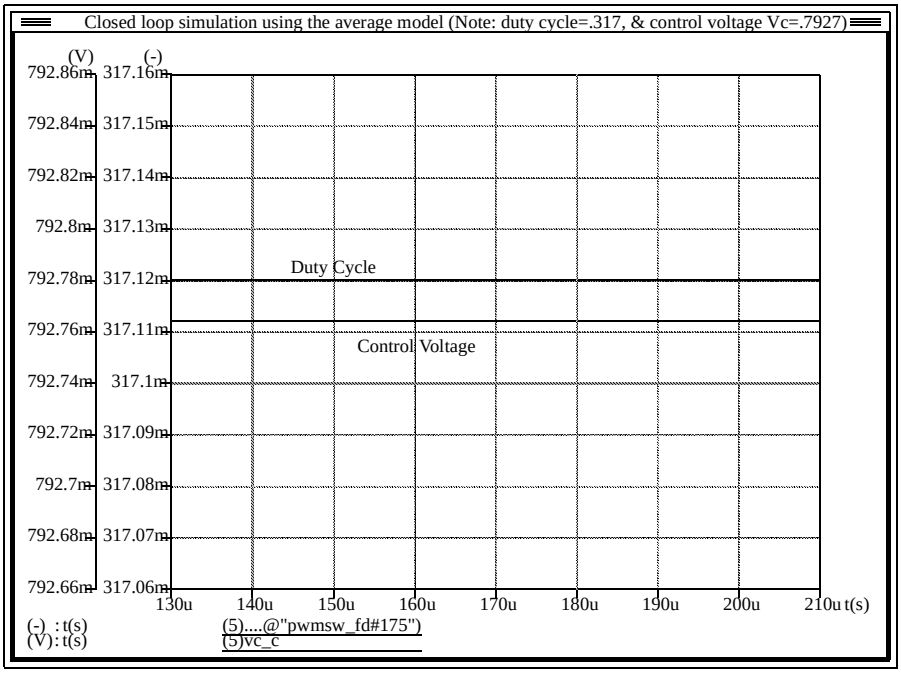


FIGURE 18 Duty Cycle and Control Voltage as solved by the system

3.3 Modulator Design and Closed Loop Simulation

The closed-loop circuit shown in Figure 19 is used for two simulations, an open-loop simulation to validate the modulation circuitry, and a complete closed-loop simulation to validate the overall design.

.

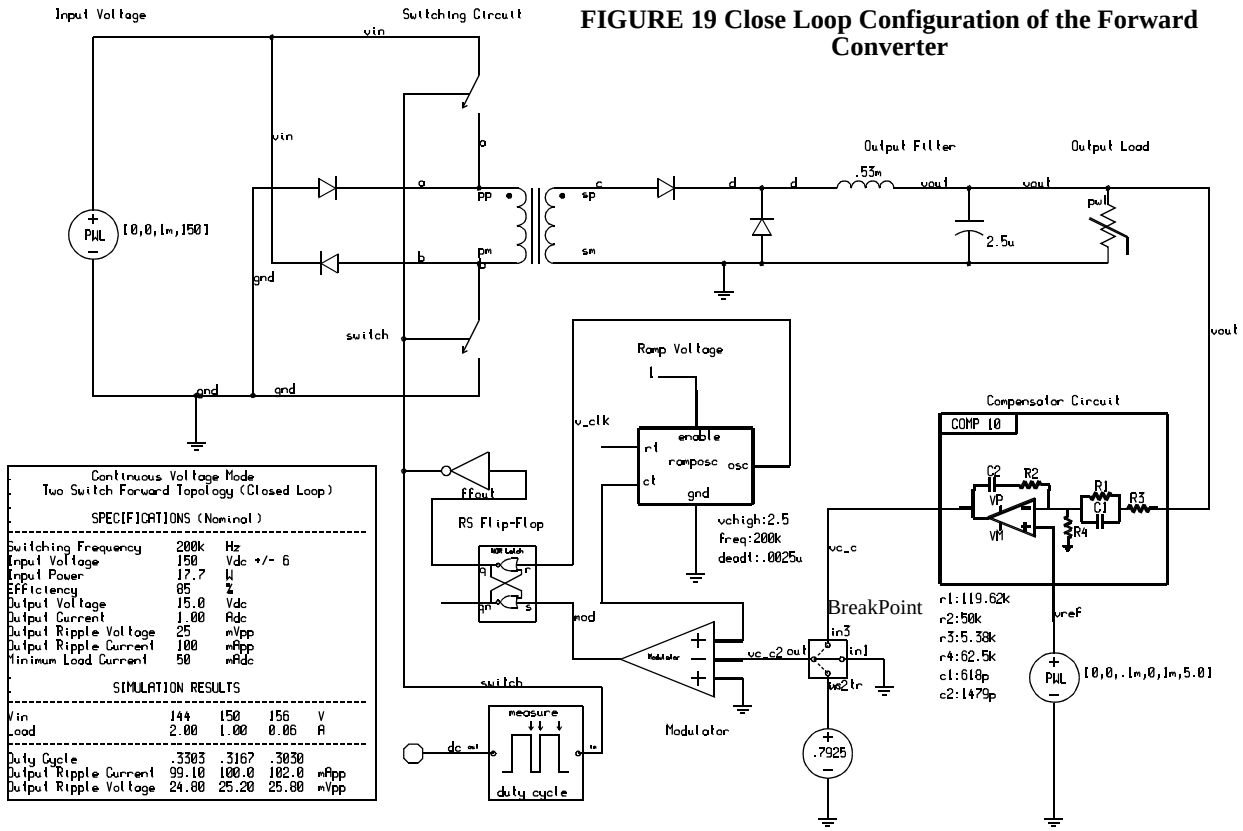


FIGURE 19 Close Loop Configuration of the Forward Converter

This configuration is used to design the modulation circuitry, and then validate the closed loop circuit (In the switching Mode - i.e. does not use the averaged model). You can now add other design elements such as snubbers, different switch technology with associated drive circuitry, soft start circuitry, or voltage and current limit circuits.

To design the modulation circuitry, the designer needs to look at the relationship of the duty cycle to the control voltage. Figure 20 shows that when the clock pulse goes high, the switch turns on, and when V_{ramp} crosses the control voltage (V_c), the switch turns off.

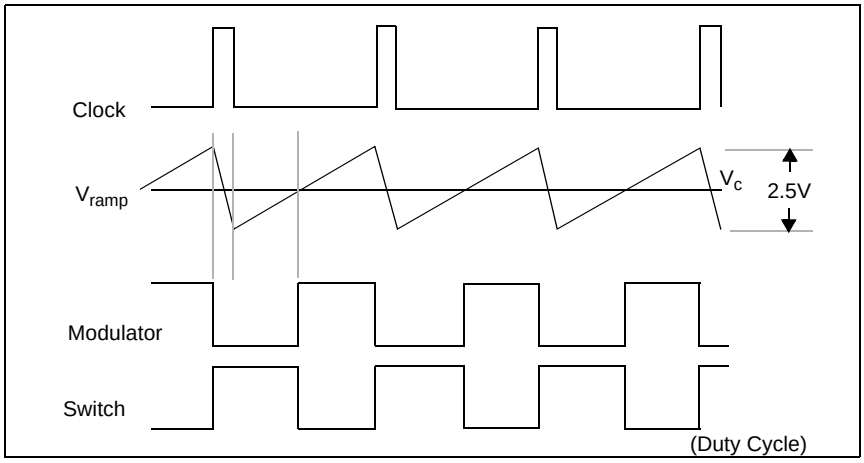


FIGURE 20 Modulation Circuit Waveforms

The duty cycle (D) is related to the control voltage (V_c) and the ramp (V_{ramp}) by the following equation:

$$D = \frac{V_c}{V_{ramp}}$$

D = 0.317 (including the diode drop)

Set $V_{ramp} = 2.5V$

$$V_c = 2.5V \times 0.317 = 0.7925V$$

3.3.1 Validate the Modulator Design using Saber

To validate the modulation circuitry, perform an open-loop simulation using the control voltage as input to the modulator. Note the breakpoint model used in Figure 19. This is the same model used in the averaged circuit which allows several types of simulations to be run from a single schematic. For the validation of the modulation circuitry, the breakpoint model opens the feedback loop and uses the control voltage as the input to the modulation circuit. The results of this simulation show the relationship of the output voltage with respect to the control voltage for a specific modulation circuit design. Figure 21 shows the results. Note that the control voltage (.7925) yields the correct output voltage and duty cycle.

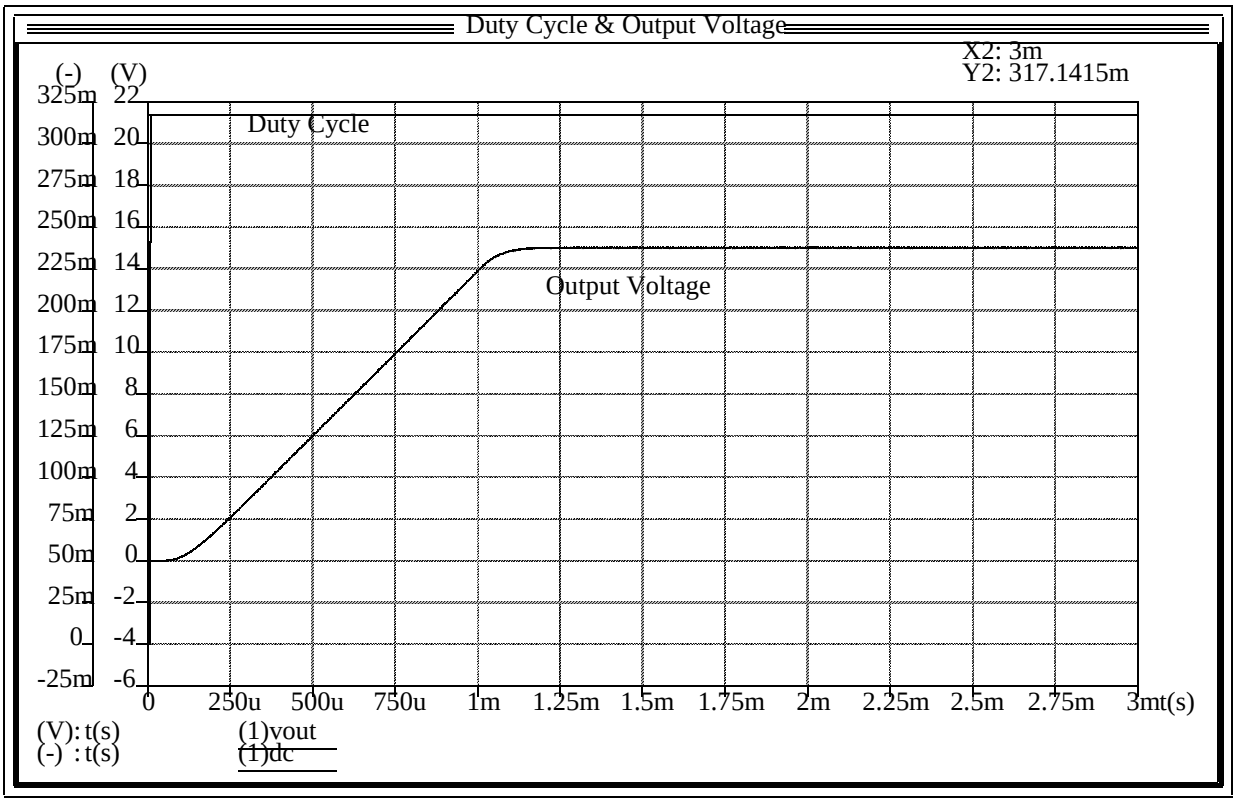


FIGURE 21 Validation of the Modulation Circuitry

Figure 22 shows the mixed digital and analog waveforms associated with the modulation circuit. Note that these waveforms are similar to those shown in Figure 20.

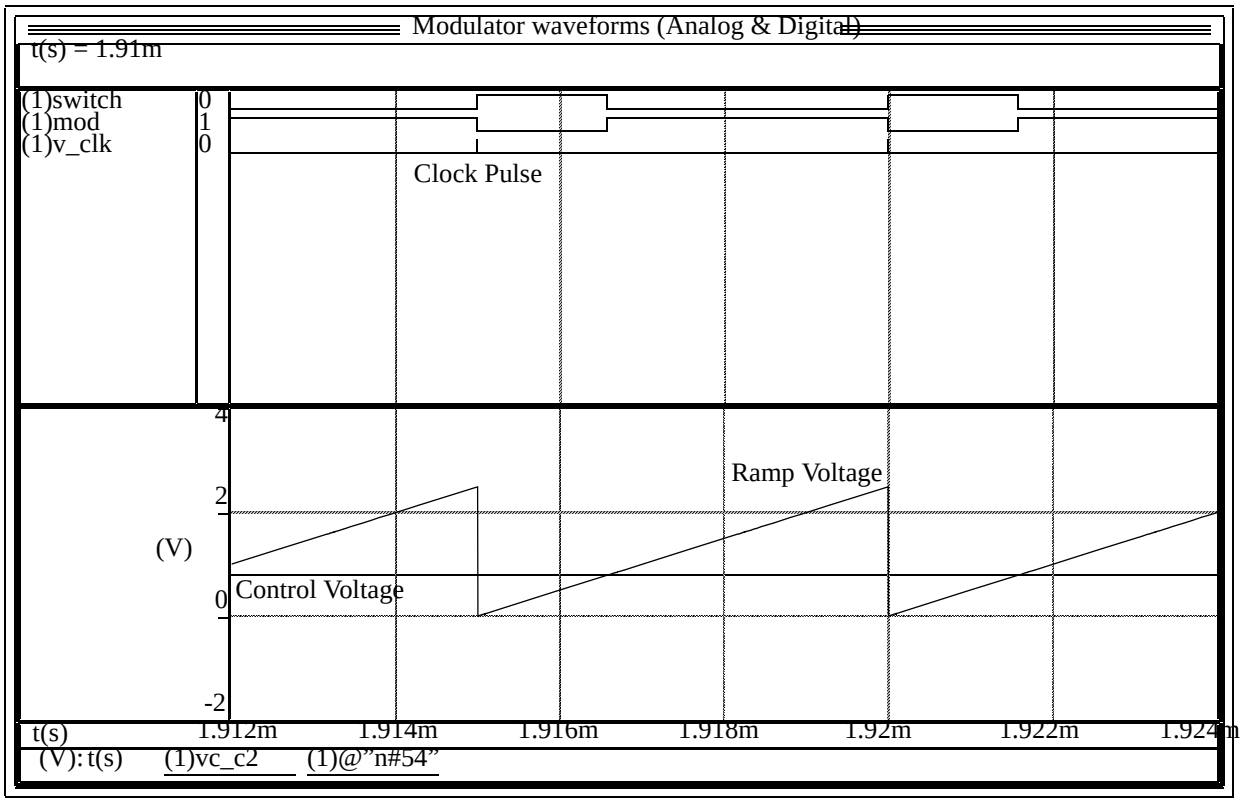


FIGURE 22 Mixed Digital and Analog Waveforms of the Modulator

3.3.2 Validate the Closed Loop Design using Saber

The last simulation described in this paper validates the closed loop response of the switching circuit. The breakpoint model is used to close the feedback loop and take the control voltage source out of the circuit. Figure 23 shows the output voltage and current as the power supply is ramped up.

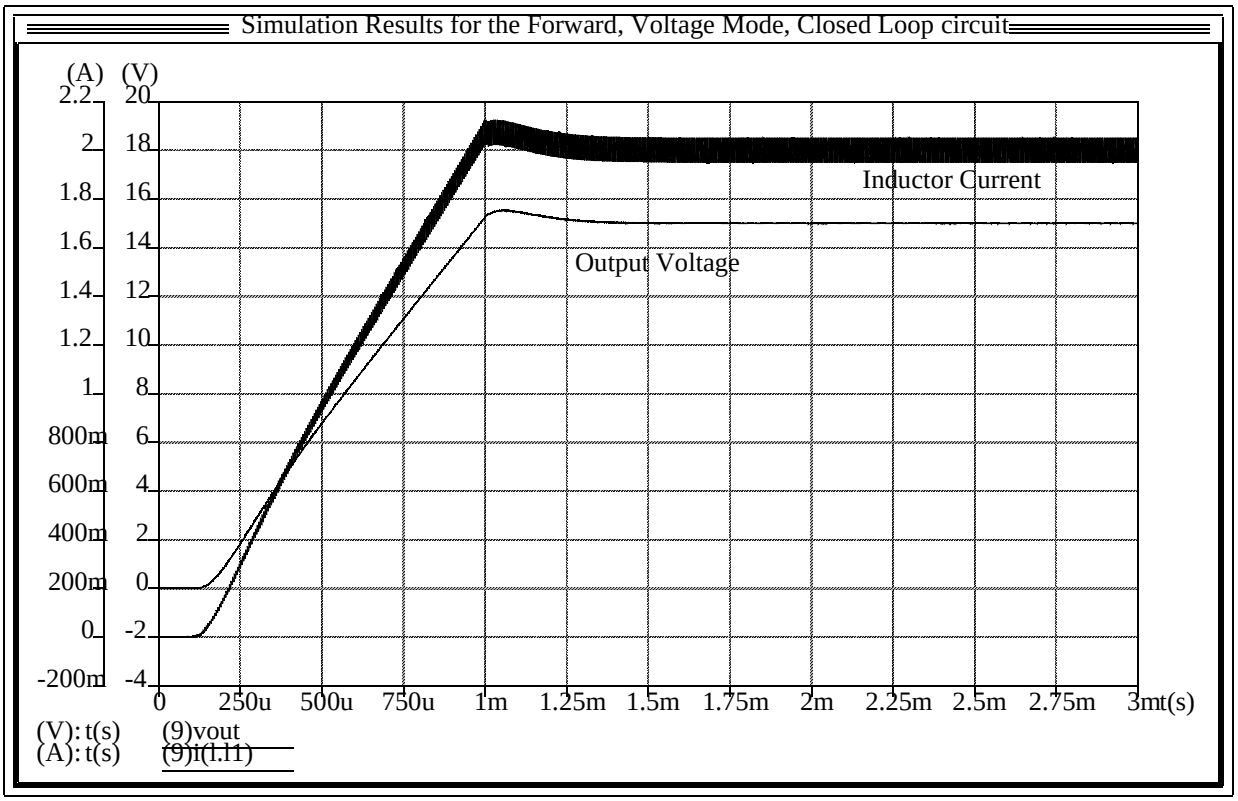


FIGURE 23 Closed Loop Simulation using the Switching Circuitry

Figure 24 shows the duty cycle measurement tool results. Note that the duty cycle settles out at approximately .317, which is the value calculated earlier.

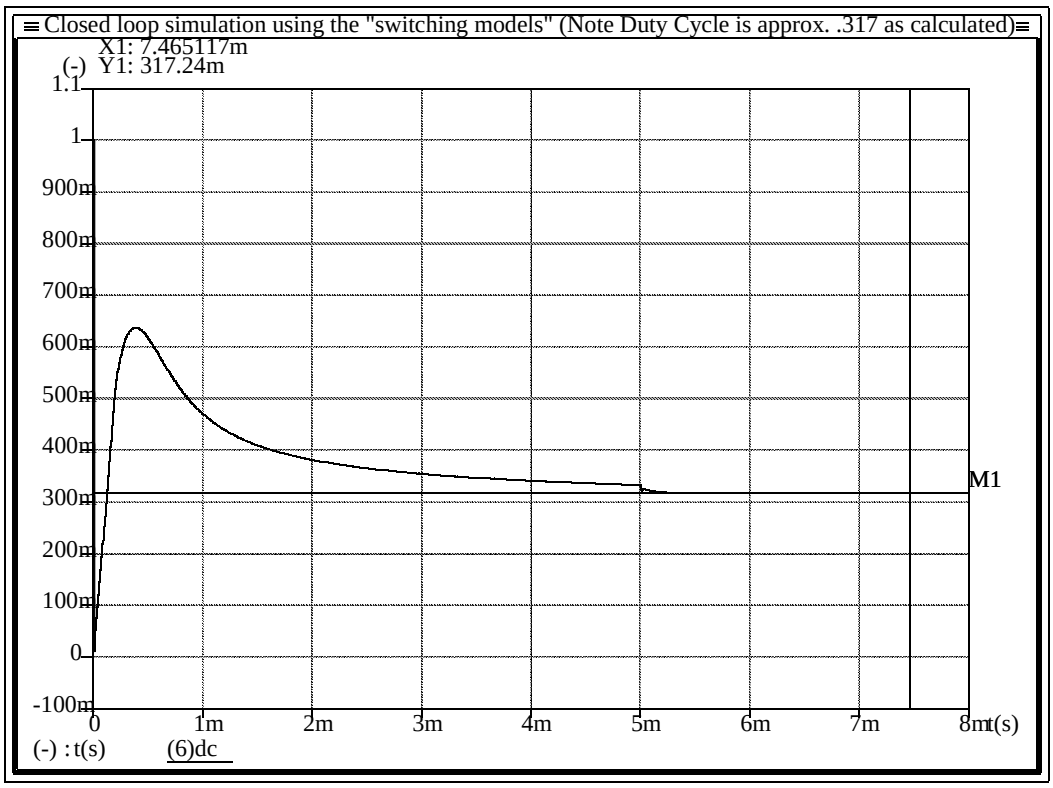


FIGURE 24 Duty cycle

Now that everything checks out, the basic design is complete. You can now add other design elements such as snubbers, different switch technology with associated drive circuitry, actual PWM IC models, soft start circuitry, or voltage and current limit circuits.

3.4 Final Component Level Design

Figure 25 shows the completed component level design of the two switch forward (Voltage Mode) converter:

* The 1825 PWM model was used in the voltage mode configuration to replace the modulation circuitry previously used.

* Additional snubber networks were added across the switching devices.

* The Ideal switch was replaced with the irf250 (200 volt) model

* A current transformer was added to drive the power MOSFETs for isolation and to drive both the low and high side switch.

* Drive circuitry was added to provide the capability of turning the power MOSFET devices on and off as required by the high switching frequency.

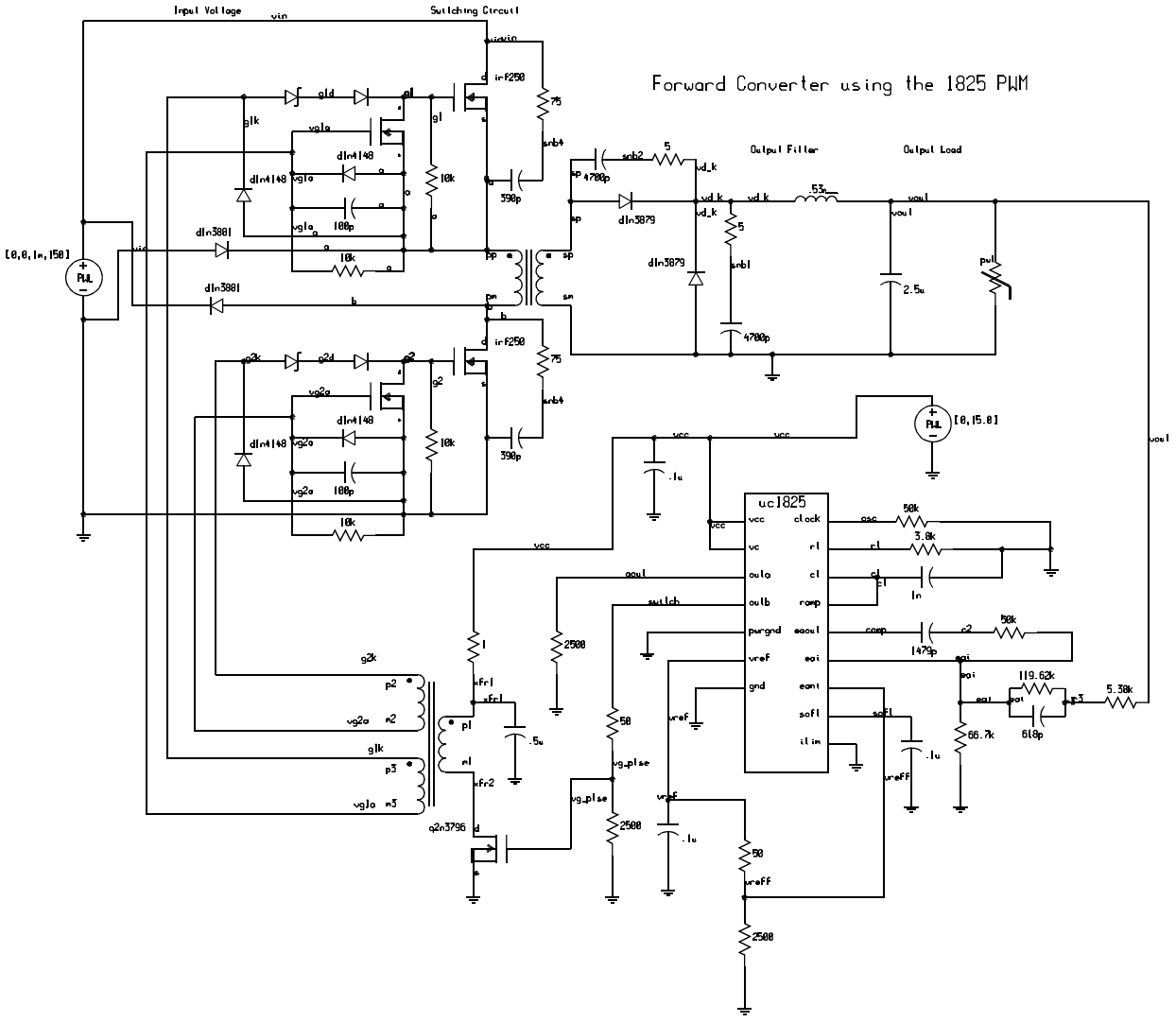


FIGURE 25 Component Level Design/Modeling of the Forward Converter

Figure 26 shows the waveforms at the inverting input “eai” and the output “comp” of the error amplifier (1825 PWM) as well as the ramp waveform produced at the “ct” pin of the 1825 PWM model. The ramp waveform at the “ct” pin is added to a 1.25 volt offset inside the 1825 PWM and then compared with the output of the error amplifier “comp” to determine the duty cycle.

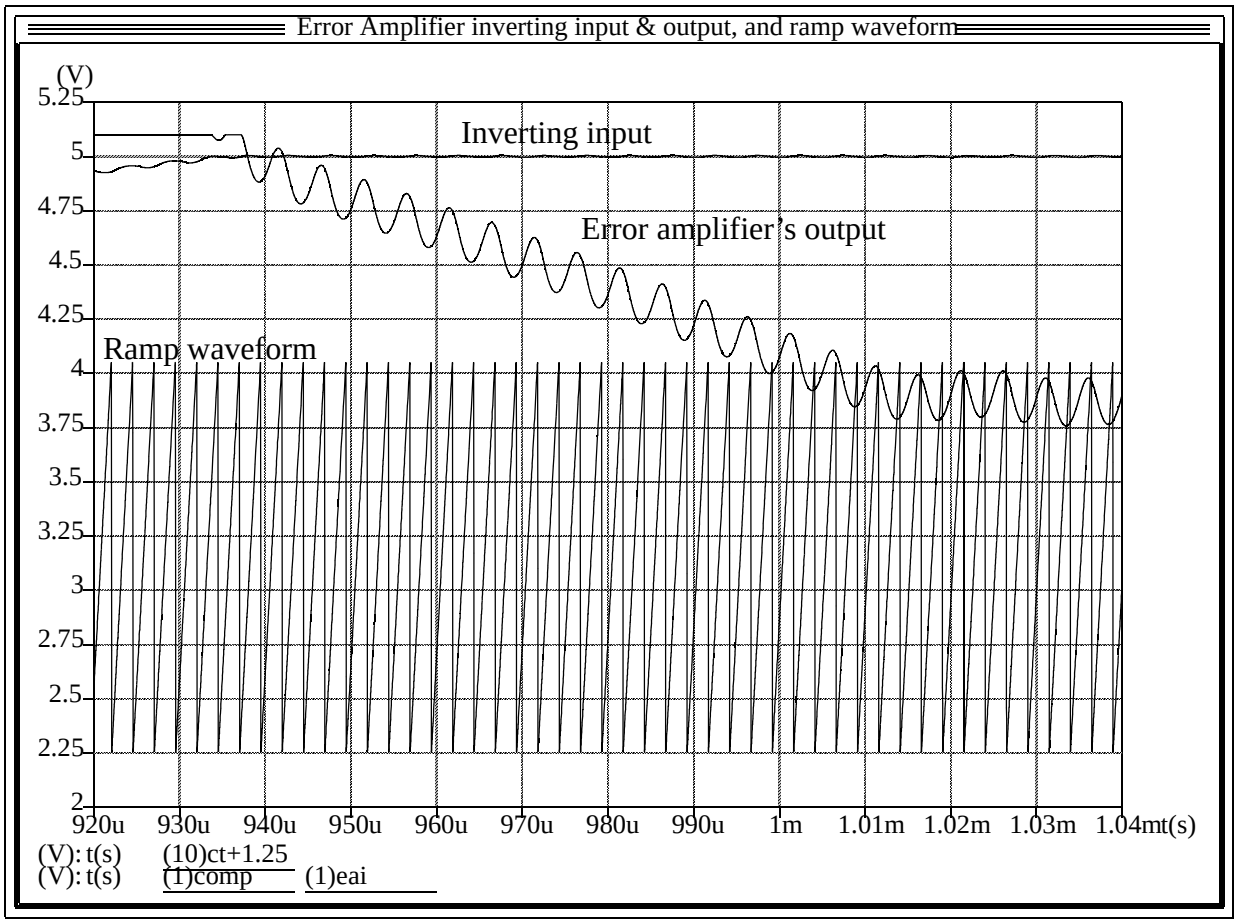


FIGURE 26 Error Amplifier’s inverting input & output, and ramp waveform from the 1825 PWM model

Note that the output of the error amplifier is at the positive rail (5.1 volts) until the inverting input ramps up to the reference voltage (5.0 volts). At this point the error amplifier’s output begins to slew negative until it crosses the ramp waveform, this now starts to reduce the duty cycle until a steady state condition is reached.

Figure 27 shows the output voltage and the current through the output filter Inductor. These waveforms are very similar to the waveforms seen in the previous closed loop simulations.

.

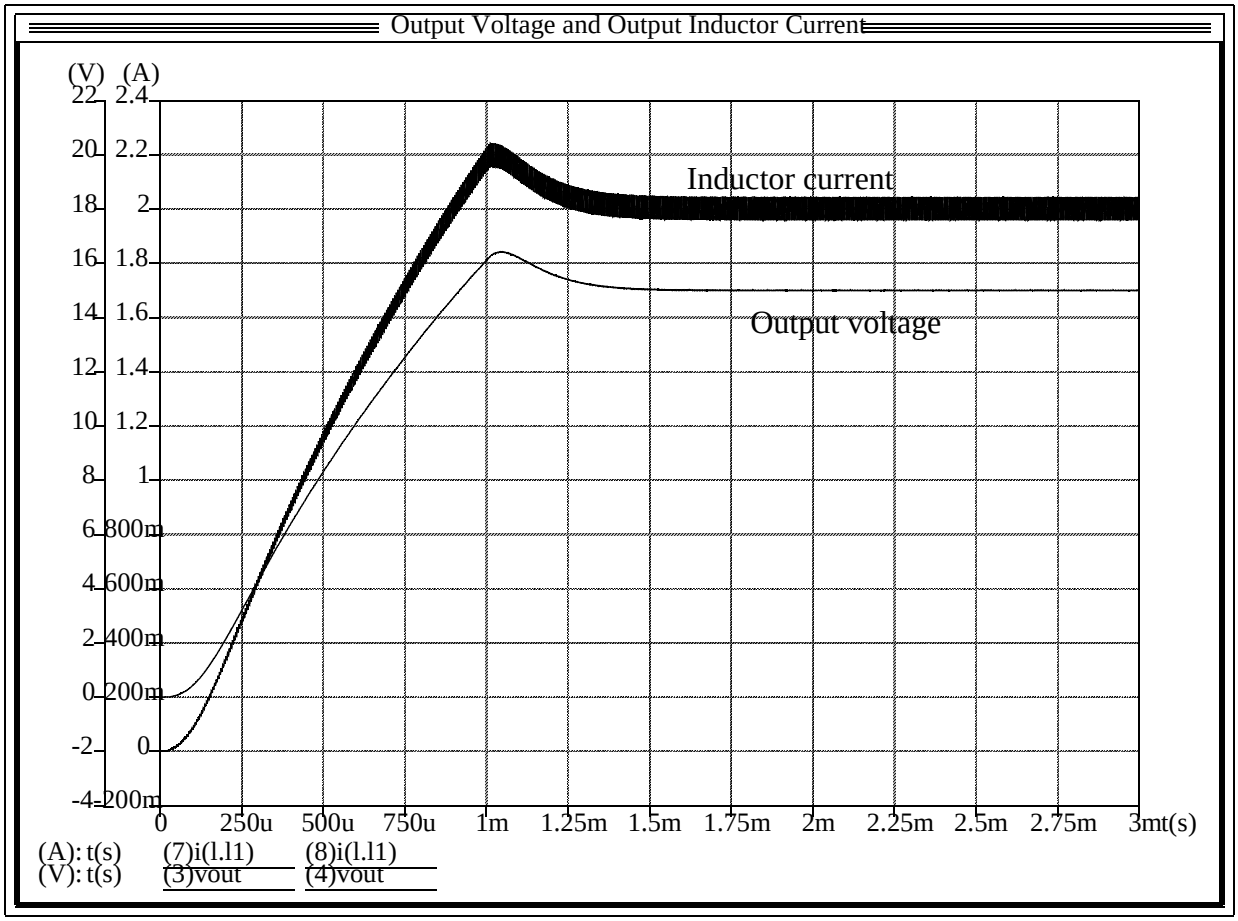


FIGURE 27 Output voltage and filer Inductor current waveforms

Note that the final component level simulation using the 1825 PWM model along with actual switching devices and associated drive circuitry yields very good results. The output voltage is at 15 volts with 25mV ripple and the Inductor current is at 2 amps with a 100mA ripple per the design specifications. The switching frequency is 200kHz.

Conclusion

The intention of this example was to educate the audience on the use of simulation in the design process of switched power converters. The software tool used to facilitate this process was the Saber simulator package. A step by step design and validation process was described.

Simulation can provide a tremendous advantage in the design process. However, it should be used intelligently and methodically to yield the greatest return on the investment of time and money.

References

[1] Brown, M., Practical Switching Power Supply Design, Academic Press, 1990

[2] Unitrode Switching Regulated Power Supply Design Seminar Manual, Unitrode Corporation, Lexington, MA