AN628
APPLICATION NOTE

DESIGNING A HIGH POWER FACTOR SWITCHING PREREGULATOR WITH THE L4981 CONTINUOUS MODE

by Ugo Moriconi

INTRODUCTION

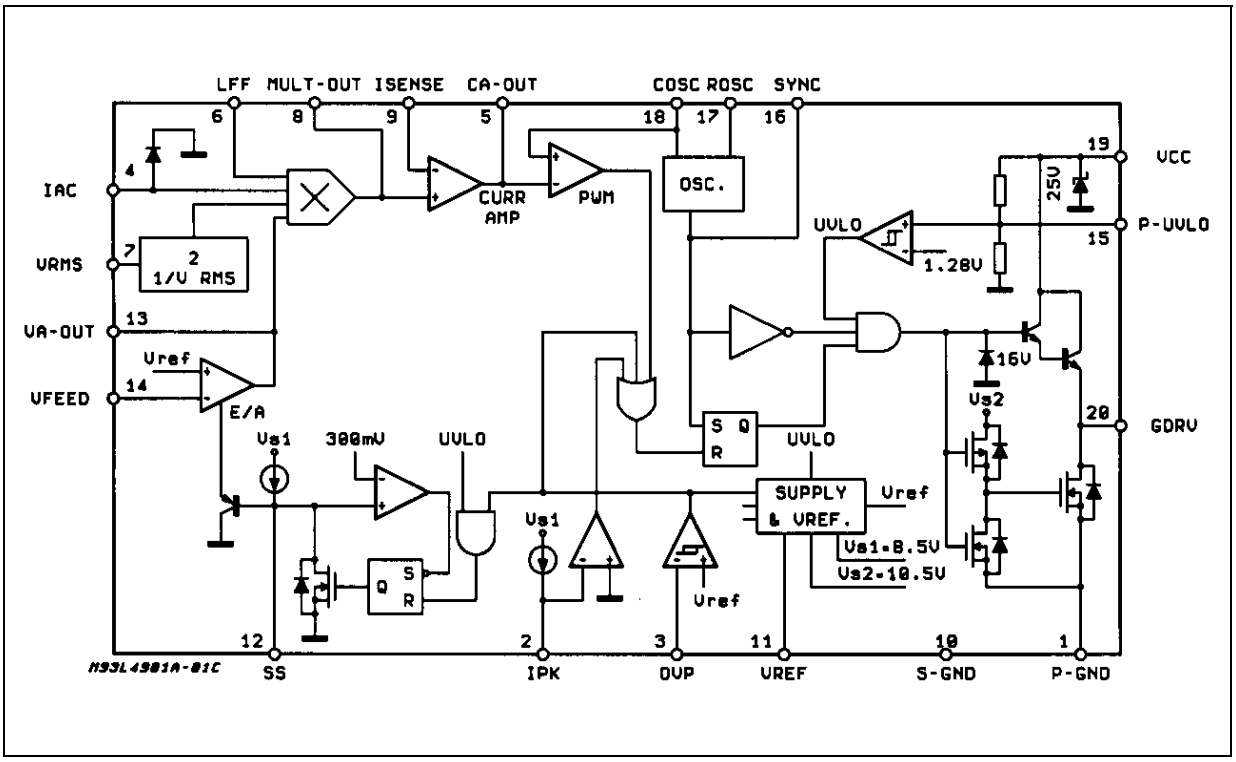
Conventional AC-DC converters usually employ a full wave rectifier bridge with a simple capacitor filter to draw power from the AC line. This "bulk" capacitor must be big enough to supply the total power during most of each half-cycle, while instantaneous line voltage is below the DC rectified voltage. Consequently, the line current waveform is a narrow pulse, and the power factor is poor (0.5-0.6) due to the high harmonic distortion of the current waveform.

If a high power factor switching preregulator is interposed between the input rectifier bridge and the bulk filter capacitor, the power factor will be improved (up to 0.99). Increasing in addition, the RMS current capability from the mains, reducing the bulk capacitor peak current and the harmonic disturbances.

Switching at a frequency much higher than the line's one, the preregulator draws a sinusoidal input current, in phase with the input line voltage.

There are several way that this can be accomplished. When the output voltage is higher than the input voltage (Vo > Vin), BOOST topology and continuos inductor current control mode are well suited to produce a good quality input sine current waveform. The input di/dt is low because the inductor is located between the bridge and the switch. This minimizes line noise and the line spikes will be absorbed by the inductor.

Figure 1. L4981 Block Diagram



THE L4981 PFC CONTROLLER IC

The L4981 integrated circuit is a continous mode average current controller with several specific functions for active power factor correction. It can operate in high quality, medium/high power conversion range and provides all the necessary features to achieve a very high power factor, up to 0.99. Thanks to the BCD technology used, operative switching frequency higher than 200kHz can be used.

The L4981 can be used in systems with universal input mains voltage without any line switch.

This new PFC offers the alternative of synchronization working at fixed frequency (L4981A), or working in modulated frequency (L4981B) to optimize the size of the input filter. Both devices control the conversion in average current mode PWM to maintain a sinusoidal line current without slope compensation.

MAIN FEATURES:

- Switching frequency higher than 200 kHz.
- Under Voltage Lockout with hysteresis and programmable turn-on threshold.
- Overvoltage and Overcurrent Protection.
- Precise (2%) on chip Reference externally available.
- Input/Output Synchronization (only for L4981A).
- Feed Forward Line and Load regulation.
- Universal input mains.
- Average current mode PWM.
- High Output Current totem pole driver.
- Low Start-up supply current.
- Soft Start.

P.F.C. BOOST TOPOLOGY OPERATION

The operation of the P.F.C. boost converter (see fig. 2) can be summarized in the following description.

The A.C. line voltage is rectified by a diode bridge and the rectified voltage delivered to the boost converter. The boost converter section, using a PWM switching technique, boosts the rectified input voltage to a D.C. controlled output voltage (V_O). The section consists of a boost inductor (L), a controlled power switch (Q), a boost diode (D), an output capacitor (CO) and, obviously, a control circuitry.

Referring to the time-variable mains voltage (sine waveform), the converter produces a boost inductor average current like the rectified input voltage, changing continuosly the duty-cycle of the active switch (Q).

The boosted D.C. voltage is controlled to a programmed value, higher than the maximum input instantaneous voltage (V_{Ipk}).

Referring to the main currents shown in fig.2 schematic, the simplified formulae are (assuming: power efficiency = 1; output ripple voltage = 0; high frequency inductor ripple current = 0):

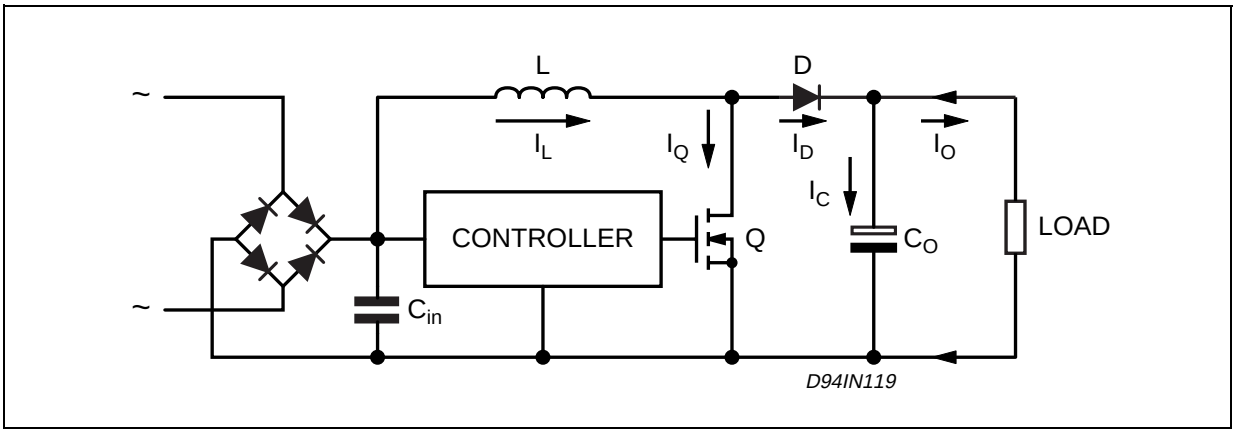
1) Peak inductor (L), switch (Q) and diode (D) currents

$$I_{Lpk} = I_{Qpk} = I_{Dpk} = 2 \cdot \frac{P_O}{V_{Ipk}}$$

2) RMS inductor current

$$I_{Lrms} = \sqrt{2} \cdot \frac{P_O}{V_{Ipk}}$$

Figure 2.



3) RMS switch current

$$I_{Qrms} = \frac{P_O}{V_{Ipk}} \cdot \sqrt{2 - \frac{16 \cdot V_{Ipk}}{3 \cdot \pi \cdot V_O}}$$

4) Average diode current

$$I_{Davg} = I_O$$

5) RMS diode current

$$I_{Drms} = \frac{P_O}{V_{Ipk}} \cdot \sqrt{\frac{16 \cdot V_{Ipk}}{3 \cdot \pi \cdot V_O}}$$

6) Total RMS capacitor (CO) current

$$I_C = I_O \sqrt{\frac{16 \cdot V_O}{3 \cdot \pi \cdot V_O} - 1}$$

7) RMS twice line frequency capacitor current

$$I_{C(2f)rms} = \frac{I_O}{\sqrt{2}}$$

8) RMS high frequency capacitor current

$$I_{C(hf)rms} = I_O \sqrt{\frac{16 \cdot V_O}{3 \cdot \pi \cdot V_{Ipk}} - 1.5}$$

The figure 3 shows the above mentioned quantities, normalized to the D.C. output current (I_O), plotted versus V_{Ipk} / V_O ratio. Moreover, the $I_{Lpk} \cdot I_{Lrms}$ normalized to I_O^2 value, related to the inductor energy ($I^2 \cdot L$), is plotted in the diagram (dotted line). This last plot gives an idea on the heavy increase of the inductor size operating with large input voltage range.

Obviously, in real application the efficiency is less than 100% ($\eta < 1$). The output voltage ripple, related to the output capacitor (C_O) is a parameter to be considered. The inductor high frequency current ripple (ΔI_L) is another parameter affected by the inductor value (L), the switching frequency (f_{sw}) and the delivered power (P_O).

Figure 3.

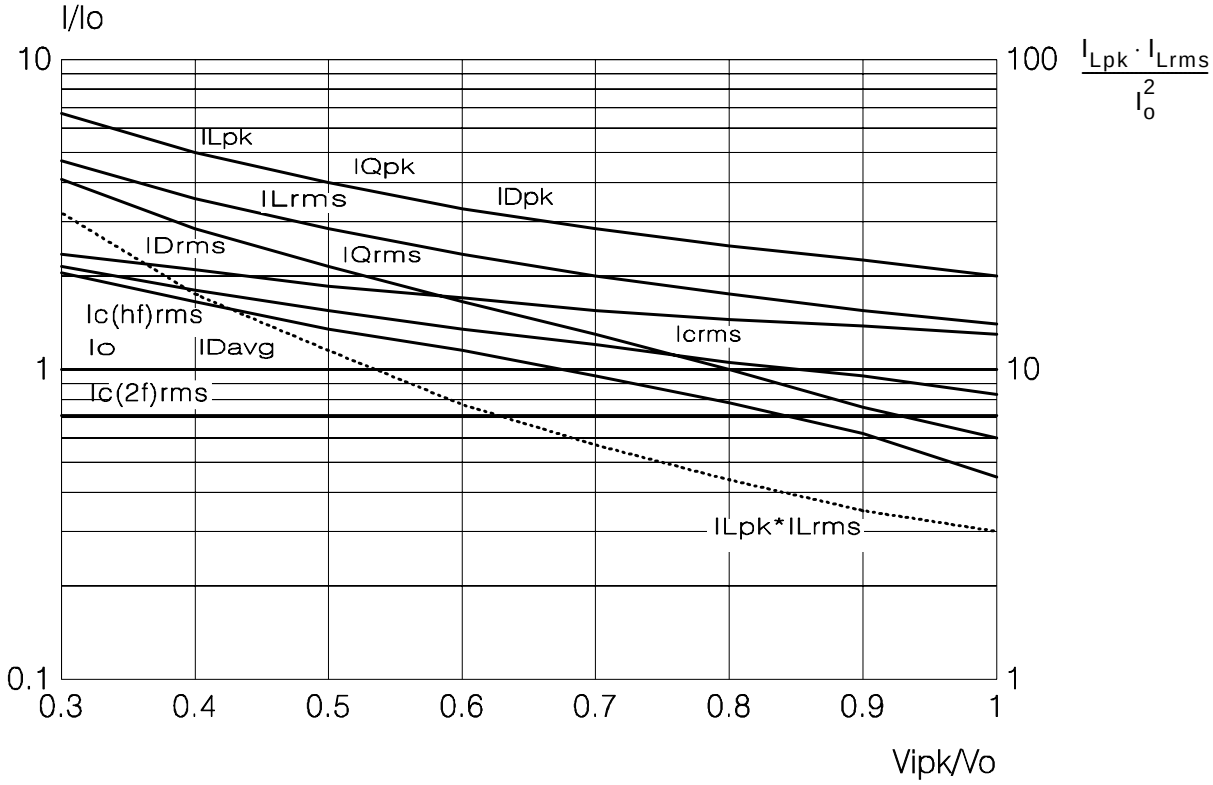
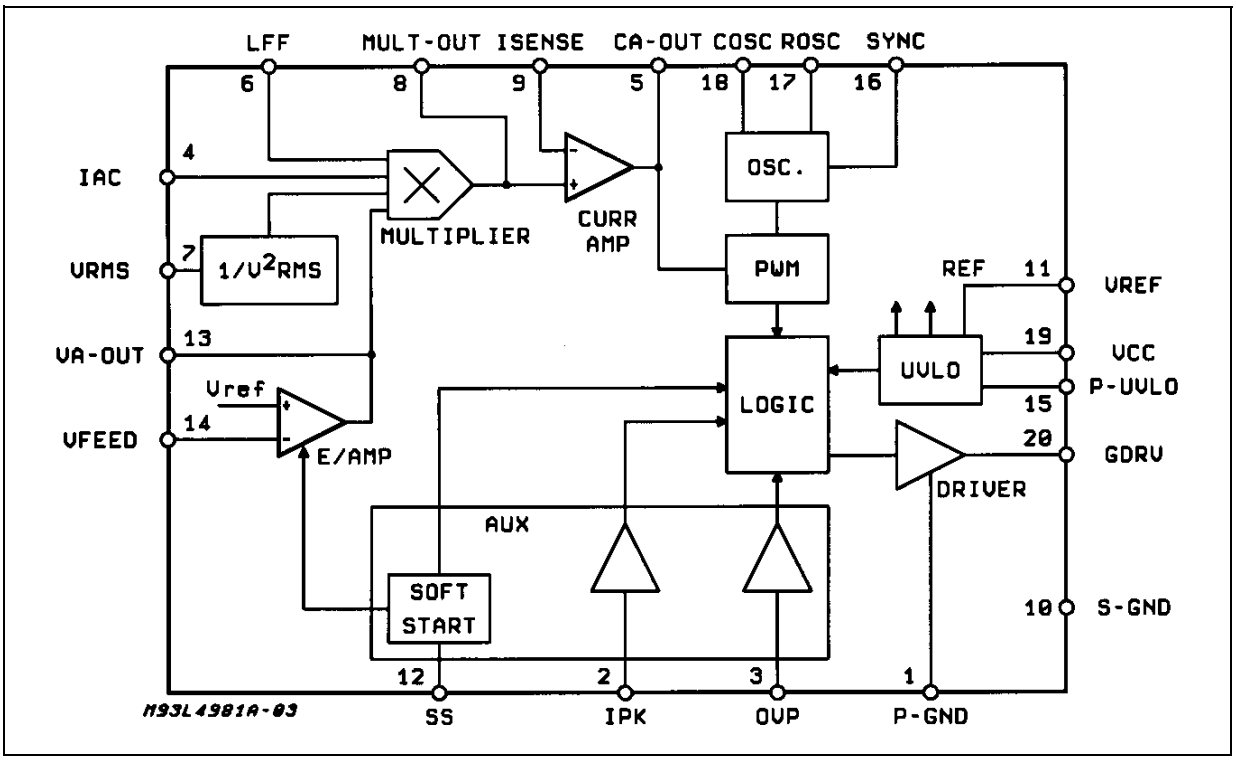


Figure 4.



CONTROLLER FUNCTION DESCRIPTION.

The L4981 I.C. controls the conversion process with a continuous mode average current method, using two control loops (current loop and voltage loop) see fig. 5. Moreover, several internal functions ensure high quality conversion performance.

A description of the internal blocks will be detailed in the design criteria section and pin description. However, referring to fig. 4, here below a brief description of the main functions is done:

Multiplier block.

This block produces an output current (programming current) as a product result of four different input signals (see fig. 13 for details). The multiplier output current, through a resistor connected to the negative side of a sense resistor, determines the error signal to the current loop.

Figure 5.

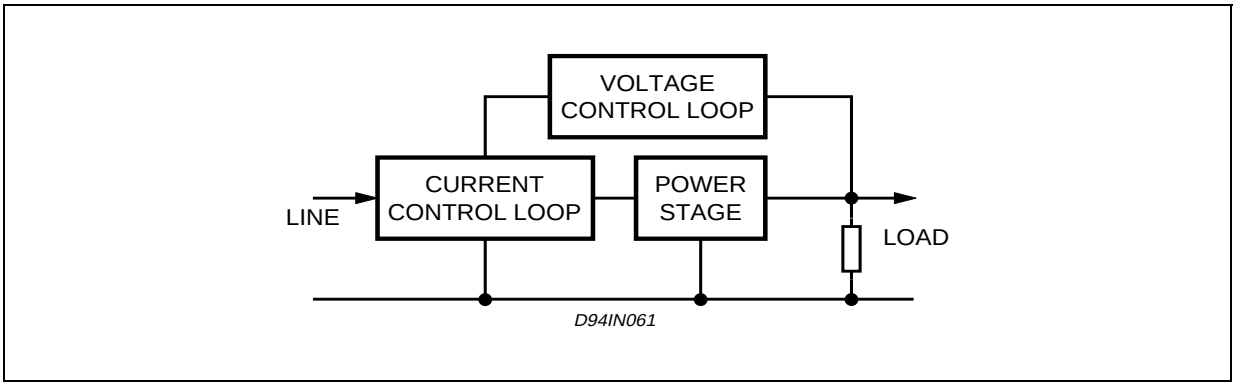
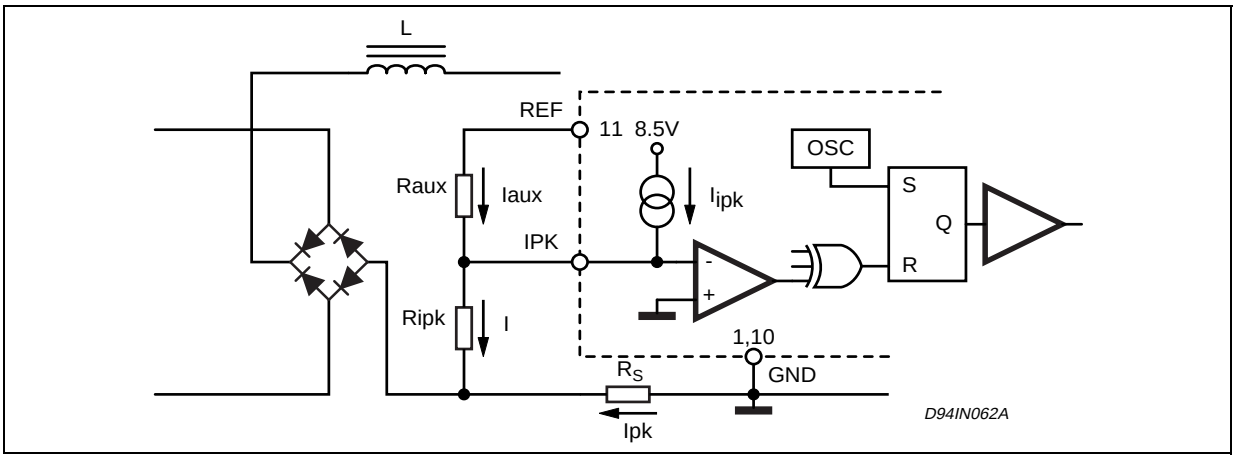


Figure 6.



Operational amplifier blocks.

Two amplifiers allow loop control. The first one (E/A), feeds back the output voltage (V_O) and delivers its output to the multiplier block. The second (C/A), feeds back the line current and produces the reference for the PWM section.

PWM block.

This block, comparing the sawtooth produced by the oscillator, with the reference signal from the C/A output, modulates its output signal duty-cycle. Its output, by the logic and driver sections, allows the controlled switch (Q) to modulate the inductor current.

Logic block.

Controls the flow from the PWM and the output with the Auxiliary function signals and soft start.

Driver block.

The driver supplies the gate current to turn on and off the power switch (Q). It delivers up to 1A peak current to allow high switching frequency applications.

Aux functions.

The Auxiliary functions allow to avoid overstress on power components of the application.

Power supply block.

This circuitry delivers the internal supply and references, recognizes the Undervoltage and Stand-by conditions to save consumption.

P.F.C. BOOST DESIGN CRITERIA

L4981 PIN DESCRIPTION AND BIASING CIRCUITRY.

Pin 1. P-GND (Power stage ground). This pin, on the pc-board, has to be connected close the external Mosfet source.

Pin 2. I_{PK} (Overcurrent protection input). The current limitation is obtained with an internal comparator that holds down the output driver when the voltage at IPK input goes down to zero. In the L4981A, to preset the IPK input there is an internal current source (I_{ipk}) of typically 85µA. The maximum peak current (I_{pk}) can be programmed connecting (see fig. 6) a single resistor (R_{ipk}) between this pin and the sense resistor (R_S):

$$R_{ipk} = \frac{R_S \cdot I_{pk}}{I_{ipk}}$$

In the L4981B, to preset the IPK input, an auxiliary resistor (R_{aux}), connected from the VREF pin to the I_{PK} pin, is required. The maximum peak current (I_{pk}) can be programmed choosing (see fig. 6) the resistances R_{aux} and R_{ipk}:

$$R_{ipk} = \frac{R_S \cdot I_{pk}}{I_{aux}}$$

Where:

$$I_{aux} = \frac{V_{VREF}}{R_{aux}}$$

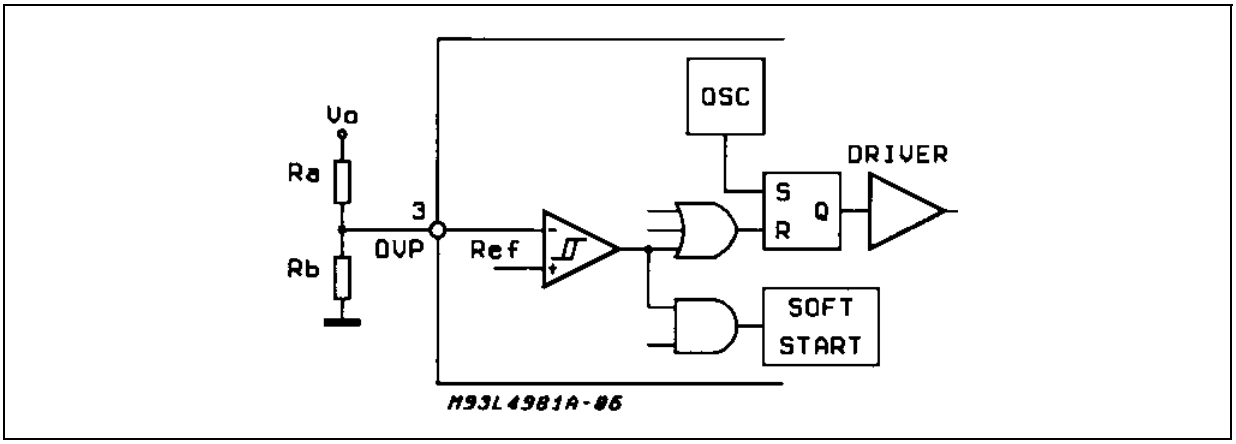
Note: If used with the L4981A, the auxiliary resistor avoids that the current source spread affects the precision of the protection simply getting an auxiliary current (I_{aux}) much higher than I_{ipk}.

Pin 3. OVP (Overvoltage protection input). A comparator with a precise 5.1V reference voltage and 250mV of hysteresis, detects the overvoltage condition and turns the controller in stand-by condition (with low power consumption) and discharges the soft start capacitor. This pin (see fig. 7) has to be externally connected with a resistive divider (Ra and Rb) to the D.C. output voltage. The divider ratio is defined by the relation:

$$\frac{Ra}{Rb} = \frac{V_O + \Delta V_{OUT}}{5.1V} - 1$$

where: ΔV_{OUT} is the output overvoltage limit.

Figure 7.

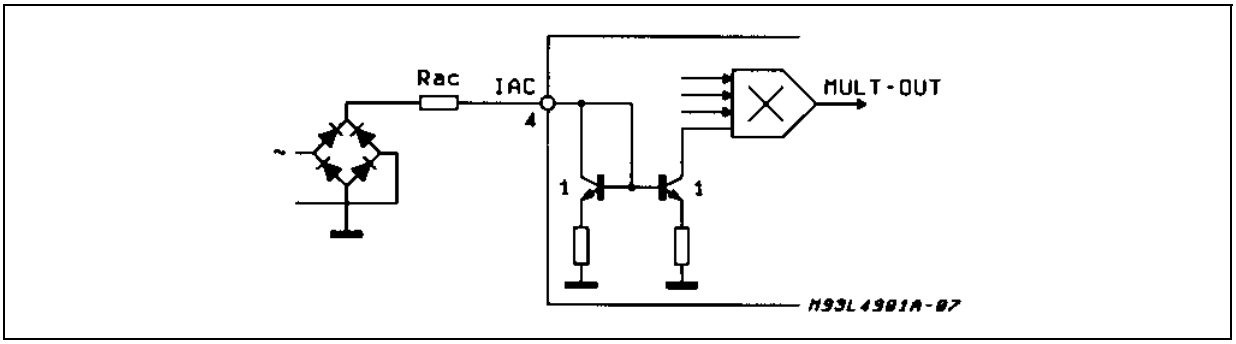


Pin 4. IAC (A.C. current input). This pin (see fig. 8) has to be connected through a resistor to the rectified line voltage to drive the multiplier with a current (I_{IAC}) proportional to the instantaneous line voltage:

$$I_{IAC} = \frac{V_I}{R_{ac}}$$

The relation between the input alternate current (I_{IAC}) and the output current (programming signal Imult) of the multiplier is described at MULT-OUT section (pin8).

Figure 8.



Pin 5.CA-OUT (Current amplifier output). The CA_OUT deliveres its signal to the PWM comparator. An external network (see fig. 9) defines the suitable loop gain to process the multiplier output and the line current signals. To avoid oscillation problem (see fig. 10) the maximum inductor current downslope (VO/L) has to be lower than oscillator ramp-slope ($V_{srp} \cdot f_{sw}$):

$$\frac{V_O}{L} \cdot R_s \cdot G_{ca} \leq V_{srp} \cdot f_{sw}$$

where:

V_{srp} is the oscillator ramp peak-peak voltage.
G_{ca} is the current amplifier gain.
f_{sw} is the switching frequency.

and rewritten as:

$$G_{ca} \leq \frac{V_{srp} \cdot f_{sw} \cdot L}{V_O \cdot R_s}$$

Figure 9.

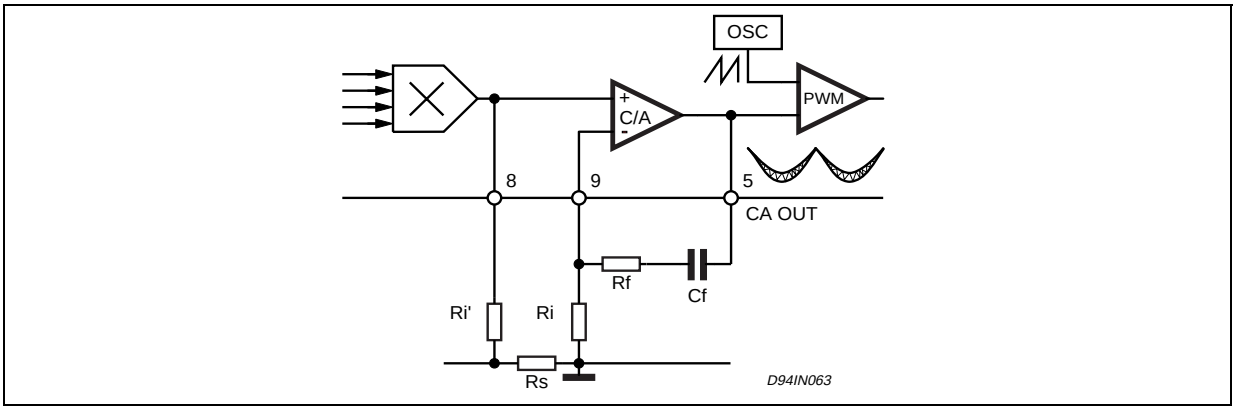
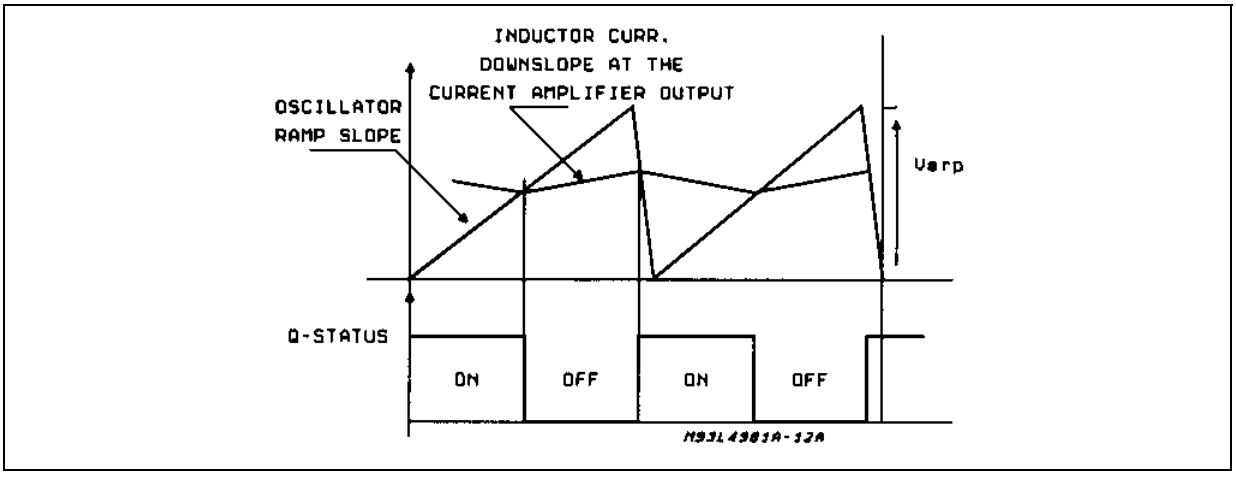


Figure 10.



defines the high frequency C/A gain $(1 + \frac{R_f}{R_i})$:

$$\frac{R_f}{R_i} \leq \frac{V_{srp} \cdot f_{sw} \cdot L}{V_O \cdot R_S} - 1$$

To define the Cf value, it's useful to consider the current openloop gain, defined by the ratio between the voltage across Rs and the current amplifier output signal:

$$G_{avg} = \frac{v_{rs}}{v_{ca}}$$

Because, in worst condition is:

$$v_{rs} = \frac{R_s \cdot V_O}{s \cdot L}$$

and the total variation of v_{ca} (the reference signal for PWM) is V_{srp}:

$$G_{avg} = \frac{R_s \cdot V_O}{V_{srp} \cdot 2\pi \cdot f \cdot L}$$

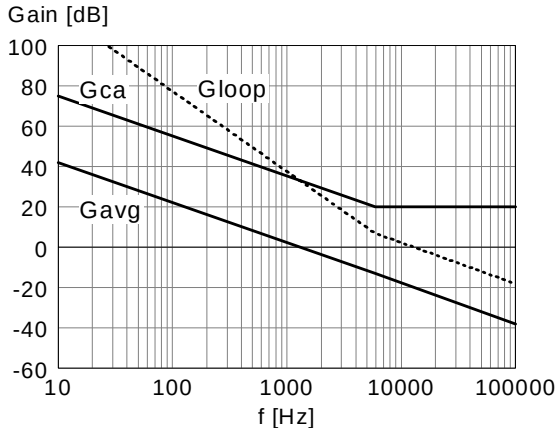
Multiplying this G_{avg} by G_{ca} and solving for the crossover frequency ($f = f_c$), follows:

$$f_c = \frac{f_{sw}}{2\pi}$$

To ensure a phase margin (higher than 45°), the zero frequency (f_z) should be about $\frac{f_c}{2}$, than:

$$f_z = \frac{f_{sw}}{4 \cdot \pi} = \frac{1}{2 \cdot \pi \cdot C_f \cdot R_f} \Rightarrow C_f = \frac{2}{R_f \cdot f_{sw}}$$

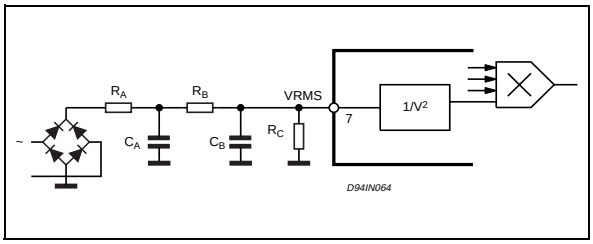
Figure 11.



Pin 6. LFF (Load feed-forward input). This voltage input pin allows to modify the multiplier output current proportionally to the load in order to improve the response time versus load transient. The control is working with V_{LFF} between 1.5V and 5.1V. If this function is not used, the LFF pin has to be connected to VREF pin.See also appendix A.

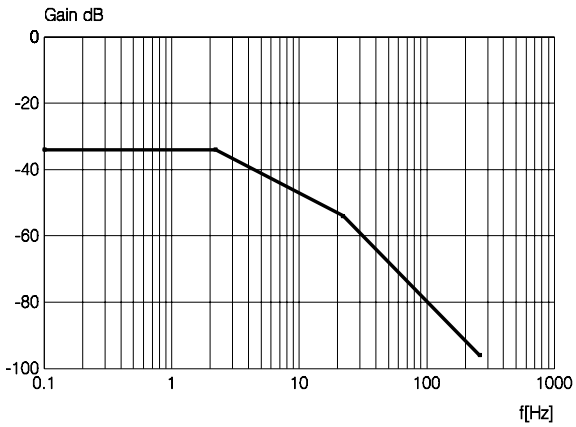
Pin 7. VRMS. Input to the divider ($1/V^2_{RMS}$), it is especially useful in universal mains applications to compensate the gain variation related to the input voltage change. It will be connected to an external network (see fig. 12a) giving a voltage level proportional to the mains V_{RMS}. The best control is reached using a V_{RMS} voltage level in the range between 1.5V and 5.5V.

Figure 12a.



To avoid line current distorsion, the rectified mains ripple (2f) level has to be reduced. A two pole filter, with three resistors and two capacitors, setting the lowest pole at 2Hz and the highest one at 13Hz, is enough to get the useful voltage level reducing to -80dB the 100Hz gain.

Figure 12b.



The signal (pin 7), with the network in fig. 12a is:

V_{RMS} = 85V (110V -20%)	VRM(7) = 1.6V
V_{RMS} = 260V (220V +20%)	VRM(7) = 5V
Gain at 2f(100Hz)	-80dB

Pin 8. MULT-OUT (Output of the multiplier). This pin deliveres the programming current (Imult) according to the relation:

$$I_{mult} = 0.37 \cdot I_{IAC} \cdot \frac{(V_{va-out} - 1.28V) \cdot (0.8 \cdot V_{LFF} - 1.28V)}{V_{RMS}^2}$$

where: $V_{VA\text{-}OUT}$ = E/A output voltage range

V_{LFF} = voltage input at pin 6

V_{RMS} = voltage input at pin 7

I_{IAC} = input current at pin 4

To optimize the multiplier biasing for each application, the relation between Imult and the other input signals to the multiplier are here reported (refer to figure 13 and see figures 13a to 13h).

Figure 13.

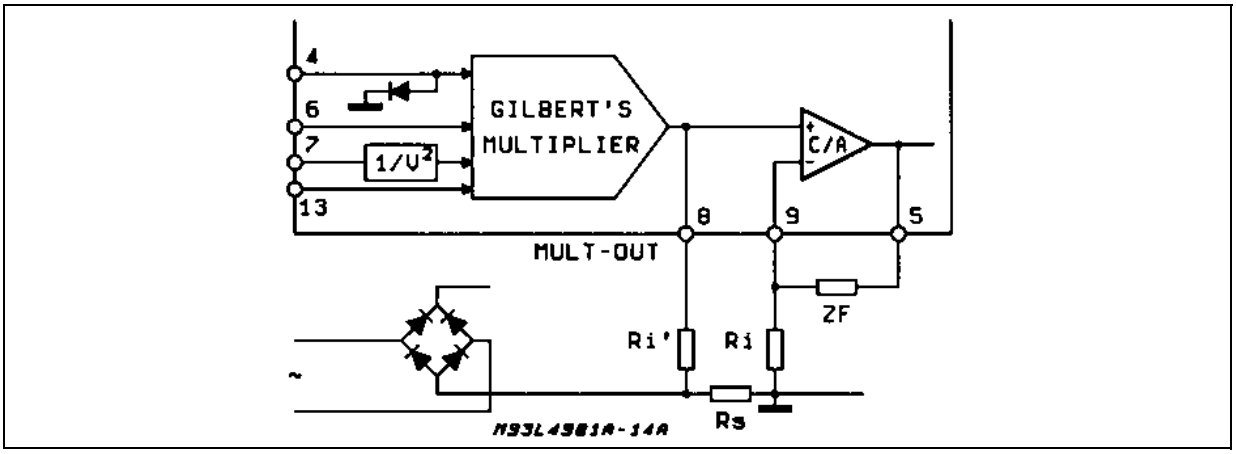


Figure 13a. MULTI-OUT vs. I_{AC} (V_{RMS} = 1.7V; V_{LFF} = 5.1V)

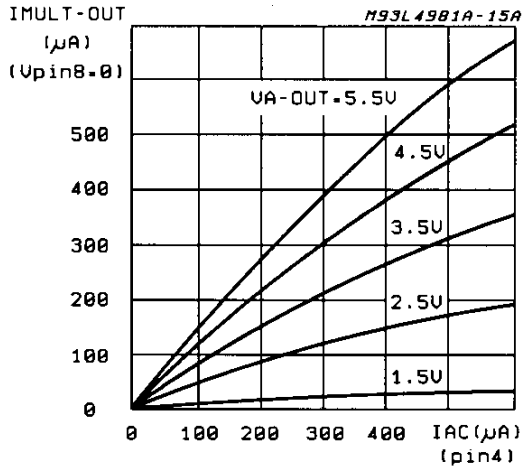


Figure 13b. MULTI-OUT vs. I_{AC} (V_{RMS} = 2.2V; V_{LFF} = 5.1V)

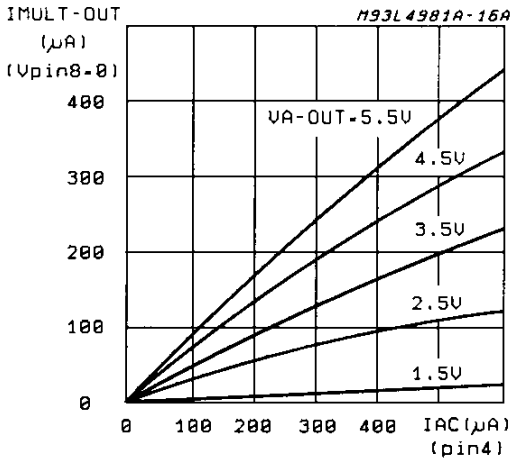


Figure 13c. MULTI-OUT vs. I_{AC} (V_{RMS} = 4.4V; V_{LFF} = 5.1V)

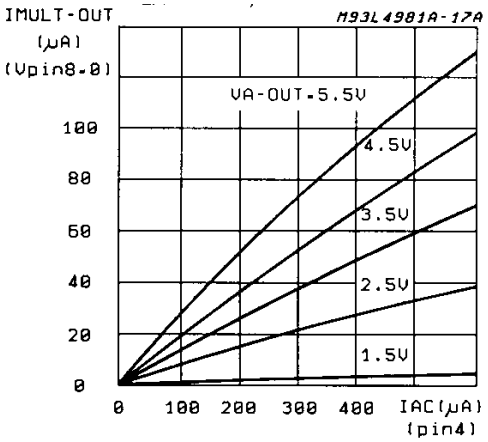


Figure 13d. MULTI-OUT vs. I_{AC} (V_{RMS} = 5.3V; V_{LFF} = 5.1V)

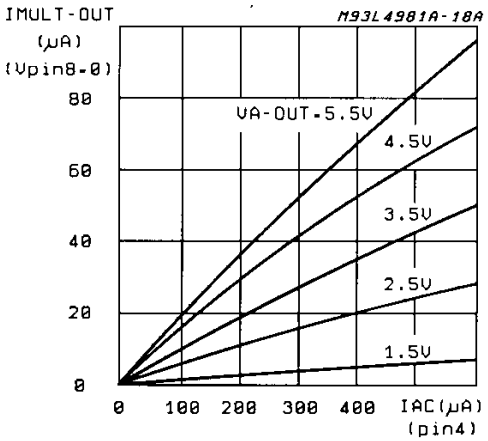


Figure 13e. MULTI-OUT vs. I_{AC} (V_{RMS} = 1.7V; V_{LFF} = 2.5V)

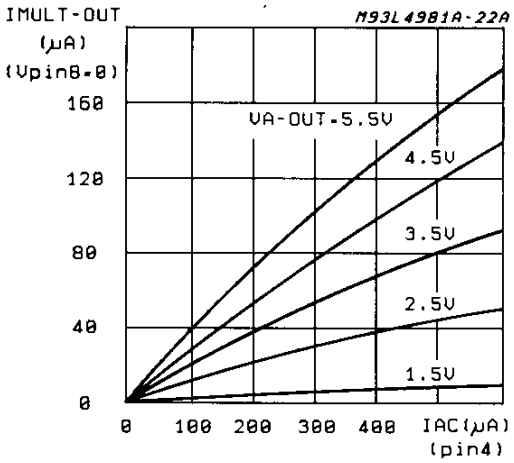


Figure 13f. MULTI-OUT vs. I_{AC} (V_{RMS} = 2.2V; V_{LFF} = 2.5V)

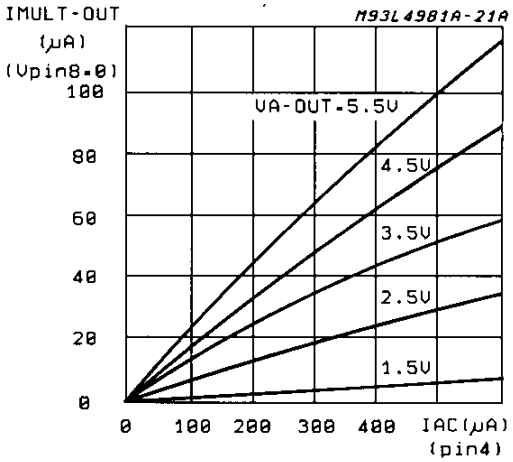


Figure 13g. MULTI-OUT vs. I_{AC} (V_{RMS} = 4.4V; V_{LFF} = 2.5V)

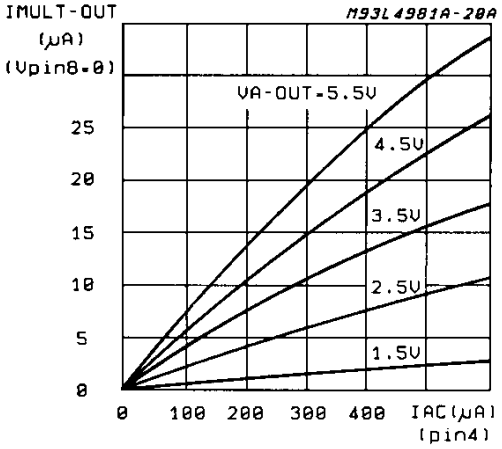
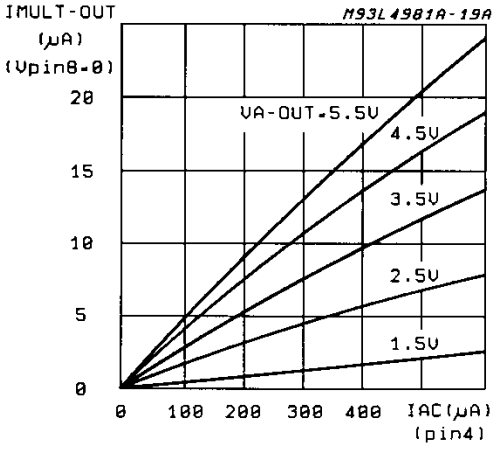


Figure 13h. MULTI-OUT vs. I_{AC} (V_{RMS} = 5.3V; V_{LFF} = 2.5V)



Pin 8 has to be connected through a resistor (R_i') to the negative side of R_S (see fig. 9) to sum the ($I_L \cdot R_S$) and the ($I_{mult} \cdot R_i'$) signals. The sum result is the error signal voltage to the current amplifier non inverting input.

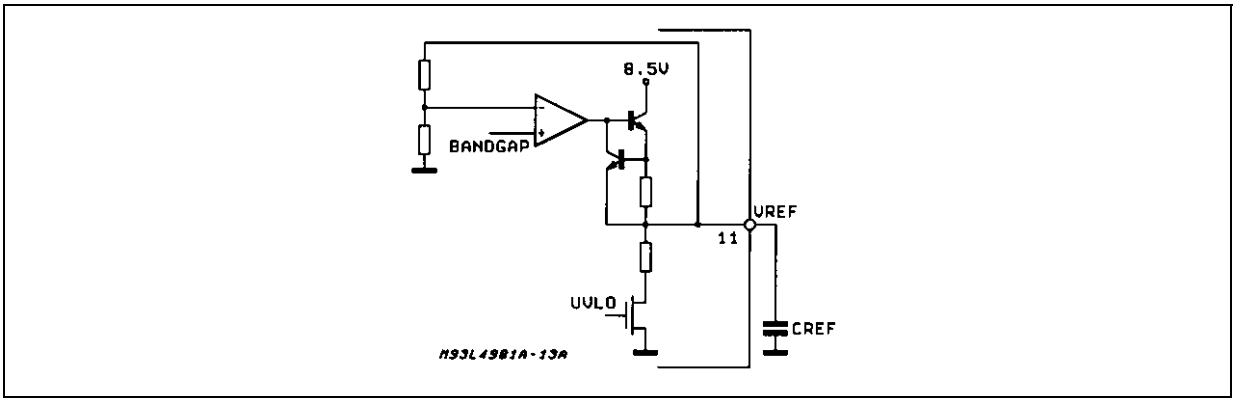
$$R_i' \cdot I_{mult} = R_S \cdot I_L$$

Pin 9. ISENSE (Current Amplifier inverting input). This pin, is externally connected to the external network described at CA-OUT (pin 5). To be noted that Ri and Ri' have the same value because of the high impedance feedback network.

Pin 10. SGND (Signal ground). It has to be connected, to the pc-board GND, close the filtering reference capacitor.

Pin 11. VREF (Voltage reference). An internal bandgap circuitry, allows an accurate voltage reference. An external capacitor filter (from 100nF to some µF) connected to the signal ground is recommanded (see fig. 14). This pin can deliver up to 10mA and can be used for external needs (e.g. enable for other circuits).

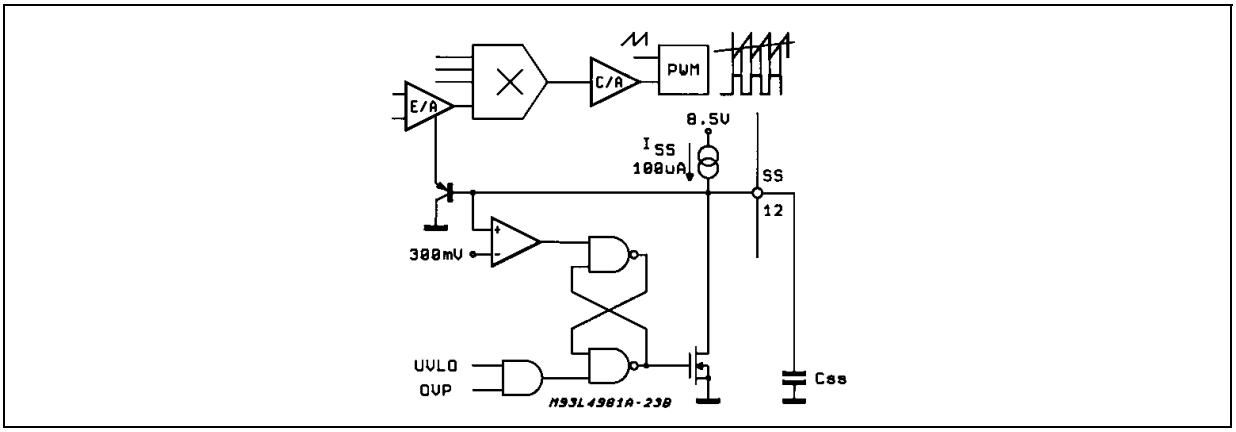
Figure 14.



Pin 12. SS (Soft start). This feature avoids current overload on the external Mosfet (Q) during the ramp-up of the output boosted voltage. An internal switch discharges the capacitor if output overvoltage or VCC undervoltage are detected. An internal current generator of 100µ with the external capacitor define the soft start time costant (see fig. 15). Because the voltage at the softstart pin acts on the E/A output (driving the multiplier with V_{VAOUT} = 5.1V typical voltage swing), the softstart time is defined by:

$$t_{SS} = C_{ss} \cdot \frac{V_{VA\text{-}OUT}}{I_{SS}}$$

Figure 15.



This time (t_{SS}) depends on the application parameters (output voltage, input voltage, output capacitor value, boost inductor size, etc.) and normally the value amounts at some tens of msec.

Pin 13. V_{VA-OUT} (Error amplifier output). Output of the E/A that determinates the control of the boosted regulated voltage (V_O). This pin has to be connected with a compensation network to the pin 14 (see fig.16).

Figure 16.

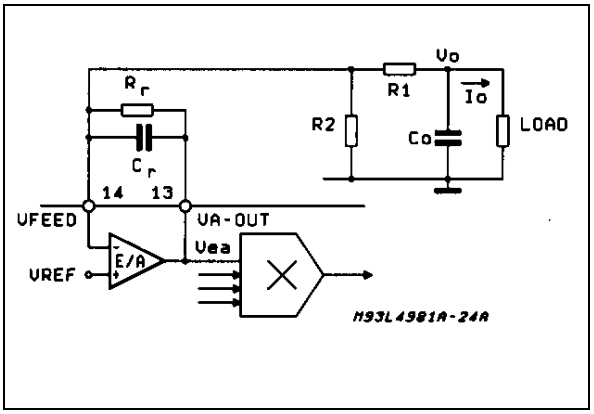
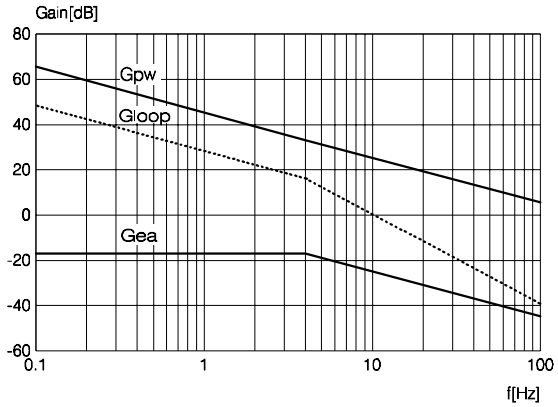


Figure 16a.



First of all, the system does not have to attempt to regulate the twice mains frequency output voltage ripple (ΔV_O) to avoid the line current distorsion. Moreover the system stability has to be ensured. The voltage open loop gain can be splitt in two separated blocks.

The first block small signal gain, is given by the ratio between the E/A output voltage (vea) and output voltage variation (vo) and is defined by the E/A network:

$$Gea' = \frac{vea}{vo} = \frac{1}{s \cdot R1 \cdot C_r}$$

Where Gea` is the E/A gain without R_r ref. fig. 16. R2 has no effect on the error amplifier gain because the inverting input potential is fixed to VREF. The Gea can be seen also as the ratio between the error amplifier output ripple and the imposed output voltage ripple (ΔV_O). The E/A output signal can swing between 1.28V to 5.1V. A value less than 2.5% of the effective E/A output swing voltage (V_{VAOUT} = 3.82V) could be chosen to fix the C_r. So, the Gea defined at the output voltage ripple frequency, determinates the C_r value to ensure the 100/120 Hz (2f) attenuation.

$$Gea \leq \frac{0.095V}{\Delta V_O}$$

$$C_r = \frac{1}{2 \cdot \pi \cdot 2f \cdot R1 \cdot Gea} \geq Ka \cdot \frac{\Delta V_O}{R1}$$

where: Ka = 1/60 for 50Hz and 1/72 for 60Hz mains frequency.

Lower C_r value could increase harmonic distortion.The second block (Power block) is represented by the output filter capacitor (C_O) with its own reactance (X_{CO}), the system has to be able to compensate the total external load variation through the E/A output response (ΔVea). The power gain transfer function (G_{pw}), for large variations can be written:

$$G_{pw} = I_O \cdot \frac{X_{CO}}{\Delta V_{ea}}$$

The total load variation (I_O) to be considered is: $P_{O(max)}/V_O$:

$$G_{pw} = \frac{P_O \cdot X_{CO}}{V_O \cdot \Delta V_{ea}} \Rightarrow G_{pw} = \frac{P_O}{V_O \cdot \Delta V_{ea}} \cdot \frac{1}{s \cdot C_O}$$

The voltage open loop gain contains two poles in the origin, then stability problem can arise. Connecting the resistor (R_r) in parallel to the capacitor C_r to shift the E/A pole from the origin to $1/(R_r \cdot C_r)$, the stability is ensured.

The crossover frequency fc can be calculated by $G_{pw} \cdot G_{ea`} = 1$ and therefore:

$$f_c = \sqrt{\left(\frac{P_O}{V_O \cdot \Delta V_{ea} \cdot 2\pi \cdot C_O}\right) \cdot \left(\frac{1}{2\pi \cdot R1 \cdot C_r}\right)}$$

To allow the highest DC gain maintaining a phase margin of at least 22°, the R_r maximum value is imposed as:

$$R_r \leq \frac{2.75}{2\pi \cdot f_c \cdot C_r}$$

The output filter capacitor value (C_O) is related to the output voltage filtering (see Power section design).

Pin 14. VFEED (Error amplifier input). This pin (see fig. 16), connected to the boosted output voltage through a divider, allows the output D.C. voltage regulation. Neglecting the contribution of the E/A feedback resistor (R_r), the 5.1V reference and the output DC voltage (V_O) define the ratio between R1 and R2:

$$\frac{R1}{R2} = \frac{V_O}{5.1V} - 1$$

To be considered that the R1, togheter with the feedback network(see pin 13 description) define the E/A gain. The R1/Rr ratio affects the load regulation (lower output current increases the output voltage) with the following relation:

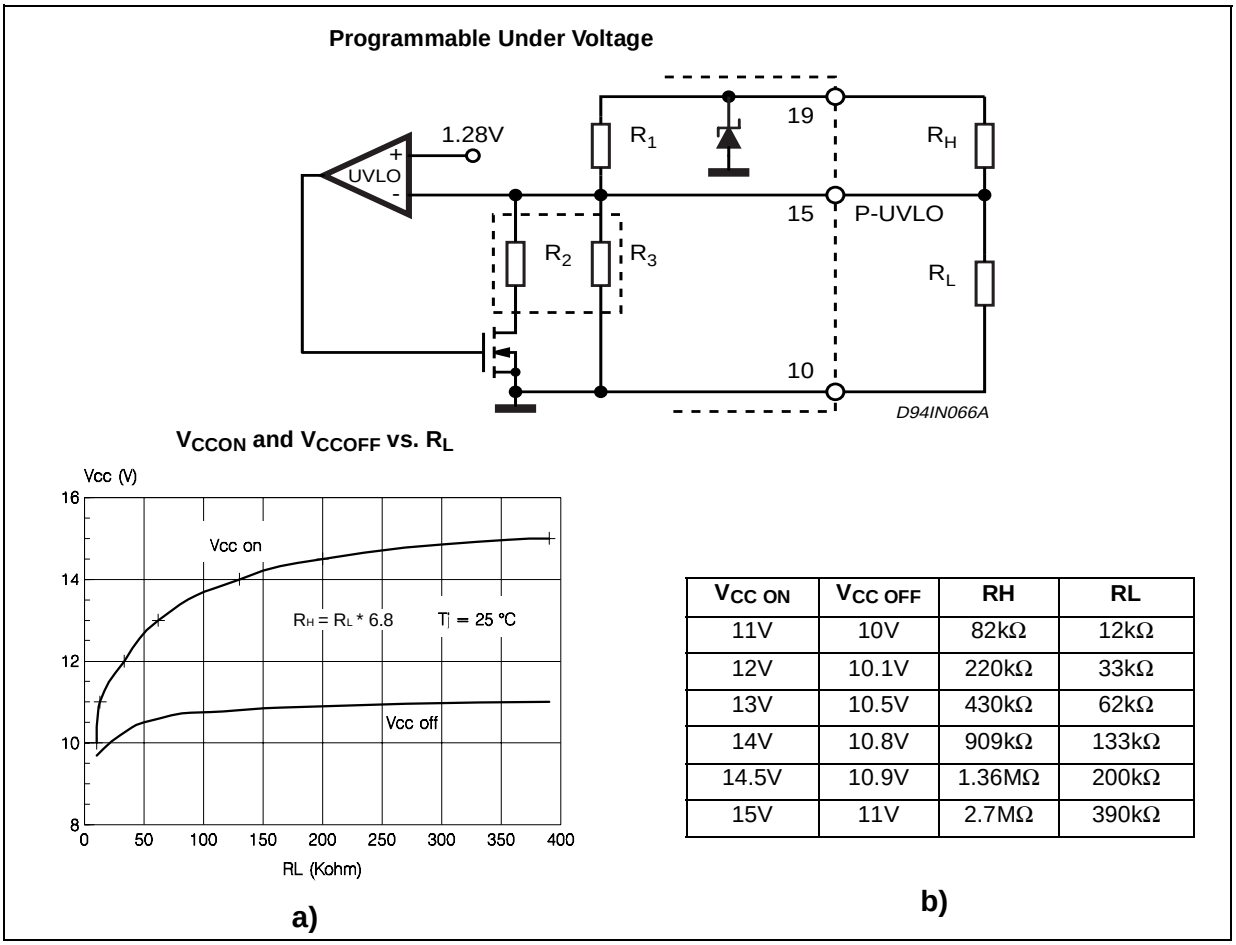
$$\Delta V_{Omax} = \frac{\Delta V_{ea} \cdot R1}{R_r}$$

where: V_{Omax} is the maximum output voltage variation due to the E/A gain reduction and load variation.
The R1 and R2 will be chosen in the high precision class:

Pin 15. P-UVLO (Programmable supply undervoltage threshold). An internal divider (between pin 19, pin 15 and ground) and an internal comparator with a threshold voltage of 1.28V fixes the default turn-on and turn-off 15.5V and 10V levels of the supply section (see fig. 17). Using an external divider (R_H and R_L) it's possible to change the supply thresholds: R_H fixes the hysteresis, R_L fixes the turn-on threshold. To design a divider for a given supply threshold, is useful know (see fig. 17), the typical resistor value, useful to design the external divider, are: R1 = 394k, R2 = 88k and R3 = 58k. Anyway, in fig. 17a/b a diagram with threshold values and a table, useful for a fast choice of R_H and R_L are shown.

For DISABLE function see Appendix B.

Figure 17.



$V_{CC\ ON}$	$V_{CC\ OFF}$	RH	RL
11V	10V	82kΩ	12kΩ
12V	10.1V	220kΩ	33kΩ
13V	10.5V	430kΩ	62kΩ
14V	10.8V	909kΩ	133kΩ
14.5V	10.9V	1.36MΩ	200kΩ
15V	11V	2.7MΩ	390kΩ

Pin 16. SYNC (In/Out synchronization). Only for L4981A, this function allows the device to be synchronized with other circuits of a system (see fig.18a). When the device is externally synchronized, the external clock has to satisfy these conditions: the signal amplitude must cross the threshold value (3.5V), the frequency has to be slightly higher than that programmed by the R-C constant (see pin 18) and the pulse width has to be at least 800 nsec.
If the device has to synchronize other circuits, the signal delivered by this pin is a positive pulse of 4.6V (0.5mA) and the pulse duration is equal to the sawtooth falltime.

The L4981B uses this pin to perform another function. If the application does not use the SYNC function, it is preferrable to focus the EMI filtering problem using the B version. Pin 16, named FREQ-MOD in B version, allows to change the switching frequency in order to spread the energy content over a wider spectrum range.

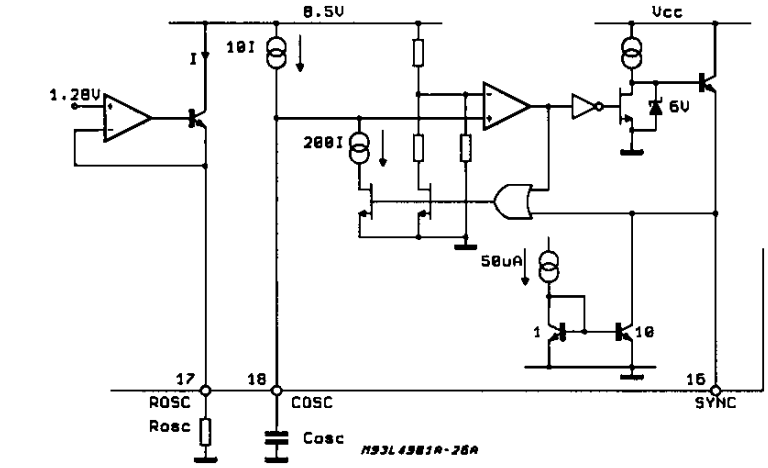
To perform the frequency modulation (see fig.18b), the pin must be connected, through a resistor (R_{fm}), to the rectified line voltage. This allows to change dinamically (cycle by cycle) the (C_{OSC}) charge and the discharge currents that define the ramp slopes of the oscillator sawtooth. The effect of the resistor produces the frequency change (see fig.18c) between the nominal value (f_{sw}) and its minimum value which occurs when the input voltage reaches the peak value (V_{Ipk}). The total frequency variation (see also pin 17 and 18) can be estimated by the formula:

$$\frac{\Delta f_{sw}}{f_{sw}} = K \cdot \frac{V_{IPK} \cdot R_{osc}}{V_{RMS} \cdot R_{fm}}$$

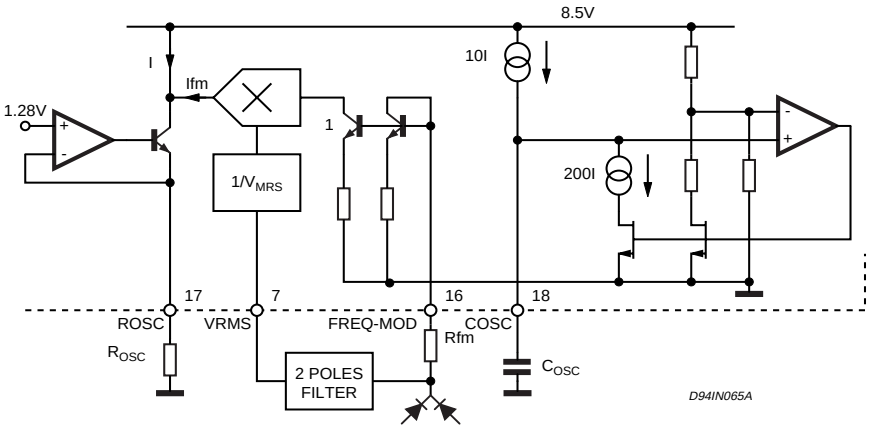
where: R_{fm} is the programming current resistor.
K is a constant value = 0.1157 for R value in KΩ and f_{SW} in KHz.

A typical 20% $\frac{\Delta f_{sw}}{f_{sw}}$ can be a good compromise.

Figure 18.

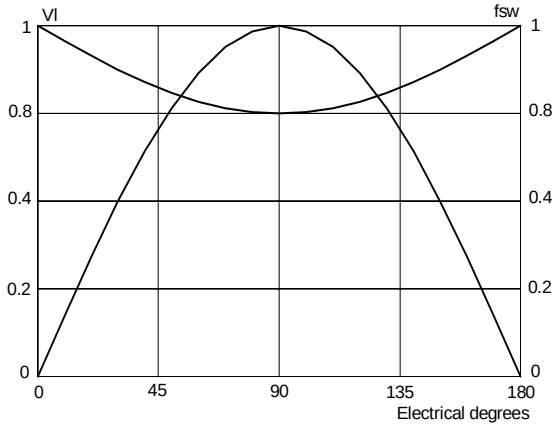


a)



b)

Modulation Frequency Normalzed in an Half Cycle of the Mains Voltage



c)

Pin 17. ROSC (Oscillator resistor). An external resistor connected to ground, programs the charge and the discharge currents that pin 18 (C_{OSC}) forces to the external capacitor. The reference voltage at pin 17 is 1.28V (see fig.18a/b)

To set the charge current, the relation is:

$$I_c \approx 10 \cdot \frac{1.28V}{R_{OSC}}$$

The discharge current is defined by:

$$I_c \approx 200 \cdot \frac{1.28V}{R_{OSC}}$$

The maximum discharge current of Id = 12mA, this means a minimum R_{osc} value of 22KΩ.

Pin 18. COSC (Oscillator capacitor). An external capacitor (see fig 18a/b), connected between this pin and ground, fixes the rise and fall time (t_r and t_f) of the sawtooth oscillator according to the previous relations (pin 17) and therefore the switching frequency. The typical ramp valley-peak voltage (V_{srp}) is fixed to 5V.

The period T is defined by:

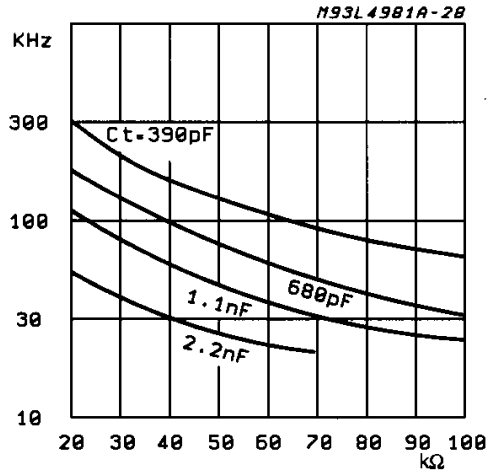
$$T = t_r + t_f = V_{srp} \cdot C_{OSC}\left(\frac{1}{I_C} + \frac{1}{I_d}\right)$$

the switching frequency is:

$$f_{sw} = \frac{1}{T} \approx \frac{2.44}{R_{OSC} \cdot C_{OSC}}$$

See also Fig. 19

Figure 19. Oscillator Diagram



Pin 19. VCC (Supply voltage input). The very low current consumption feature before the turn-on threshold is reached. The undervoltage circuitry, with the threshold hysteresis of 5.5V typ. (see also pin 15) and an internal clamp at 25V (typ.) ensure the IC safety operation.

Pin 20. GDRV (Gate driver output). This output is internally clamped to 15V (see Fig. 20), to avoid ageing problems of the gate oxide. The output driver is normally connected to the gate of the power device through a resistor (say 5 to 50 Ohm) to avoid overshoot and to control the dI/dt of the switch.

POWER SECTION DESIGN

Booster Inductor

The Boost Inductor design involves various parameters to be handled and there are different approaches to define them.

In continuous mode operation, the energy stored in the boost inductor in each switching cycle, is not completely transferred to the output (bulk) capacitor. A quantity of energy is stored in the magnetic circuit, reducing in this way the input current ripple. This minimizes the line noise and reduces the input filter size (see fig.21).

Figure 20.

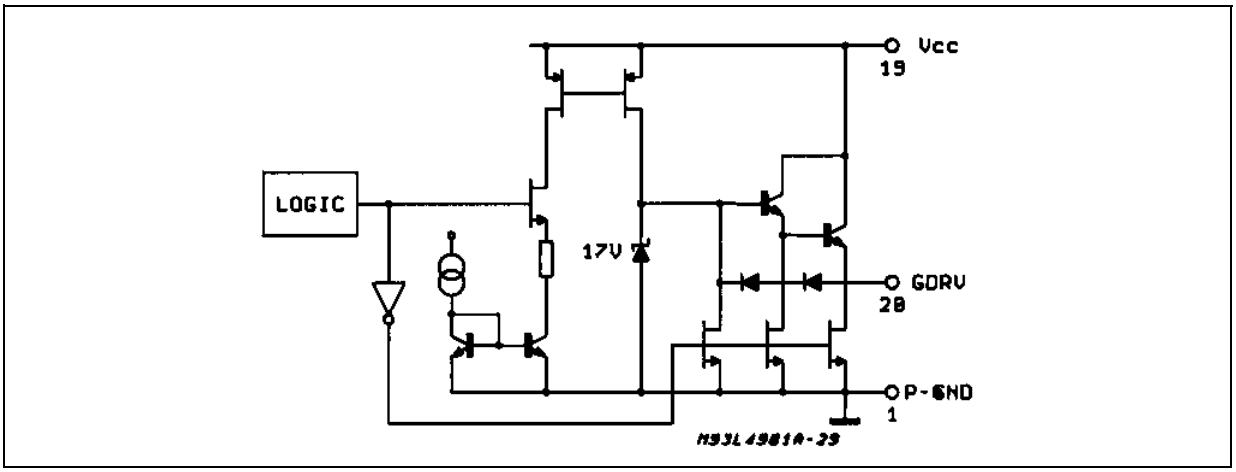
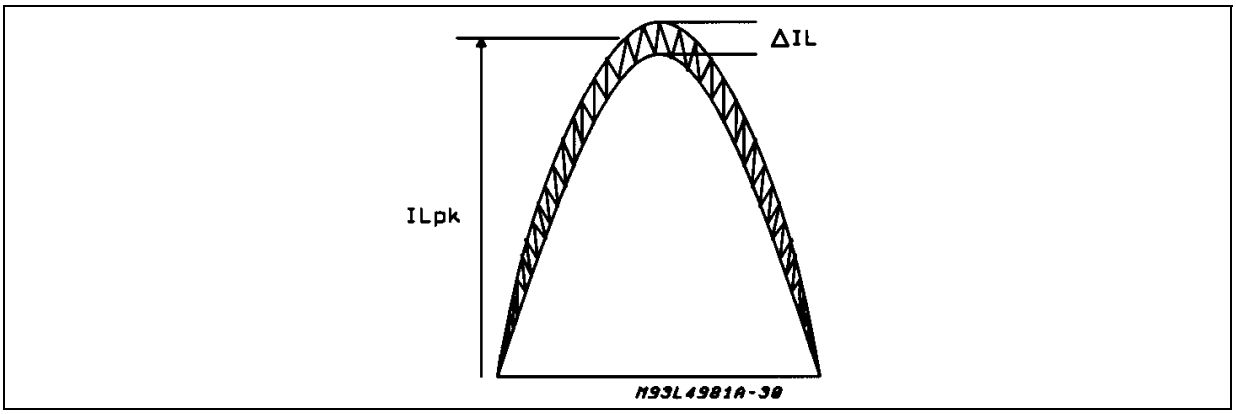


Figure 21.



The energy transferred from the boost inductor to the bulk capacitor in each cycle is:

$$E/cycle = \frac{1}{2}L \cdot (I_{Lp}^2 - I_{Lv}^2) = L \cdot I_{Lt} \cdot \Delta I_L$$

where:

L = Boost Inductance
I_{Lp} = Inductor Peak Current ($I_{Lt} + \Delta I_L/2$)
I_{Lv} = Inductor Valley Current ($I_{Lt} - \Delta I_L/2$)
I_{Lt} = Instantaneous Line Current ($I_{Lp} + I_{Lv}$)/2
ΔI_L = Twice Inductor Current Ripple ($I_{Lp} - I_{LV}$)

Because the instantaneous line current ($_{ILt}$) that corresponds to the average inductor current in the cycle, draws a full rectified (half- sinusoidal) waveform, it is useful to refer to the AC line RMS and peak parameters:

$$I_{Lpk} = \sqrt{2} \cdot I_{Lrms}$$

where:

$I_{rms} = I_{Lrms} = P_I/V_{Irms}$ is the line current
$P_I = P_O/\eta$ is the input power
η is the power yeld.

The power transferred by the inductor in each cycle

$$P_t = \frac{L \cdot I_{Lt} \cdot \Delta I_L}{t_{on}}$$

where: $t_{on} = \delta / f_{sw}$ and $\delta = (V_O - V_{lt}) / V_O$

For a given L, the twice ripple current ΔI_L is the quantity associated to the transferred energy and can be calculated as a certain percentage of the I_{Lpk} inductor current.

$$\Delta I_L = \frac{V_{lt} \cdot (V_O - V_{lt})}{V_O \cdot f_{sw} \cdot L}$$

If the maximum V_{lpk} value is higher than the $V_O/2$, the maximum ΔI_L occours when $V_{lt} = \frac{V_O}{2}$ and its value is

$$\Delta I_{L(max)} = \frac{V_O}{4 \cdot f_{sw} \cdot L}$$

If the V_{lpk} maximum value does not reach $V_O/2$ voltage value, the maximum ΔI_L is reduced and its value is :

$$\Delta I_{L(max)} = \frac{V_{lpk}(V_O - V_{lpk})}{V_O \cdot f_{sw} \cdot L} .$$

In continuous mode operation, an acceptable curent ripple level (K_r) can be considered between 10% to 35%.

$$K_r = \frac{\Delta I_L}{2 \cdot I_{Lpk}}$$

Smaller current ripple on the inductor involves smaller noise on the rectified main bus reducing the input filter size; but the ripple reduction will impose an increase of the boost inductor.

The high voltage, the flux density and the frequency range make the standard high frequency ferrite the most useful material in P.F.C. applications. To avoid the core saturation, related to the high permeability materials, it is necessary built an air-gap in order to allow an adequate magnetic force range (H+Hgap).

An easy approach, is to have an approximated minimum value of core size that could be used to perform the conversion:

$$\text{Volume} \geq K \cdot L \cdot I_{Lpk} \cdot \left(I_{Lpk} + \frac{\Delta I_L}{2} \right)$$

where : K = specific energy constant.

L = Boost inductor value in H.

The specific energy constant (K), mainly depends on the ratio between the gap length (l_{gap}) and the effective length (l_{eff}) of the magnetic core set and on the maximum ΔB swing. Practically

$$K \approx 14 \cdot \frac{l_{eff}}{l_{gap}}$$

can be used to get the minimum volume of the core set in cm^3. After the minimum core-set size is estimated, the suitable type will be selected with technical and economic evaluations.

Next step will be the design of the coil parameters.

The above mentioned formula $P_{Ot} = \frac{L \cdot I_{Lt} \cdot \Delta I_L}{t_{on}}$

if referred to the magnetic path, can be rewritten :

$$P_{Ot} = Ae \cdot l_{eff} \cdot H \cdot \frac{\Delta B}{t_{on}}$$

where :

Ae = effective area of the core section.
l_{eff} = effective magnetic path length.
ΔB = deviated magnetic flux density.
H = magnetic field strength.

The ratio between the ferrite and the air path magnetic permeability, depends on the ferrite materials. Core materials for power application (such as B50/51), have a initial permeability value about 2500 times that of air. This means that, above a certain air-gap length percentage, it is possible to neglect the leff (length of the core) simplifing the calculation e.g. if a 1% of air-gap length, respect to the core lenght value is used, the error introduced is about 4%.

Rewriting $\left(P_{Ot} = Ae \cdot l_{eff} \cdot H \cdot \frac{\Delta B}{t_{on}}\right)$

$$P_{Ot} \approx Ae \cdot l_{gap} \cdot H_{gap} \cdot \frac{\Delta B}{t_{on}}$$

equating to and simplifing $P_{Ot} = \frac{L \cdot I_{Lt} \cdot \Delta I_L}{t_{on}}$

$$Ae \cdot l_{gap} \cdot H_{gap} \cdot \Delta B \approx L \cdot I_{Lt} \cdot \Delta I_L$$

Because: $l_{gap} \cdot H_{gap} \approx N \cdot I_{Lt}$ and $\Delta B = \mu_0 \cdot \Delta H$

$$Ae \cdot N \cdot \mu_0 \cdot \Delta H \approx I \cdot \Delta I_L$$

$$\Delta H \approx N \cdot \frac{\Delta I_L}{l_{gap}}$$

and finally:

$$N \approx \sqrt{\frac{L \cdot l_{gap}}{\mu_0 \cdot Ae}}$$

This simplified relation is much easier to use than the complete one:

$$N \approx \sqrt{\frac{L}{\mu_o} \cdot \left[\frac{l_{gap}}{\left(\sqrt{Ae} + \frac{\pi}{4} \cdot l_{gap}\right)^2} + \frac{l_{eff}}{\mu_0 \cdot Ae}\right]}$$

After N has been defined, it's necessary to check the core for saturation of the magnetic path (rated $N \cdot I_{max}$ vs. Air-gap on ferrites databook). If the check is too close the rated limit, an increase of the lgap (gap lengh) and a new calculation will be necessary. Copper losses $R_L \cdot I^2_{Lrms}$ and former's winding space available will be considered for the wire selection.

An auxiliary winding can be used just to get a low cost supply for the I.C. It will be a low cost thin wire coil will be used and the number of turns is the only parameter to define.

Input Bridge

The input diodes bridge can be standard off-line, slow-recovery and low cost devices. The device selection considers just the input current (Irms) and the thermal data.

Input Capacitor

The input filter capacitor (C_{IN}) has to sustain the input instantaneous voltage (V_{It}), with an imposed voltage ripple, during the turn-on (t_{on}) time of the Mosfet.

The worst conditions will be found at the minimum rated input voltage $V_{Irms(min)}$.

The maximum high frequency voltage ripple ($r = \Delta V_I / V_I$) has to be imposed:

$$C_{IN} \geq K_r \frac{I_{rms}}{2 \cdot \pi \cdot f_{sw} \cdot r \cdot V_{Irms}}$$

Where: K_r is the current ripple coefficient.
r = 0.02 to 0.08.

The C_{IN} maximum value is limited to avoid current distortion.

Output Bulk Capacitor

The choice of the output bulk capacitor (C_O), mainly depends on the electrical parameters that affect the filter performances and also on the subsequent application.

The D.C. output voltage and overvoltage, the output power and voltage ripple are the first parameters to consider in all applications. The RMS capacitor ripple current $I_{C(2f)rms} = I_o/\sqrt{2}$ and so, the output voltage ripple (ΔV_O) will be:

$$\Delta V_O = I_O \sqrt{\frac{1}{(2\pi \cdot 2f \cdot C_O)^2} + (ESR)^2}$$

With a low ESR capacitor can be simplify:

$$C_O + \frac{I_O}{2\pi \cdot 2f \cdot \Delta V_O} = \frac{P_O}{2\pi \cdot 2f \cdot \Delta V_O \cdot V_O}.$$

Although the ESR, normally does not affect the output ripple parameter, it has to be considered in power losses account both for the rectified mains frequency and the switching frequency.

If the application (i.e. computer supply) has to guarantee a specified Hold-Up time (t_{HOLD}), the capacitance sizeing criteria will change:

The C_O has to deliver the supply energy for a certain time and a specific dropout voltage.

$$C_O = \frac{2 \cdot P_O t_{HOLD}}{V_{O\_min}^2 - V_{op\_min}^2}$$

where:

V_{O_min} = minimum output voltage value (normally at the maximum load conditions)

V_{op_min} = minimum output operative voltage before the 'power fail' detection.

Power Switch

A power MOSFET is the active switch used in most application for its frequency features. It will be selected according with the output boosted voltage and the delivered power. There are two contributions for power losses in the mosfet: conduction losses and switching losses. The on-state power losses can be calculated using the formula:

$$P_{on\text{-}MOS} = I_{Qrms}^2 R_{dson}$$

One extimation of the switching losses can be done considering two separated quantities:

$$P_{capacitive} \approx \left(\frac{10}{3} \cdot C_{oss} \cdot V_o^{1.5} + \frac{1}{2} C_{ext} \cdot V_o^2\right) \cdot f_{sw} \cdot$$

$$P_{crossover} \approx V_O \cdot I_{rms} \cdot t_{cr} \cdot f_{sw} + P_{rec}$$

where:

C_{oss} is the Drain capacitance at V_{DS} = 25V.
t_{cr} is the crossover time.
C_{ext} is the external layout stray capacitance.
P_{rec} is the contribution due to the diode recovery.

To reduce the crossover losses a snubber network can be used.

Booster diode

The booster diode will be selected to withstand the output voltage and current. Moreover, it has to be as fast as possible in order to reduce the power switch losses.The STMicroelectronics Turboswitch™ diode series match this specifications, and are expecially suitable for this application.

The diode power losses can be split in two contributions: conduction losses and switching losses. The conduction losses can be estimated by:

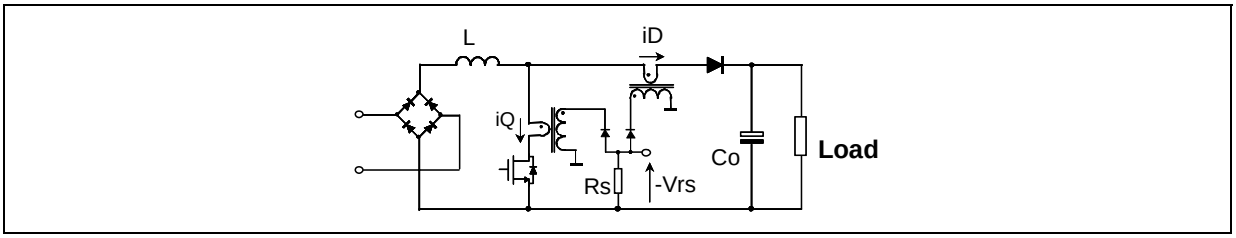
$$P_{Don} = V_{to} \cdot I_O + R_d \cdot I_{Drms}^2$$

where: V_{to} = threshold voltage
R_d = differential resistance

Sense Resistor

The sense resistor produces the signal for the current feedback loop and for the overcurrent protection circuit.
An easy criterion to choose the sense resistance is to minimize the power dissipated assuring a sufficient signal to noise ratio. In much high power applications, it could be considered the magnetic sensing approach (see fig. 22).

Figure 22. Magnetic Sense



DESIGN PROCEDURE.

In order to fix the described concepts, here follows a brief description of a possible design flowchart referred to a typical "low-medium range power" PFC application.

Design target specification:

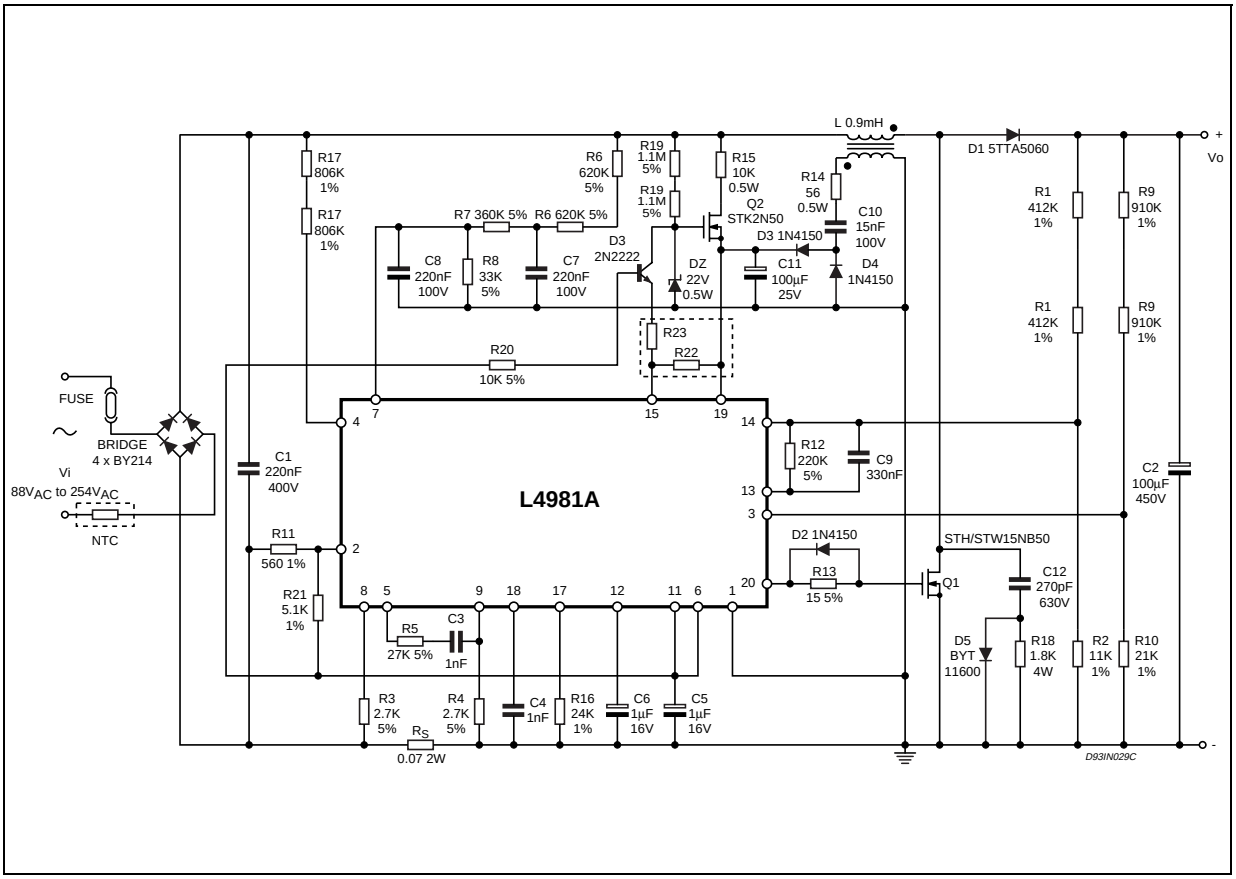
- Wide range mains; V_{INrms} = 88 Vac to 264 Vac.
- Pre-Regulated DC output voltage; V_O = 400 V.
- Rated output power; P_O = 200W.

The design starts fixing the operating conditions.

- The switching frequency 100kHz ///
- The 100Hz voltage ripple imposed at full load is ± 8V; this is satisfied selecting C_{out} = 100µF
- The Over Voltage limit is set at V_{out}+50V
- The maximum current ripple at nominal load has been chosen = 35%

The circuit in fig. 23 can be proposed as reference for medium range power PFC application.

Figure 23. Low-medium Power Typical Application (V_O = 400V; P_O = 200W)



Input capacitor

The input capacitor, placed across the rectified mains, must be considered as part of the EMI filter. The advantage, in placing this part after the mains rectification, is the shunt effect for the high frequency current in order to avoid it to flow throws the diodes of the bridge due to the poor recovery characteristic.

On the other side, the value of this capacitor must to be held as low as possible because the inherent DC voltage content affects the harmonic distortion.

With 220nF, the high frequency is filter enough and the introduced DC level can be considered not significant at reasonable load.

Output capacitor

For the output capacitor selection, it can be consider just the output voltage ripple.

Choosing 100µF/450Vthr 100/120Hz ripple is ± 8Vac

Instead, if the pre regulated voltage bus must ensure enough energy for Hold-up requirements (i.e. the energy is delivered to a power supply system), the Coot value will be increased to around 180µF.

Sense resistor

The sense resistance (Rest) is selected considering both, the signal level and the power dissipation parameters.

Using ±70mΩ, the sense signal is good enough to be managed by the current loop. On the other side, the maximum power dissipation will be:

$$P_{ros} = R_S \cdot (I_{lrms}^2 + I_{lhfrms}^2) \leq 0.5W$$

Where Alarms max. = 2.50A

Power Mos

The Mosfet breakdown voltage is imposed; Bvdss ≥ V_{out} + Dv_{out} + margin = 500V. The R_{dson} is selected taking in to account the conduction power dissipation.

The formula for calculation is: $P_{on\_max} = I_{qrms}^2 \cdot R_{don}$

i.e. considering $R_{on(t)}$ = 0.7Ω the P_{on_max} = 2.15 · 0.7 = 3.3W.

Adding the switching (and the capacitive) losses we can estimate 8W to 10W total power dissipation.

Boost Diode

The continuous current mode of operation, suggest using an Ultra-fast reverse recovery diode. The STMicroelectronics TURBOSWITCH™ family offers a good solution for this kind of application.

Boost Inductor

The inductor design starts defining the L value that is a function of the switching frequency and the accepted current ripple. In this design, we suggest an inductor value L = 0.75mH that can be realized using an ET3411 gapped set-core ferrite.

The results, concerning the described circuit, have been tested. And the result are shortly here reported:

V_i	f	P_i	PF	A-THD	H3	H5	H7	H9	V_O	ΔV_O	P_O	η
(V_{rms})	(Hz)	(W)		(%)	(%)	(%)	(%)	(%)	(V)	(V)	(W)	(%)
110	60	220	0.999	1.79	1.40	0.40	0.31	0.28	392	8	201	91.6
220	50	217	0.997	2.25	1.68	0.83	0.57	0.48	398	8	204	94.2

DEMO-BOARD:

Design process and Evaluation results

In order to provide a powerful tool for the complete evaluation of the L4981, It is available a populated Demo-Board. The design process and the description for the demo, is here described.

The demo has been designed to operate in wide range mains and the size and is finalized for a "medium-high" output power range.

Let us start fixing the overall target of the application.

Electrical target specification:

- Wide range mains; V_{INrms} = 88 to 264 Vac.
- Regulated DC output voltage; V_O = 400 V.
- Rated output power; P_O = 360W in any mains condition.
- Target efficiency ≥ 90% in nominal load conditions.

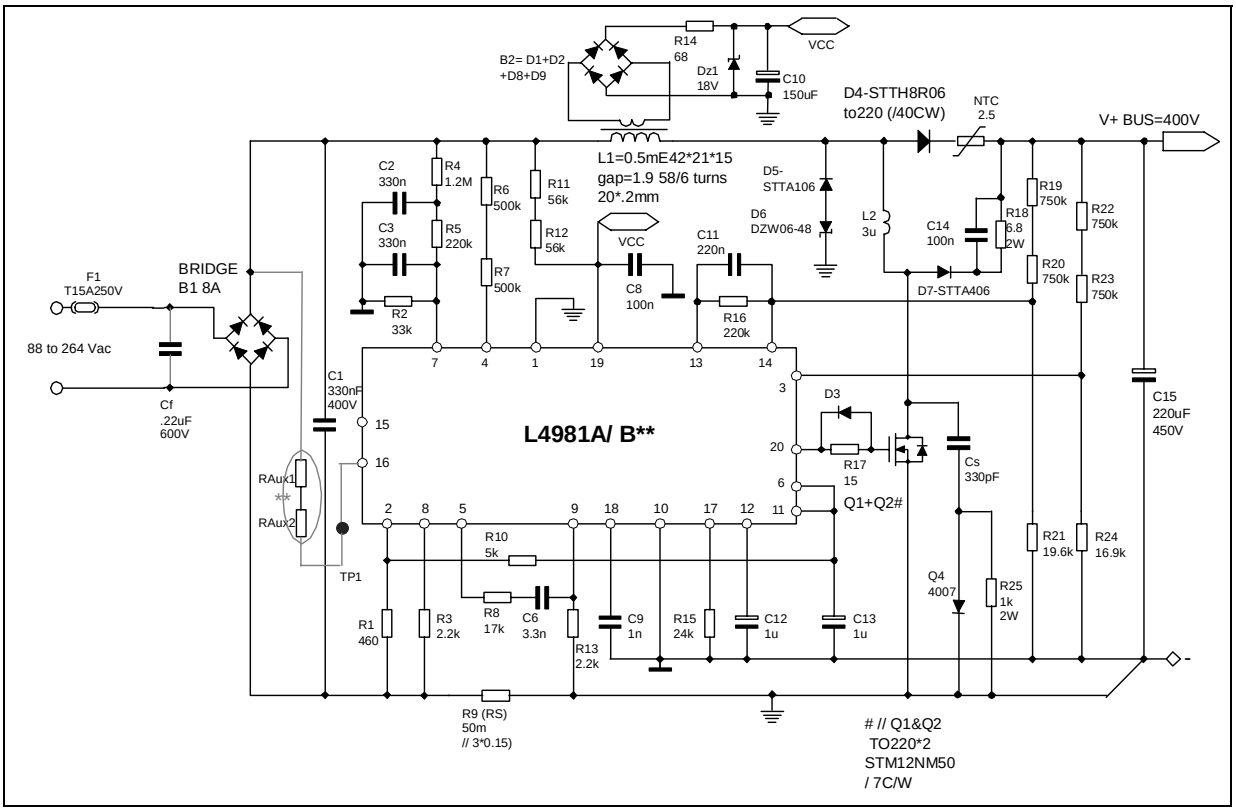
Chosen operation conditions of the application

- The rectified mains (100/120Hz) full load voltage ripple is ± 7-8 V (peak to peak) this is achieved using an output capacitor C_{out} = 220Uf/450V
- The maximum current ripple, in nominal load condition, is selected to be about 20%. This can be obtained using the boost inductor L = 0.55mH and setting the switching frequency at 100kHz. ##
- The Over Voltage Protection has been set at V_{out} + 58V

The demo is capable to deliver around 400W output power; anyway in order to limit the temperature, the rated power is limited to 360W.

The schematic is shown in fig 24.

Figure 24. Demo Board Circuit (V_O = 400V; P_O = 360W)



Some design peculiarities

A **magnetic snubber** solution has been adopted in order to limit/control the ramp rate of the current at the turn-on edge of the Power Mos, referring to the schematic, the parts involved in this function are:

L2, D5, D6, D7, C14 and R18.

The function of the auxiliary inductor L2 is to reduce the ramp rate of the current reducing in this way the peak current, due to the recovery of the boost diode (D4), and the associate noise emission.

The additional benefit of this magnetic snubber is also the reduction of the switching power dissipated in the Mos. D5 and D6 needs to provide a path that allows the demagnetization of the inductor L2, clipping the negative spike thus avoiding the Breakdown activation of the booster diode D4.

D7, C14 and R18 will clamp the energy of L2 at the turn off edge of the Mos.

The **inrush current** limiter NTC is placed between the cathode of the boost diode and the bulk capacitor C15. In this way, the current flowing in to the NTC limiter is the same of the boost diode well below the mains current especially at minimum mains value.

The demo is provided with "**self-supply**" circuit. The proposed supply circuit, using a Graetz bridge is much efficient anyway; it can be inadequate when the output power is reduced down to less than 5W.

On board, it has been recovered place for the Raux1 and Raux2. The two resistors will be connected in case of **L4981B** version evaluation.

Here follows some comment concerning the design and the selection of the **power parts** of the demo.

Input capacitor selection

The demo is not provided with complete dedicated EMI filter. At the input side, two parts compose the capacitor; the first (Cf.) is placed across the AC input of the bridge and the second one (C1) is tied to the rectified mains. The advantage, of this configuration is the minimization of the DC content in placing a low value after the mains rectification (C1), just to filter the high frequency. The capacitor Cf placed in the AC side must be considered as part of the EMI filter.

Output capacitor selection

For the output capacitor selection, it can be consider just the output voltage ripple.

Choosing Co = 220µF (450V), the maximum rectified mains ripple is:

$$\Delta V = \frac{\pi_o}{200 \cdot \pi \cdot V_o \cdot C_o} = 7.3V$$

Sense resistor selection

The sense resistance is set at 50mOhm ($R_S = 3 \cdot 0.15Ohm//$) maximum power dissipation (@ 88Vac mains and 360W) will be:

$P_{Rs(max)} = RS \cdot (I_{lrms}^2 + I_{lhfrms}^2) = 1.04W$
Where: $I_{lrms\ max.} = 4.55A$

Power Mos

In the selection of the power switch, it has been preferred to share the thermal dissipation in two separate TO220 packages. This is a good solution because the size of the heath sinkers can be limited.

The breakdown voltage is imposed = 500V.

Considering the On resistance (@ T_j = 100°C) = 320 mΩ the formula for the dissipated power calculation are:

Conductive losses $P\_On_{(max)} = I_{Q(max)}^2 \cdot R_{don} = 3.9 \cdot 0.32 = 4.9W$.

Adding the capacitive (about 2.5W) and the switching losses (as low as 2-3 W, thanks to the snubber) we can estimate **10 to 12W** total power dissipation at lower mains value.

Boost Diode

The 8A 600V chosen Turbuswitch fits well with the application. The power dissipated in the boost diode is about 1.4W.

Boost Inductor

The 0.55mH chosen inductor value allows a low ripple (23%) of its current; moreover, there is enough room (in the industrialization phase) to reduce the switching frequency holding an acceptable current ripple (e.g. reducing the frequency to 75 kHz the current ripple will be held within 30%.

In this design, the coil has been realized with a gapped set-core ferrite E42*12*15.

The results that can expect, realizing the described circuit, has been tested. And the result are shortly reported from Table 1 to Table 6.

The PCB and component Layout can be seen in figgs 25, 26 and 27 (The Gerber files of the PCB are available on request).

Figure 25. Component Layout (Dimensions 88 x 150mm)

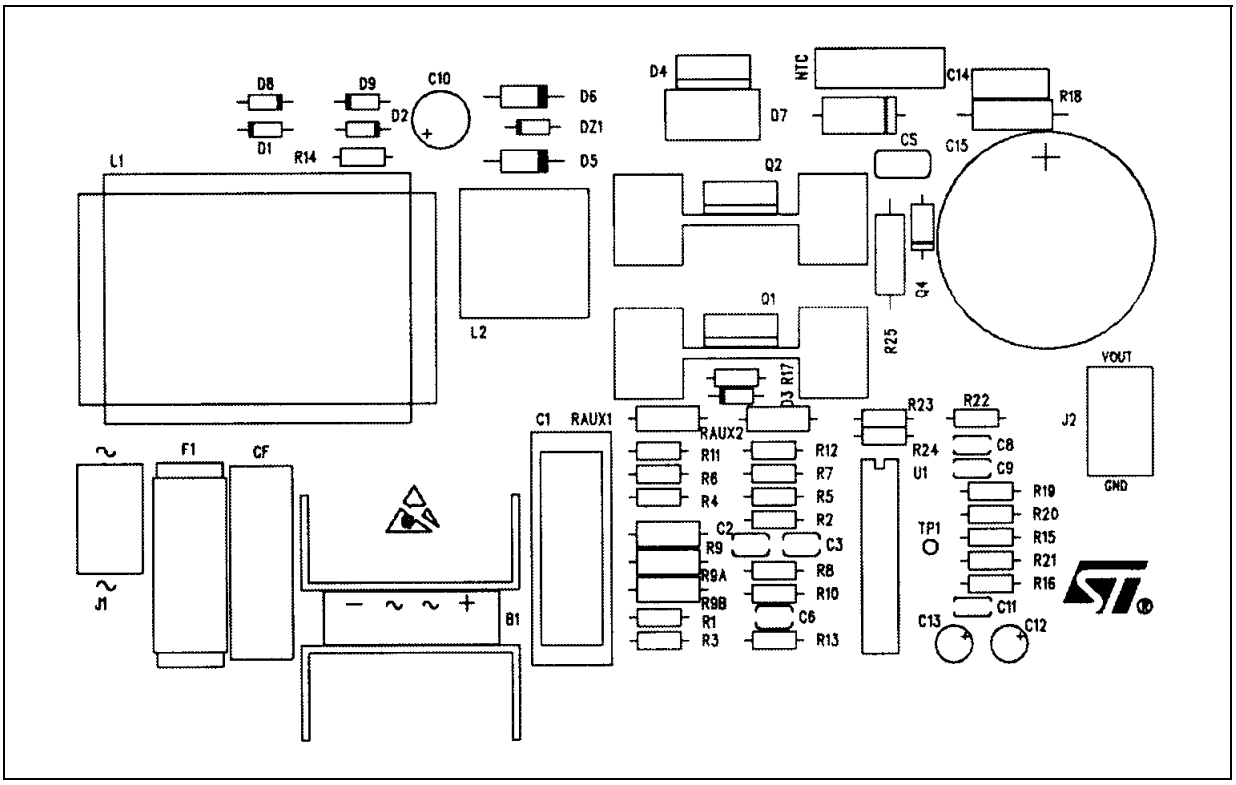


Figure 26. P.C.B. Component Side (Dimensions 88 x 150mm)

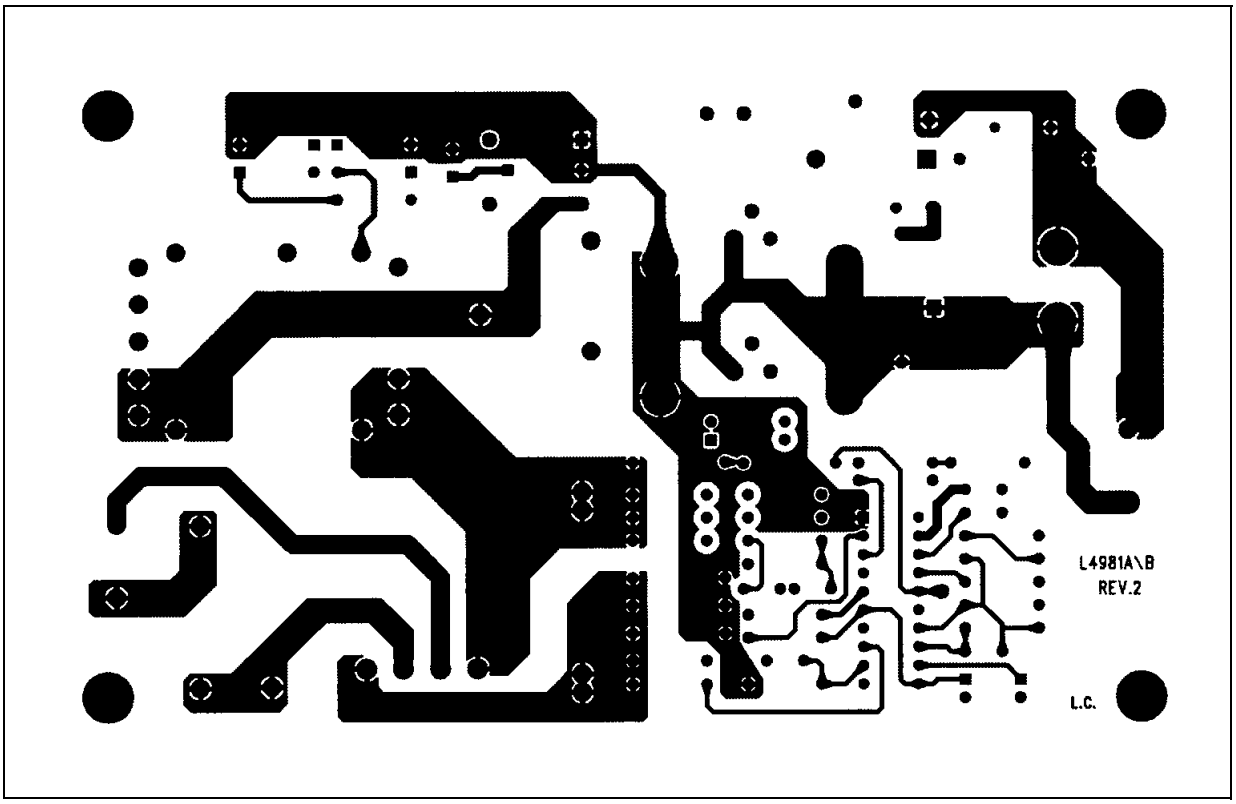
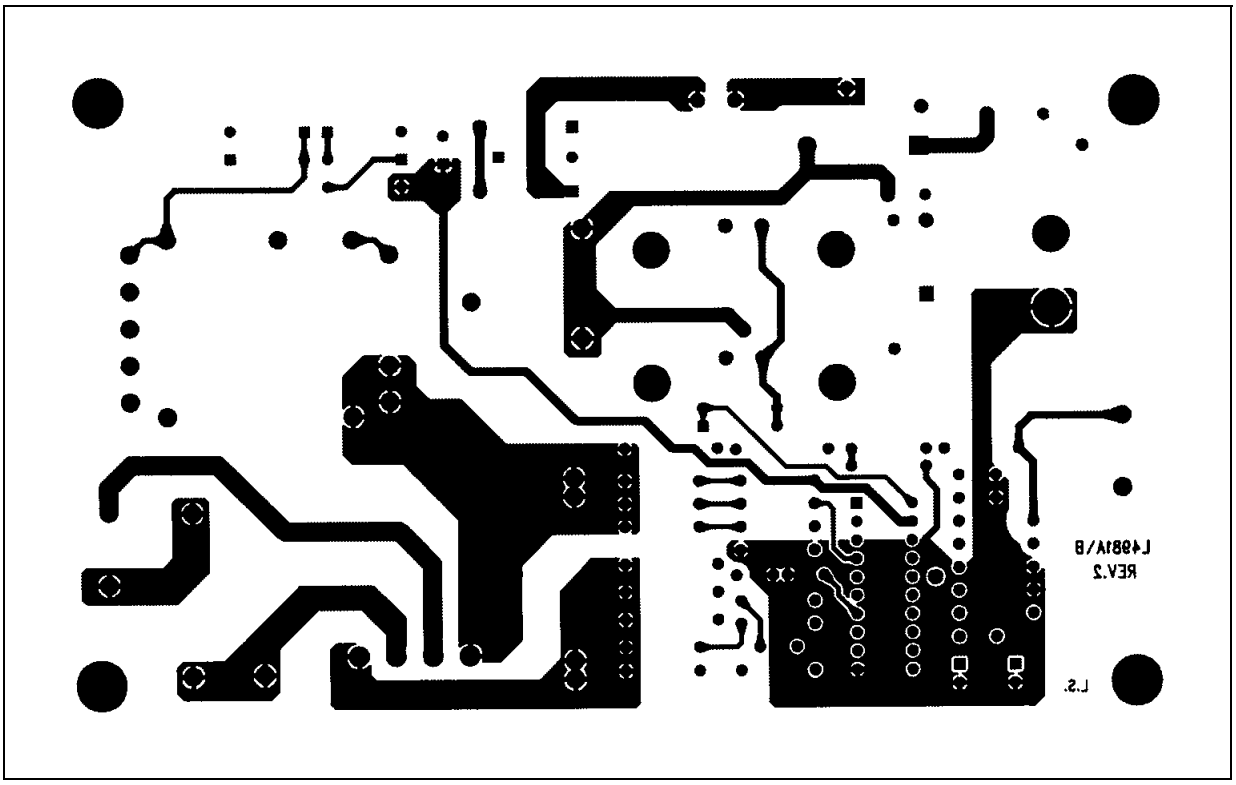


Figure 27. P.C.B. Solder Side (Dimensions 88 x 150mm)



DEMO BOARD TEST RESULTS

Table 1. Maximum power range at 110Vac

V_{mains}	P_{out}	V_{out}	P_{in}	THD	PF	Eff.
88Vac	403W	401Vdc	433W	5.1%	0.998	.93
110Vac (*)	407W	403Vdc	431W	2.2%	0.999	.945
132Vac	409W	404Vdc	430W	2.7%	0.999	.95

(*) Most significant losses balance at maximum power (110Vmains):

- Power-mos (Q1+Q2) dissipated power = 9.6W.
- Bridge (B1) dissipated power = 6.3W.
- Boost turbo-diode (D4) dissipated power = 1.6W.
- Boost inductor L1 = 2W
- Aux. Inductor L2 = 1.6W.
- NTC dissipated power = 1.1W.
- Snubber = 1.4W

Table 2. Maximum power range at 220Vac

V_{mains}	P_{out}	V_{out}	P_{in}	THD	PF	Eff.
176Vac	415W	407Vdc	430W	4.2%	0.997	.965
220Vac (*)	417W	408Vdc	431W	5.8%	0.994	.967
264Vac	419W	409Vdc	431W	7.4%	0.989	.972

(*) Most significant losses balance at maximum power (220Vmains):

- Power-mos (Q1+Q2) dissipated power = 7.1W.
- Bridge (B1) dissipated power = 4W.
- Boost turbo-diode (D4) dissipated power = 1.3W.
- Boost inductor L1 = .6W
- Aux. Inductor L2 = 0.9W.
- NTC dissipated power = 0.8W.
- Snubber = 0.9W

Table 3. Nominal power range at 110Vac

V_{mains}	P_{out}	V_{out}	P_{in}	THD	PF	Eff.
88Vac	366W	404Vdc	397W	5%	0.998	.92
110Vac (*)	370W	406Vdc	395W	2.2%	0.999	.94
132Vac	372W	407Vdc	394W	3%	0.999	.945

(*) Most significant losses balance at nominal power (110Vmains):

- Power-mos (Q1+Q2) dissipated power = 9.3W.
- Bridge (B1) dissipated power = 5.7W.
- Boost turbo-diode (D4) dissipated power = 1.5W.
- Boost inductor L1 = 1.8W
- Aux. Inductor L2 = 1.35W.
- NTC dissipated power = 1W.
- Snubber = 1.2W

Table 4. Nominal power range at 220Vac

V_{mains}	P_{out}	V_{out}	P_{in}	THD	PF	Eff.
176Vac	378W	410Vdc	394W	4.7%	0.997	.959
220Vac (*)	381W	412Vdc	395W	6.4%	0.993	.964
264Vac	381W	412Vdc	395W	8.1%	0.987	.964

(*) Most significant losses balance at nominal power (220Vmains):

- Power-mos (Q1+Q2) dissipated power = 6.9W.
- Bridge (B1) dissipated power = 3.5W.
- Boost turbo-diode (D4) dissipated power = 1.3W.
- Boost inductor L1 = 0.5W
- Aux. Inductor L2 = 0.83W.
- NTC dissipated power = 0.8W.
- Snubber = .8W

Table 5. Half power range at 110Vac

V_{mains}	P_{out}	V_{out}	P_{in}	THD	PF	Eff.
88Vac	219W	420Vdc	239W	2.4%	0.999	.916
110Vac (*)	220W	421Vdc	238W	3.6%	0.999	.925
132Vac	222W	423Vdc	237W	2.7%	0.999	.937

(*) Most significant losses balance at half power (110Vmains):

- Power-mos (Q1+Q2) dissipated power = 7.5W.
- Bridge (B1) dissipated power = 3.7W.
- Boost turbo-diode (D4) dissipated power = 1.1W.
- Boost inductor L1 = 1.3W
- Aux. Inductor L2 = 0.95W.
- NTC dissipated power = 0.7W.
- Snubber = 1W

Table 6. Half power range at 220Vac

V_{mains}	P_{out}	V_{out}	P_{in}	THD	PF	Eff.
176Vac	223W	424Vdc	236W	8%	0.993	.945
220Vac (*)	223W	424Vdc	235W	10.5%	0.994	.949
264Vac	223W	424Vdc	235W	15%	0.978	.95

(*) Most significant losses balance at half power (220Vmains):

- Power-mos (Q1+Q2) dissipated power = 5.64W.
- Bridge (B1) dissipated power = 1.9W.
- Boost turbo-diode (D4) dissipated power = 0.88W.
- Boost inductor L1 = .5W
- Aux. Inductor L2 = 0.6W.
- NTC dissipated power = 0.52W.
- Snubber = 0.7W

Significant waveforms

Since the described application is provided with a "magnetic snubber circuitry", it is of some interest to have a look at some switching waveform.

In figure 28, it is depicted the power drain voltage and the current measured in L2 (aux. Inductor) .

To be observed the "delay effect" of the current and the control of its slope. In fact, this circuitry allows to hardly reducing the Voltage-Current power crossing and the ramp rate of the drain current, reducing in this way the power dissipated inside the switch and the high frequency contents of the switching.

In figure 29, it is shown both the switching edge and pointed the recovery charge due to the boost diode and the effect of the Voltage Clamp (D7, C14, R18).

In figure 30, the switch-off edge is magnified and pointed out the effect of the RCD snubber to ground (Cs, Q4 R25) limiting the dV/dt and the above-mentioned Voltage Clamp.

Finally, in figure 31, it is shown and pointed, in the reverse recovery region, the demagnetization effect of the D5+D6 and its control on the second slope of the recovery itself.

Figure 28.

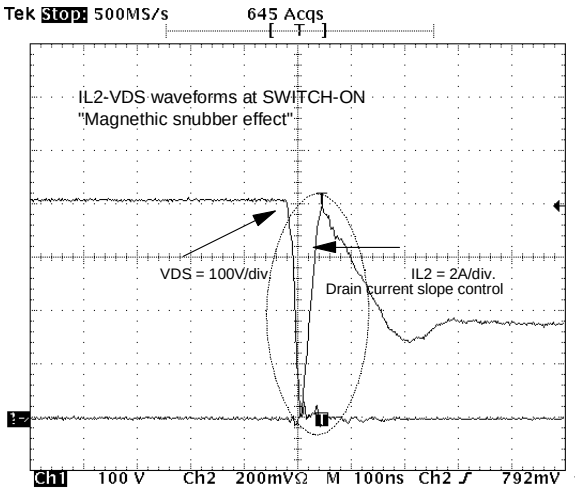


Figure 29.

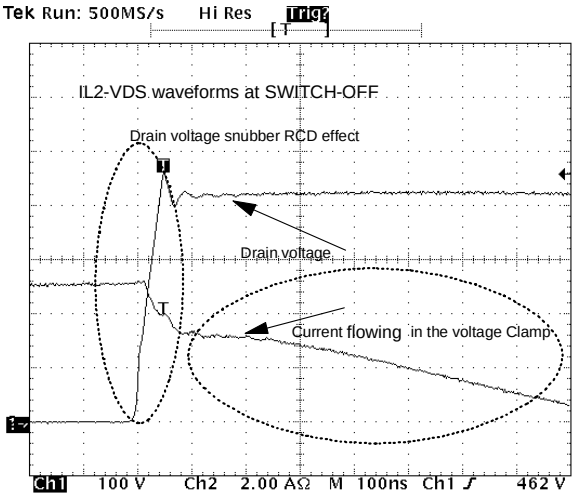


Figure 30.

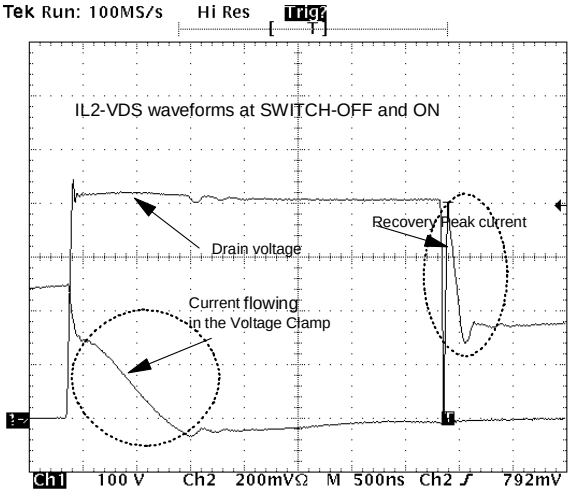
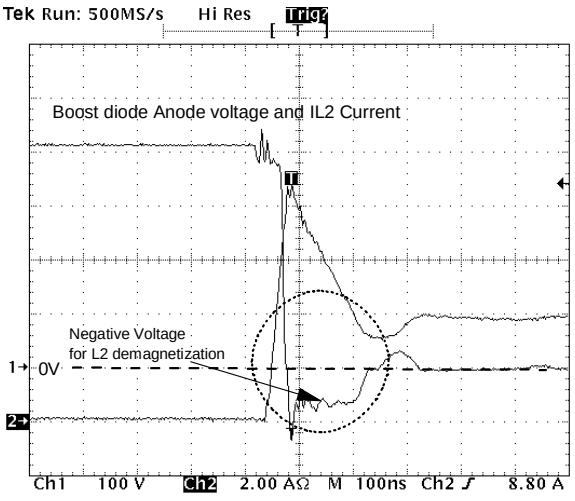


Figure 31.



Miscellaneous:

The 360W Demo Board is replacing a previous 200W version. It is possible to order this tool quoting the order code EVAL4981A. The board comes with a CDROM containing the inherent documentation and a special program dedicated to the ST PFC controllers (L4981 and L6561) that make it easy the design of these applications.

APPENDIX A

LFF (pin 6) Function.

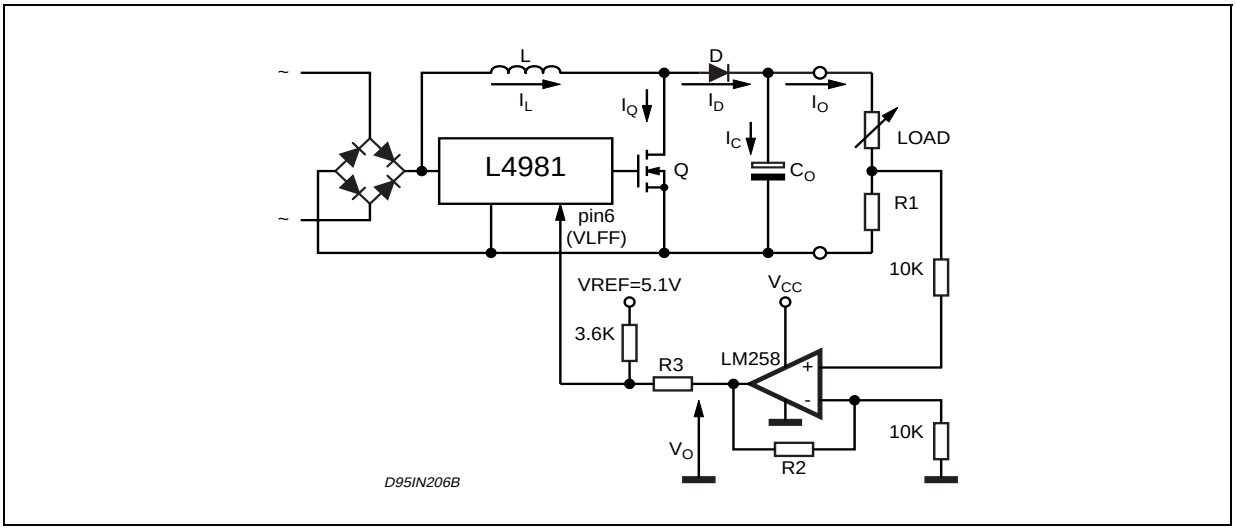
Since in Power Factor applications the Error Amp. compensation network has to filter the mains frequency contents, in order to reduce harmonic distortions, the crossover frequency of the loop gain must be low. This involves a poor load transient response.

An additional function (LFF) is available in L4981A/B devices. It is expecially suitable to modify the multiplier output current, proportionally to the load, in order to improve the system response bypassing the E/A.The control is working with VLFF voltage between 2V and 5.1V.

In fig. 32 is shown an application example to explain this function. An external OP-AMP has been used to get the suitable signal voltage avoiding sense resistor (R1) power dissipation.

In the real application the sense resistor is often replaced by sense transformer.

Figure 32. Application example



Design criteria:

It is avisable to ensure a minimum VLFF ≅ 2V at the minimum output current.Since the OP-AMP (LM258) Vol = 0.7V (@ 1mA), to get the minimum voltage at VLFF, 1.3V has to be added. A resistor devider tied to the reference voltage (pin 11 of the controller) shifts the output of the OP-AMP.

$$\text{therefore } 1.3V = \frac{(5.1V - 0.7V)}{R3 + 3.6k\Omega} \cdot R3 \Rightarrow R3 = 1.3k\Omega$$

The OP-AMP supply voltage is the same used for PFC controller (V_{CC}) and its gain if fixed in order to produce V_O = 5.1V at the maximum load ($I_{O\,max}$).

$$V_O = R1 \cdot I_{Omax} \cdot \left(1 + \frac{R2}{10k}\right) = 5.1V$$

E.g. for I_{Omax} = 3A. R1 = 0.1Ω - 1W R2 is roughly 160KΩ.

APPENDIX B

Disable

Sometimes it is useful to disable the controller. For example, in a complete system in which a PWM regulator follows the PFC stage, at low output power it is advantageous to shutdown the PFC section to improve the overall system efficiency (stand-by / sleep mode). Likewise most of controllers, one way to do this (using L4981A/B), is pulling down either the Soft-Start or the E/A output pin . In addition the L4981A/B can be disabled grounding the P-UVLO (pin 15) see fig 33.The P-UVLO function has been designed to program the supply thresholds by means of an external divider (see application note for details) but it can be effectively used for this purpose forcing a voltage below the internal reference (1.28V).Besides turning off the driver output stage this method puts the controller in "before start-up" condition and gives the advantage of minimizing the supply consumption of the IC.

Figure 33.