A Classification and Evaluation of Paralleling Methods for Power Supply Modules

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Abstract--There is a fairly large number of methods for paralleling power converters. This paper classifies and examines these paralleling schemes, focusing on the active current-sharing approaches. Based on this classification, some new paralleling schemes can be achieved. Emphasis is placed on discussion and assessment of merits and limitations of these schemes. Finally, the prominent features of the dominant paralleling schemes are verified by simulation of a two-paralleled buck converter system.

1. INTRODUCTION

Generally, the paralleling of power converter modules offers a number of advantages over a single, high-power, centralized power supply. Paralleling of standardized converter modules is an approach that is used widely in distributed power systems for both front-end and load converters [37], [41]. A desirable characteristic of a parallel supply system is that individual converters share the load current equally and stably. Parallel modules are usually non-identical due to finite tolerances in the power stage and control parameters. If special provisions are not made to distribute the load current equally among paralleling modules, then it is possible that one or more units may have an excessive load current. This causes higher thermal stress on specific units and reduces the system reliability [15], [19], [20], [28], [39]-[41], [43].

In order to achieve desirable characteristics when operating converter modules in parallel, a variety of approaches, with different complexity and current-sharing (CS) performance, have been proposed, developed, and analyzed in the past [1]-[58]. However, a comprehensive comparison of these methods is not presented in literature. A successful selection of the paralleling scheme requires a firm understanding of merits and limitations of different paralleling schemes. The paralleling scheme must be selected by taking the complexity, cost, modularity, and reliability into consideration. Various interactions among converter modules should be incorporated into the control design and system integration to ensure stability, reliability and a good dynamic performance.

This paper presents a classification and comparative evaluation of various paralleling methods, focusing on investigation of active current-sharing approaches. Emphasis is placed on discussion and assessment of the merits and limitations of the schemes. Finally, some simulation results for a two-paralleled buck converter system are given.

2. CLASSIFICATION OF PARALLELING SCHEMES

In this paper, paralleling methods are classified into two basic categories from the viewpoint of the operating mechanism to current sharing, i.e., droop methods and active current sharing methods. Figure 1 shows the classification of paralleling schemes. Based on how to get droop features, the droop methods can be further categorized into five types of conducting schemes. For active current-sharing methods, actually, *a conducting scheme consists of a specific control structure and a current-programming_method.* There are three basic control structures from the viewpoint of a current sharing control strategy, namely, inner loop regulation, outer loop regulation and external controller structures. Also there are a number of current-programming schemes among the paralleled modules. Therefore, there are more than ten active current-sharing schemes composed of the control structures and the current-programming schemes.

Table 1 shows some of the active current-sharing schemes formed by three control structures and six current-programming methods. Of these schemes, in particular, the ones with shaded areas are potential new schemes. (AM+OLR) scheme is employed by control chip UC 3907. Moreover, (BACP+ILR) and (BACP+OLR) schemes are also used extensively in the practical parallel system (see detailed description in later section). It should be pointed out that converters employing peak and average current controls under common outer loop have inherent peak and average current-sharing capability. Here we regard them as a special branch only under inner loop regulation structure; thus, they are not included in Table 1.

3. ASSESSMENT OF PARALLELING SCHEMES

There are a number of schemes for paralleling power supply modules. These schemes are described and discussed here, with an attempt made to investigate their principles, origins and applications, highlighting their merits and limitations.

3.1 DROOP SCHEMES

A droop method can be defined as one in which the output voltage droops as the load current is increased. Its operation

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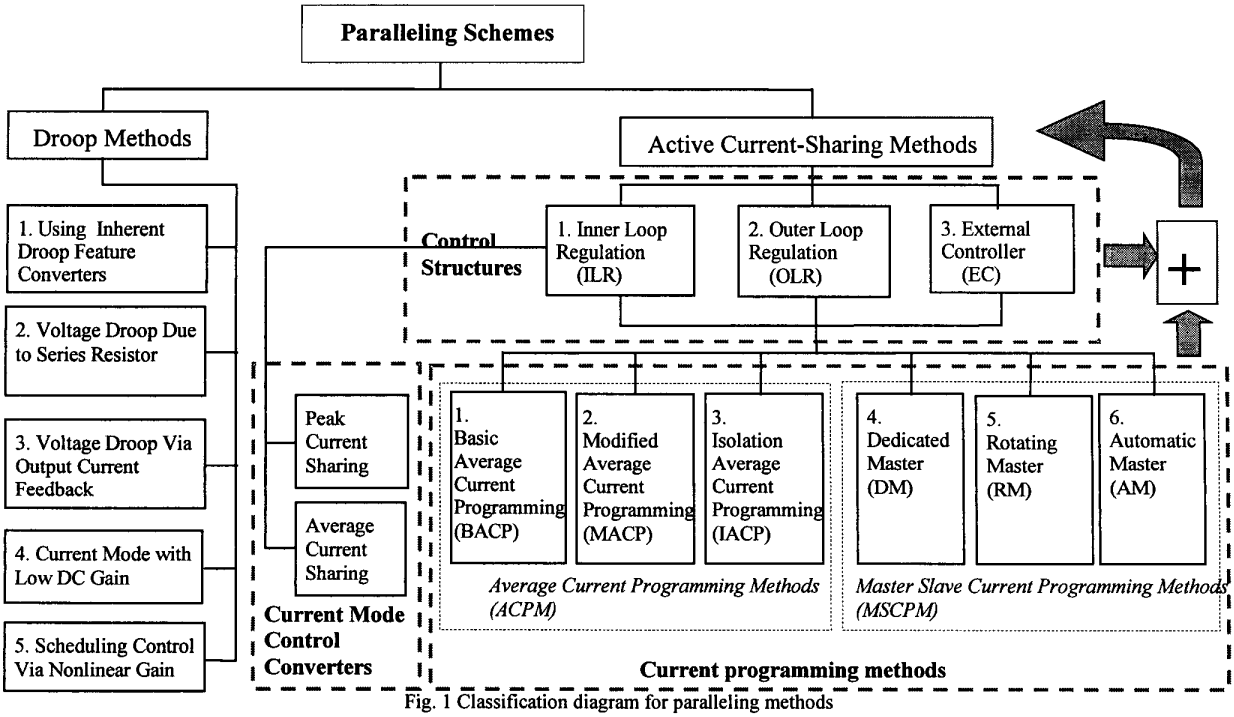

Fig. 1 Classification diagram for paralleling methods

TABLE 1
COMBINED ACTIVE CURRENT-SHARING SCHEMES

Paralleling schemes		Current-programming methods					
		BACP	MACP	IACP	DM	RM	AM
Control structures	ILR	BACP + ILR	MACP + ILR	IACP + ILR	DM + ILR	RM + ILR	AM + ILR
	OLR	BACP + OLR	MACP + OLR	IACP + OLR	DM + OLR	RM + OLR	AM + OLR
	EC	BACP + EC	MACP + EC	IACP + EC	DM + EC	RM + EC	

mechanism is to program output impedance to achieve current sharing among converters. Generally speaking, the better the current sharing, the worse the voltage regulation is for the converters, so the reason conventional power supplies do not share current well is that they are designed to be good voltage sources with a low output resistance. In other words, A converter's current-sharing ability can be determined by its droop characteristic, i.e., the converter's output current versus output voltage.

This family of schemes needs no wire interconnections among control circuits of parallel converters, and so it is actually an open loop technique that individually programs the output impedance of each power supply. This paper presents five possible droop schemes that can be used to parallel power supplies or power converters.

Scheme #1 Using Converters with Inherent Droop Feature

A simple scheme to set up a parallel system is to choose converter modules with a droop feature properly. Some converters, such as buck and boost converters operating in discontinuous inductor current mode, the series resonant converter, and so forth, have inherent load-sharing ability, and probably can be used in a paralleling system without tight regulation requirements [1],[20].

Scheme #2 Voltage Droop Due to Series Resistor

In this paralleling scheme, all of the paralleled supplies have an initial setting that, via a potentiometer, are made almost identical. A resistor is placed in series with the output to provide an IR voltage drop in the output [17],[27].

Obviously, the major disadvantage of this approach is the high power dissapation in the series resistor if the droop in output voltage is large. Because of added power dissipation, this scheme normally is used only for low power linear post-regulators.

Scheme #3 Voltage Droop via Output Current Feedback

In this method a voltage is sensed across a series resistor and used to produce a droop in the output voltage that is proportional to the output current of the supply [17]. A block diagram is shown in Fig. 2. The output droop property can be expressed as:

$$V_o = V_{initial} - I_o \times R_{droop} \quad (1)$$

where R_{droop} is the equivalent series droop resistor and is equal to $H_i(R_1+R_2)/R_2$. $V_{initial}$ represents the equivalent initial value of output voltage and is equal to $V_{ref}(R_1+R_2)/R_2$.

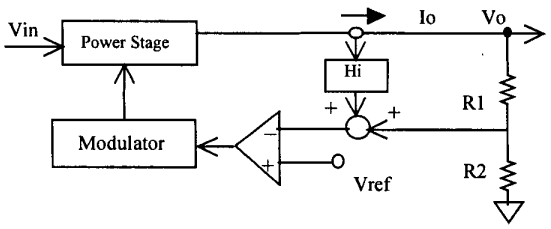

Fig. 2.Voltage droop via output current feedback

Scheme #4 Current Mode with Low DC Gain

This droop scheme is implemented by eliminating the series capacitor (DC isolation capacitor) in the feedback path of the error amplifier of a current-mode supply, namely, not using an integrator in the transfer function. This greatly reduces the DC gain of the error amplifier, thus producing a droop in the output voltage.

A block diagram of the scheme is shown in Fig. 3. The output droop property can be expressed approximately as:

$$V_o = V_{initial} - I_o \times \frac{R_1}{R_f} \times H_i \qquad (3)$$

where H_i is the gain of the current sense circuit, and $V_{initial}$ represents the equivalent initial value of output voltage and is equal to $V_{ref}(1+R_1/R_2+R_1/R_f)$.

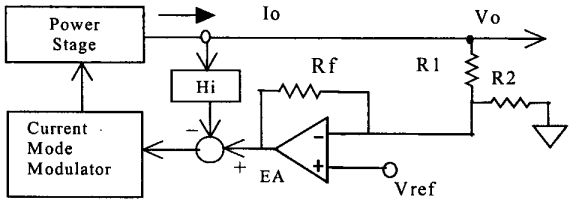

Fig. 3 Current mode with low DC gain

Scheme #5 Scheduling Control Via Nonlinear Gain

This droop scheme is implemented by nonlinear gain scheduling. The block diagram of the scheme is shown in Fig. 4. The total control gain $K=K_1 \times K_2$. the higher the DC gain, K, the worse the current-sharing, and the better the load regulation. Thus, good current-sharing in the required operating range can be scheduled and ensured, particularly in case of heavy load.

The five droop schemes mentioned are described only at the conceptual level. For more details of the output droop characteristics of paralleling DC/DC converter systems, refer to [17],[19],[20],[22],[27],[33],[45].

General features of the droop schemes are summarized as follows:

Advantages:

- easy to implement and expand
- no wire connection among control circuits of converters
- high modularity and reliability.

Disadvantages:

- degrading load regulation to achieve droop characteristics
- poor current-sharing due to open loop for parallel system.

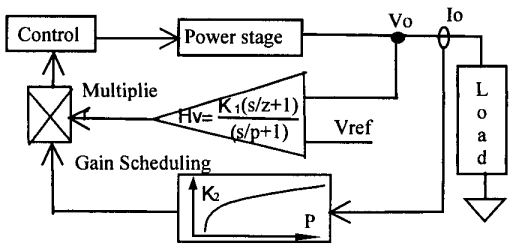

Fig. 4 Scheduling Control Via Nonlinear Gain

3.2 ACTIVE CURRENT-SHARING SCHEMES[**]

An active current sharing scheme is a combination of a specific control structure and a current-programming scheme. Three control structures and six current-programming schemes are analyzed and discussed below. Their merits and limitations are reviewed.

Actually, as for a single converter, it can be deemed that there is an additional control loop with an active current-sharing control scheme, we refer it to as a current-sharing control loop in this paper.

3.2.1 Control Structures for A Paralleling System

According to the operation mechanism of current-sharing in paralleled converters, three basic control structures are summarized below, and their merits and limitations are discussed.

Structure #1 Inner Loop Regulation (ILR)

This control structure implies that reference voltage, voltage feedback and compensator are common. A typical structure of this scheme is shown in Fig. 5 where G(s) is the transfer function of voltage error compensator, and $Z_{c1},\cdots$, and Z_{cn} represent cable impedance. Error signals (V_{se1} and V_{sen}) from a current-programming controller are used to adjust the output of the voltage loop compensator to obtain the appropriate operating control voltage V_{ci}, where $i = 1,2\cdots n$, which feeds the PWM generator of each converter in order to produce the desired current-sharing.

For converters with peak and average current mode control, the current sharing can be achieved by providing the same control reference for the internal current loop of each module. For the peak current control, pulse-by-pulse peak current sharing can be obtained by the use of a fast-acting current loop even in the case of the
mismatch in power stage parameters and no use of current-programming.

Merits and limitations of this control structure are summarized as follows:

Merits:

- stable current-sharing
- precise output voltage regulation.

[**]Although a more detailed review is available, some are not included here due to limited space. Interested readers may contact the authors to obtain related copies.

As a result, output currents of the converters in parallel are in tight control with the fixed outer voltage loop, i.e., sharing error signals do not pass through the voltage loop compensator. Thus it is possible that the overall system response may be more stable and faster than that obtained with outer loop regulation (described in the next section).

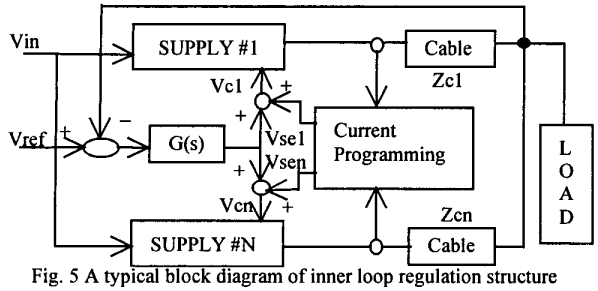

Fig. 5 A typical block diagram of inner loop regulation structure

Limitations:

- degrades the modularity of the system
- poor fault-tolerance.

Each module cannot operate as an individual converter because each has the outer voltage loop in common. Consequently, the fault-tolerance capability for a paralleling system is relatively poor.

Structure #2 Outer Loop Regulation (OLR)

This structure uses current-programming error to adjust the reference of the outer voltage loop until equal load current distribution is achieved. The concept of this control structure is presented graphically in Fig. 6. The key feature of the structure is that each converter module has independent output voltage feedback.

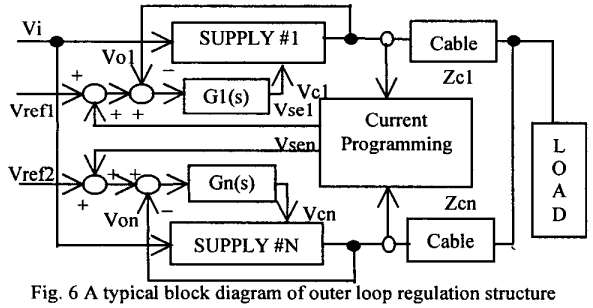

Fig. 6 A typical block diagram of outer loop regulation structure

The advantages and disadvandages of this sharing control structure are summarized as follows:

Advantages:

- good modularity and standardization for manufacturing
- flexibility in system configuration, easy to expand and maintain the system
- excellent fault-tolerance against the failure of any single module.

Disadvantages:

- possibly unstable in transient [18],[48].

For example, the output voltage of a parallel system may become unstable when reference voltages are adjusted by a set of variation (uncertain) sharing error signals.

- limited voltage-feedback gain.

The infinite dc gain of the error amplifier sufficiently amplifies any finite mismatch between the voltage references of converter modules (unavoidable in practice) to cause a severe imbalance in the current level of converter modules. To avoid such a problem, the voltage feedback compensation must have a finite dc gain.

Structure #3 External Controller (EC)

Another alternative structure is to use an external controller to perform the current-sharing [15],[31],[37]. This is achieved by comparing all load sharing signals from the individual power units and adjusting the corresponding feedback control signal to balance the load currents. A typical block diagram of this structure is shown in Fig. 7.

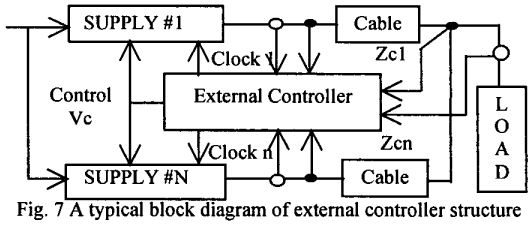

Fig. 7 A typical block diagram of external controller structure

This system performs well but requires an additional controller and multiple connections among the contoller and each supply. In addition, a controller coordinates all converters, so the system reliability could be affected to a certain extent. Once the controller shuts down, the current-sharing situation no longer exists. Also, it may have a severe impact on overall system reliability due to the large number of interconnections and the increased possibility of single-point failure. Because of these reasons, this scheme might have been discarded temporarily in favor of one of the active current-sharing techniques. However, in today's rapid development of distributed power systems, this technique should perhaps be examined in a new light [1].

Merits and limitations of this control structure are summarized as follows:

Merits:

- easy to implement active interleaving.

The control module can simultaneously provide control voltages and clock signals for each module of the paralleling system. Phased clocks can dramatically cut ripples.

- good current sharing and output voltage regulation
- easy to implement failure monitoring
- good chance to fully utilize an existing supervision system.

It may be possible to use a redundant high-level supervisory controller, leaving the individual cells to only manage gating and fault handling. This control mode probably can attain the highest performance because of the possibility of active interleaving.

Disadvantages:

- more interconnections among modules and external controller
- degradation of modularity
- degradation of reliability due to more interconnections and a complicated control.

3.2.2 Current-Programming Schemes

Current-programming (CP) is an important link in an active current sharing scheme. The functions of the current-programming are to communicate control circuits of all paralleled converters, to acquire the current sharing error signal of each module, and then to feed the control circuit of each module by an adjustment amplifier.

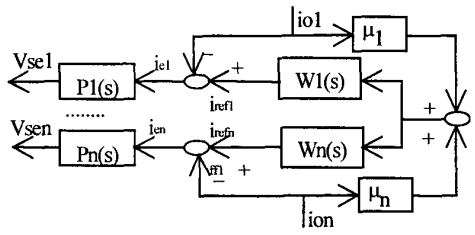

Fig. 8 A unified block diagram for current-programming

Figure 8 shows a unified simplified block diagram that describes current-programming of n converters in parallel, which shows how the current reference signal, i_{refi}, is generated. $P_1(s)$,···and $P_n(s)$ represent transfer fuctions of adjustment amplifiers, μ_1,···and μ_n represent interface links of modules to a common sharing bus. The weighting functions, $W_1(s)$,···and $W_i(s)$ create the reference current signal in proportion to the desired current-sharing ratios. The differences between desired current levels, i_{refi}, and actual output current, i_{oi}, constitute the current error signal, i_{ei}. The desired output current level for each converter is the total current weighted by a function proportional to the desired current-sharing ratio. Therefore, the dc summation of the weighting functions, $W_1(0)$ +··· $+W_2(0)$, shown in Fig. 10, is equal to unity. Also, Fig. 8 is suitable for signal processing for a paralleling system with power modules with different ratings.

Unless otherwise stated, the following description is for the paralleling of power converters with identical capacity.

Average Current-Programming Methods (ACPM)

In Fig. 8, when the functions μ_1 through μ_n are equal to one and the weight function $W_i(s)$ is gain in proportion to the current rating of each converter in a parallel system, we have the "average current-programming method." All converters provide signals proportional to their output currents, which are then weighted and averaged to get a sharing-current reference, i_{ref}, proportional to the average converter output current. In each converter, for example, converter n, the reference i_{refn} is compared to the output current i_{on} of that converter to get a sharing-current error. This error is processed through the adjustment amplifier $P_n(s)$; the product $P_n(s)(i_{refn} - i_{on})$ is used in sharing control to adjust the output voltage of converter n so that its output current is made approximately equal to the weighted average of the output current. All converters are maintained at "approximately" equal output current for the parallel system of identical capacity converter modules.

Scheme #1 Basic Average Current-Programming (BACP)

A typical implementation of the scheme is a patented technique, where each power module's current monitor drives a commonly shared bus via a resistor [16]. The scheme is called basic BACP in this paper, as shown in Fig. 9. The adjusting amplifier will sense, if there is a differential across the resistor, equating to a load current imbalance, and adjust the control loop of the converters accordingly. The sharing bus where all resistors connect represents the average load current contribution. More detailed information can be found in [9],[10],[13],[16],[18],[21],[23],[24],[26],[48],[49],[51].

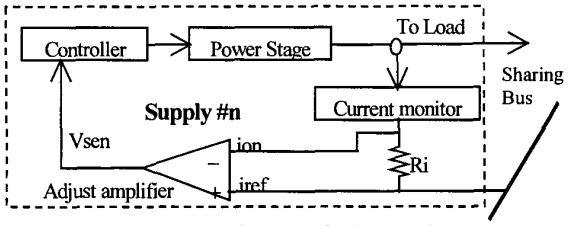

Fig. 9 A typical example for basic BACP

Scheme#2 Modified Average Current-Programming (MACP)

A modified scheme is presented in [7], which does not employ the operational amplifier to generate the current-sharing error. The advantage of this modified scheme is its inherent stability. The main disadvantages mentioned above, however, also can be found in this scheme. Moreover, obvious poor transient response and additional ripples due to mismatching of the R, C parameters, may result in specific application problems.

Scheme #3 Isolation Average Current-Programming (IACP)

Based on the idea of ACPM, an isolation ACP is presented, which is called the "frequency-based current-sharing technique" [3]. It employs the frequency domain method for encoding and communicating current-sharing information to implement galvanic isolation of current-sharing control circuits.

This scheme has significant advantages over existing methods, in particular, in eliminating the galvanic interconnections among module controllers. Thus, single point failure problems can be resolved by this new scheme, so it can be used wherever fault tolerance and high reliability are important to system requirements. Practical implementation and features of the scheme are presented in [5],[11],[58]. A potential problem of this scheme is high cost due to using a complicated circuit and techniques. In other words, this evolved scheme is still in the early development stage; more evaluation and practical design considerations need to be explored further in the future.

BACP is still dominant and is used widely in many practical field applications in the three schemes mentioned above. The advantages and disadvantages of the BACP are summarized below:

Advantages:

- relative stable and precise current sharing
- single interconnection sharing bus
- noise immunity sharing control.

As compared below with the master/slave method, low frequency noise does not cause sharing control failure in this method.

Disadvantages:

- relatively poor reliability
- poor fault-tolerance.

While this scheme performs accurate current sharing, it can result in specific application problems. An example is when a supply runs into a current limit, causing the sharing bus to be loaded down and the output voltage to regulate to the lower adjusting limit. A similar failure mode will exist if any unit on the sharing bus is inoperative. Moreover, it is difficult to make a weighted factor $W_n(s)$ change automatically; otherwise, high-cost, complicated control circuits have to be used.

Master Slave Current-Programming Methods (MSCPM)

Methods of current-programming with the master-slave concept can fall into three schemes according to the approaches of producing the master module: dedicated master, rotating master and automatic master, also called "democratic" master. The operating principle of MSCPM is similar to the ACPM except the current reference i_{ref} in Fig. 8 is simply in proportional to the master module output current.

Scheme #4 Dedicated Master (DM)

In Fig. 8, when one of μ_1 through μ_n is assigned to be one, and the others are zero as well as all $W_i(s)=1$, we get the block diagram of the dedicated master sharing scheme. That is to say, one module is dedicated to be the master; its output current will become the reference for current-sharing (CS) loops of the remaining modules (slaves).

The scheme does provide current sharing and can achieve stable output voltage regulation, but it does not achieve redundancy, since the master failure disables the entire system. Some analysis and discussions are described in references [4],[24],[28],[31][36],[48].

Scheme #5 Rotating Master (RM)

In Fig. 8, when any one of μ_1 through μ_n becomes one in turn and the other conditions are the same as the dedicated master, we have the block diagram of this scheme.

The idea of the rotating master is proposed in reference [35]; it is indeed an advance compared with the dedicated master in the idea of enhancing system reliability. In this scheme, each module has the capability and chance of becoming a master through a specific control logic.

While this scheme improves system reliability, some specific application problems may occur. One possibility is that output voltage might fluctuate because of the continuous exchange of the master module. Another practical problem, obviously, is complicated implementation.

Scheme #6 Automatic Master (AM)

In Fig. 8, when μ_1 through μ_n become an ideal unidirectional rectifier, we get the block diagram of the automatic master. A typical implementation of this scheme is shown in Fig. 10. This scheme automatically selects a module with the highest output current to be the master, and adjusts control signals accordingly in a certain control mode to correct the imbalance of the load current. This scheme is similar to the BACP scheme (Fig. 9) except that the resistor is replaced with an idea diode.

This scheme incorporates some advantages of the average current method and the dedicated master scheme, so it is an improvement over the former two schemes, which are also known as the "democratic current sharing" method in some literature.

In the above mentioned three master-slave schemes, the automatic master method gained popularity among power supply designers and is used widely in practical applications; in particular it is implemented in ICs UC3907 and UC3902 by Unitrode Inc. [1]-[4],[12],[15],[18]. Features of the scheme are summarized as follows:

Merits:

- single interconnection sharing bus
- good fault-tolerance
- easy to expand and modify paralleling system.

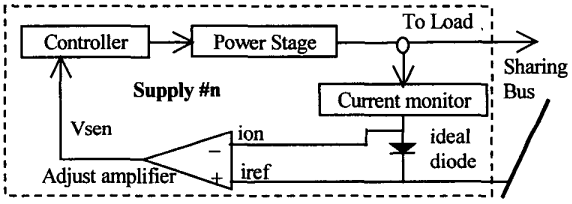

Fig. 10 A typical implementation of automatic master scheme.

Limitations:

- poor transient sharing performances
- possible sharing control failure
- noise sensitive sharing control.

4. SIMULATION EXAMPLES FOR ACTIVE CURRENT-SHARING METHODS

The schematic used for simulation is shown in Fig. 11. The Saber simulator is used to simulate several typical cases. The simulated output voltage and currents are shown in Figs. 12(a) and 12(b), respectively. Figure 12(a) shows excessive output voltage transients due to a step load change while the output is being regulated. From Fig. 12(b), we see that the output currents diverge to significantly different values due to the different equivalent resistances of inductors and cables in two converters, $R_{L1}=0.01\Omega$ and $R_{L1}=0.09\Omega$.

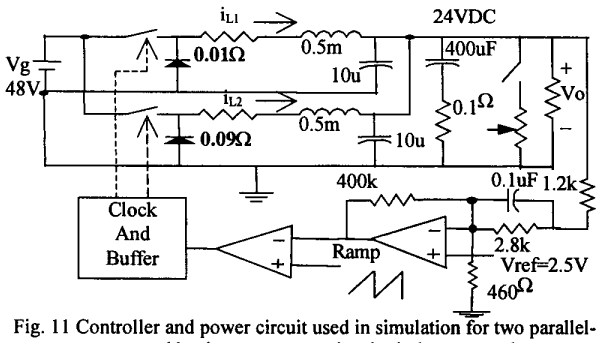

Fig. 11 Controller and power circuit used in simulation for two parallel-connected buck converters under single-loop control.

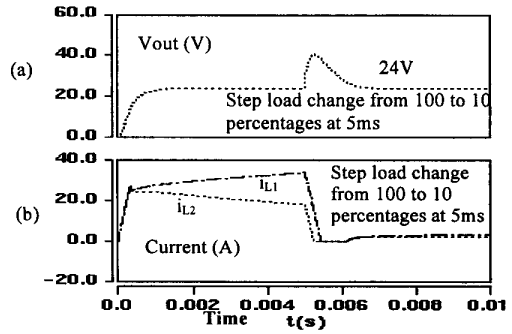

Fig. 12 (a) Output voltage. (b) Output currents of two buck converters under no current-sharing control (Step-load change at t=5ms).

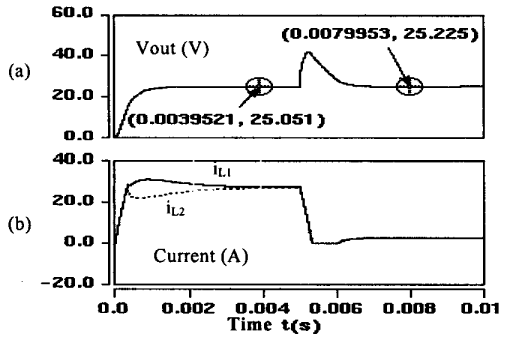

Fig. 13 Simulated results using (AM+OLR) sharing method, i.e., automatic master under outer loop regulation. (a) Output voltage (b) Output current.

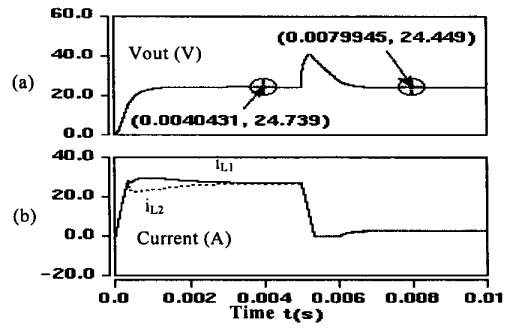

Fig. 14 Simulated results using the (BACP+OLR) sharing method. (a) Output voltage (b) Output current.

It is shown in the following section that the difference between output inductor currents can be reduced significantly by the combined active current sharing schemes proposed by this paper.

These results also illustrate some characteristics of the aforementioned schemes. Comparing Figs. 13 and 14, we can see that the (BACP+OLR) method has better transient sharing characteristics than the (AM+OLR) method. This is because the (AM+OLR) method provides no control for the output current of the master converter, and relatively high output current overshoot during transient. From the comparison of Figs. 13 and 15, we can find that the (AM+ILR) method has more precise output voltage regulation than the (AM+OLR) method; this is because the reference voltage is adjusted in a timely fashion in the (AM+OLR) method, while the reference voltage in the (AM+ILR) method is not affected by the sharing current control loop. In the above-mentioned methods, the (AM+ILR) method has the best overall characteristics, not only in steady-state but also in transient response. But its reliability may be affected by the common outer loop.

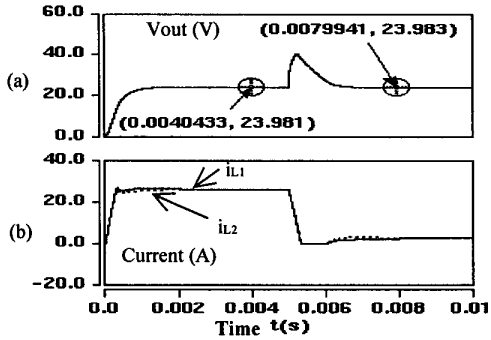

Fig. 15 Simulated results using the (AM+ILR) sharing method. (a) Output voltage (b) Output current.

5. CONCLUSIONS

This paper presents a classification of paralleling methods for power supply modules. Based on this classification, some new active current-sharing schemes can be obtained by proper combination of the sharing control structures and the current-programming methods listed in this paper. For instance, a combination of the inner regulation sharing control structure and current-programming scheme of an automatic master can achieve some advantages.

This paper also gives a comprehensive review of paralleling schemes for power supply modules. Although it is impossible to cover each aspect of each scheme in one paper, we tried to present most of the methods and their issues that we deem are of common interest to practicing engineers in order to give a general picture of this field, while still including a few in-depth discussions on several special topics to provide some insights into paralleling system design.

In other words, each paralleling scheme has its own merits and limitations, and each application has different criteria.

Some schemes and their designs of paralleling systems still need to be assessed in more detail in the future.

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