Conducted EMI Issues in a 600-W Single-Phase Boost PFC Design

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Abstract—This paper presents the results of experimental activity concerned with the development of a 600-W boost power-factor corrector (PFC) complying with the EMC standards for conducted EMI in the 150-kHz-30-MHz range. In order to accomplish this task, different circuit design and layout solutions are taken into account and their effect on the conducted EMI behavior of the converter is experimentally evaluated. Common-mode and differential-mode switching noise, together with input filters' design and topology and with the printed circuit board layout (in terms of track length and spacing, ground and shielding planes, etc.) are the key aspects which have been considered. In particular, the paper reports the conducted EMI measurements for different filter capacitor placements and values, for different power switch drive circuits, together with several other provisions which have turned out to be decisive in the reduction of the generated EMI.

Index Terms—Conducted EMI, power-factor-corrector rectifier, printed circuit board layout.

I. INTRODUCTION

HE employment of boost power-factor correctors (PFC's) in order to comply with the IEC 1000-3-2 low-frequency EMC standard [1]-[3] is becoming more and more ordinary in a large variety of industrial applications of switch-mode power supplies (SMPS's). This solution, however, increases the conducted interference generation of the power supply in the high-frequency range. As a consequence, while the low-frequency harmonic content of the current driven from the utility grid is normally well controlled and compliant with the aforementioned IEC standard, the high-frequency currents generated by the converter on the grid may be beyond the corresponding standard limits [4]-[7]. To avoid this, it is very important to properly design the EMI filters and the circuit layout so as to minimize the effects of the switching converter on the line pollution. This paper discusses the design of a 600-W boost PFC complying with the EMC standards for conducted EMI in the 150-kHz-30-MHz range [8]. Different circuit design and layout solutions are taken into account and their effect on the conducted EMI behavior of the converter is experimentally evaluated. Common-mode and differential-mode switching noise, together with input filters' design and topology and with

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the printed circuit board (PCB) layout (in terms of track length and spacing, ground and shielding planes, etc.) are the key aspects which have been considered. In particular, the paper reports the conducted EMI measurements for different filter capacitor placements and values, different power switch drive circuits, together with several other provisions, which have turned out to be decisive in reducing the conducted EMI level of the converter [9]. By means of this design example, which employes two-layer PCB technology, the paper also shows that the application of the theoretically derivable EMC basic design rules, which, in principle, should guarantee the limitation of the EMI in a switching power converter, may, in some cases, become partially ineffective because of second-order effects (e.g., resonances, component parasitics, connections). The experimental results illustrate these unexpected outcomings and the validity of the adopted provisions which allow one to design a fully compliant power supply.

II. BASIC SCHEME OF THE CONVERTER

Fig. 1 shows the basic scheme of the considered boost PFC. The ratings of the converter are reported in Table I. These represent the typical characteristics of a PFC designed for a large variety of applications (e.g., telecom applications). A conventional and simple design procedure can be adopted to derive the necessary passive components' values, required to guarantee the continuous conduction mode of operation for the converter practically during the whole line period and a suitable output voltage ripple level. Also, the selection of the required switch and diode is almost straightforward, given the current and voltage stresses, which are easily determined analyzing the converter's typical waveforms. The resulting list of adopted components is reported in Table II.

III. CONSIDERATIONS ON THE POWER STAGE DESIGN

The considered topology is simple and well known [10]–[13]. However, when it comes to EMI control, it is necessary to adopt particular care in the definition of the layout of the power stage [14]–[18].

Of course, the main sources of EM noise can be easily identified in the power switch and diode. The reduction of the wire lengths for the current return paths and for the high dv/dt circuit branches, together with the reduction of the areas embraced by high di/dt loops, as shown in Fig. 2, appear to be fundamental provisions. It is, therefore, fundamental that the area between the power switch and the two high-frequency bypass capacitors, which are used to drain the current pulses generated during the

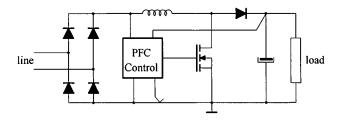


Fig. 1. Basic scheme of the boost PFC.

TABLE I CONVERTER RATINGS

Input voltage (RMS)	90-260 V
Output power	600 W
Output voltage	380 V
Switching Frequency	70 kHz

TABLE II
MAIN CONVERTER COMPONENTS

Output capacitor	680 μF
Inductor	600 μΗ
Mosfet	IRFP450
Diode	RURP1560
Controller IC	L4981A

commutations, is made as small as possible. Indeed, if the emitting area is small, the efficiency of the equivalent loop antenna, indicated in Fig. 2, is small, too. As a consequence, the amount of radiated noise which can couple with the circuit conductors, thus becoming conducted noise, also will be minimized. This is the reason why, even if the major concern of this design is the minimization of conducted EM noise, it is important to reduce the efficiency of the radiating sources as much as possible. In order to do that, another important practical provision is to twist, if possible, all the critical tracks of the PCB, and wind the wire of the toroidal inductor used in the converter power stage as shown in Fig. 3. This keeps the emitting areas as small as possible (introducing also a mutual cancellation of the fluxes), without compelling one to excessively shrink the magnetics and the size of the PCB, which is normally difficult and sometimes impossible.

All of these considerations have a quite relevant effect on the design of the PCB of the converter. As shown in the upper part of Fig. 4, which represents the solder layer of the PCB, the tracks between the high frequency bypass capacitors and the switching components are kept as short as possible and twisted according to what has been sketched in Fig. 3. Moreover, this provision helps to extend the effectiveness of the capacitive filter to higher frequencies, by allowing one to increase the frequency of the resonance between the capacitors and the track stray inductance as much as possible. In order to evaluate this frequency, the total stray inductance of the switching loop can be estimated to be about 1 nH/mm (diode and capacitor lead distance must be included in the computation).

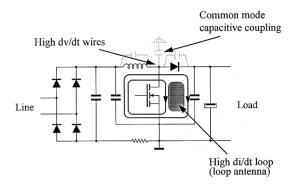


Fig. 2. Critical points of the circuit for EMI generation.

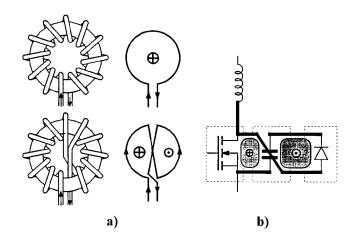


Fig. 3. Reduction of radiating areas by means of twisted current paths (a) in the toroidal inductor and (b) in the tracks of the PCB.

Observing the PCB layout given in Fig. 4, it is possible to see that the track connected to the power switch drain (the central lead of the MOSFET), which exhibits very fast voltage variations during the switch commutations, is kept very short and shielded by means of two constant voltage tracks ($+V_{\rm out}$ and $-V_{\rm out}$) and the ground-connected converter heat sink on the solder layer, and a shield plane connected to ground on the component layer, so as to minimize the generation of radiated EMI.

Also, the gate circuit, which exhibits an high peak current, must be accurately designed according to the previously discussed guidelines. As already mentioned, the key factor is the area embraced by the circuit which must be as small as possible. This is particularly critical when it comes to the insertion of a suitably designed *RC* snubber circuit. The snubber is highly recommended mainly to slow down the MOSFET turn-on, thus reducing the power diode recovery current. As a consequence, the turn-on peak current in the MOSFET is also reduced and, even if the switching time is increased, the converter efficiency is not heavily affected. Moreover, any ringing in the gate circuit can be greatly amplified in the drain; therefore, the adoption of the snubber is advantageous also to damp such oscillations. The effects of this provision will be illustrated by experimental waveforms.

Finally, the control circuit must be effectively protected against the disturbances by reducing the length of the sensitive tracks as much as possible. This is particularly important for

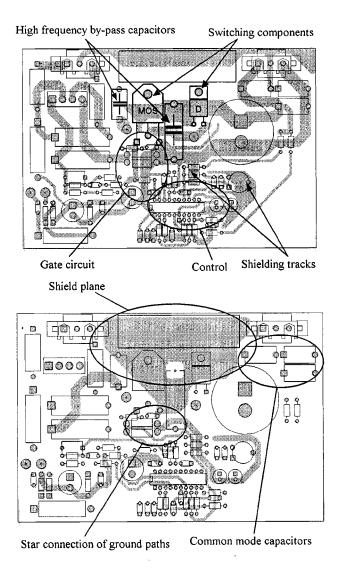


Fig. 4. PCB of the converter: solder layer (top) and component layer (bottom). The size of the board is $150~\rm mm\times100~mm$.

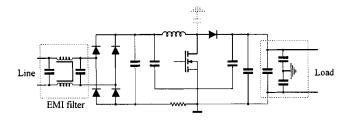


Fig. 5. Schematic of the converter including input and output EMI filters.

the analog inputs of the control implementing the feedback loops for the regulation of the output voltage and input current. As shown in Fig. 4, the corresponding tracks must be short and shielded by means of tracks exhibiting a stable voltage level and a low impedance to ground.

In the component layer of the converter's PCB, which is shown in the bottom part of Fig. 4, a shield plane is implemented which extends under the power switching components and is connected to ground in a single point which is the MOSFET source. It is important to notice that this is the center

TABLE III

MAXIMUM EXPECTED VOLTAGE NOISE DERIVED FROM CURRENT RIPPLE
HARMONIC COMPONENTS

Harmonic	Frequency	Voltage noise	Voltage noise	
Order		(not filtered)	(filtered)	
1	70 kHz	153 dB μV	87 dB μV	
2	140 kHz	141 dB μV	57 dB μV	
3	210 kHz	$134\ dB\ \mu V$	$40~dB~\mu V$	
4	280 kHz	$128~dB~\mu V$	$26~dB~\mu V$	
5	350 kHz	$127~\text{dB}~\mu\text{V}$	$19dB\mu V$	
6	420 kHz	125 dB μV	9 dB μV	

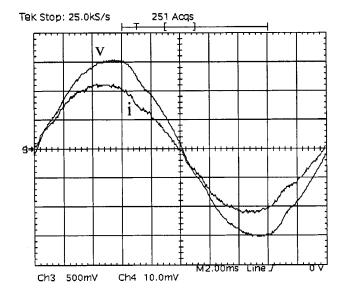


Fig. 6. Line voltage (100 V/div) and current (2 A/div). Horizontal scale: 2 ms/div.

point of a single star connection of the ground tracks, needed to avoid ground loops involving sensitive parts of the circuit (control circuit, gate circuit).

The design of the power stage can be completed by determining the common mode and differential mode input filters [15], depicted in Fig. 5, which represents the complete converter circuit. The input filter for the differential mode noise, which is a third-order filter, can be designed calculating the maximum value of each harmonic component of the current ripple. The current ripple maximum amplitude is given by

$$\Delta I_{\text{max}} = \frac{V_{\text{out}}}{8f_s L} \cong 1.13 \text{ A.}$$
 (1)

Assuming the ripple waveform to be triangular and varying the duty cycle, it is possible to find the maximum amplitudes of the harmonic ripple components which, of course, take place at different duty-cycle values. In order to design the filter, we assume that the input current ripple flows through the line impedance (100 Ω), which is actually the equivalent differential mode impedance of the line impedance stabilizing network (LISN) requested by the standards. The expected noise amplitude, calculated at different harmonic frequencies without the input filter, is reported in the third column of Table III.

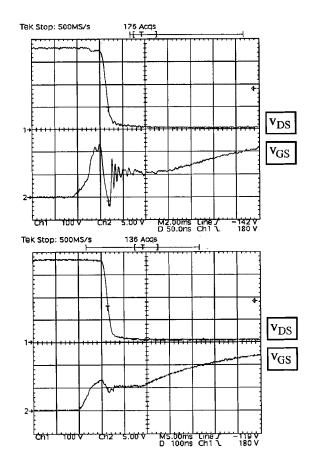


Fig. 7. Gate circuit snubber effect at turn-on. Top: turn-on without snubber ($v_{\rm DS}=100~{\rm V/div}; v_{\rm GS}=5~{\rm V/div};$ horizontal scale: 50 ns/div). Bottom: turn-on with R-C snubber ($v_{\rm DS}=100~{\rm V/div}; v_{\rm GS}=5~{\rm V/div};$ horizontal scale: 100 ns/div).

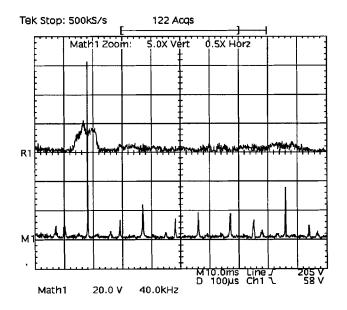


Fig. 8. Switching frequency modulation effect on $v_{\rm DS}$ voltage spectrum. Upper trace: modulation on. Lower trace: modulation off.

Based on these values, it is possible to determine the required filter attenuation to comply with the standard. The attenuation must be suitably oversized (at least 10 dB μ V) to cope with

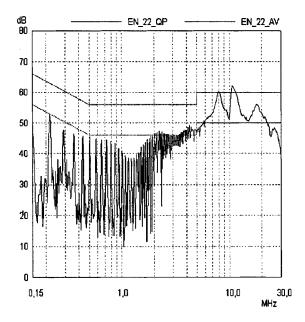


Fig. 9. Conducted noise for the boost PFC (peak measurement).

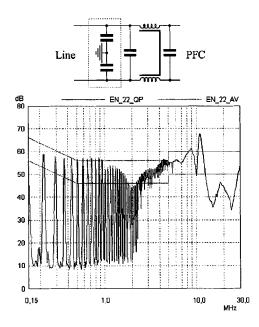


Fig. 10. Effects of additional common-mode capacitive input filter insertion (peak measurement).

possible resonances due to circuit parasitics and with the additional contribution of the common mode component of the conducted noise. Considering again the 100- Ω load for the filter, it is then possible to choose the values of the differential mode inductors and of the capacitors of the filter. A standard common-mode inductive filter ($L_{\rm cm}=6.8\,{\rm mH}$) has been employed, which presents a value of the differential mode inductance $L_{\rm dm}=70~\mu{\rm H}$. The value of the line side filter capacitor is consequentely selected to be equal to 1 $\mu{\rm F}$, while that of the rectifier side capacitor is 2 $\mu{\rm F}$ split across the diode bridge rectifier. Expected filtered noise is then given in the fourth column of Table III.

It is worth noting that the switching frequency has been selected so as to have the first and second harmonic component

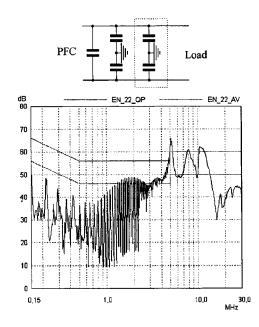


Fig. 11. Effects of additional common-mode capacitive output filter insertion (peak measurement).

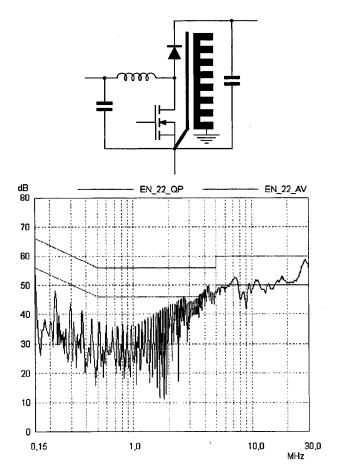


Fig. 12. Effects of shield insertion between MOSFET and heat sink. The shield is connected to the MOSFET source (peak measurement).

of the ripple below the lower frequency considered by the standards [4], [5], thus reducing the filter requirements.

Lastly, as shown in Fig. 5, a common-mode capacitive filter is connected to the output side of the converter, that is as close as

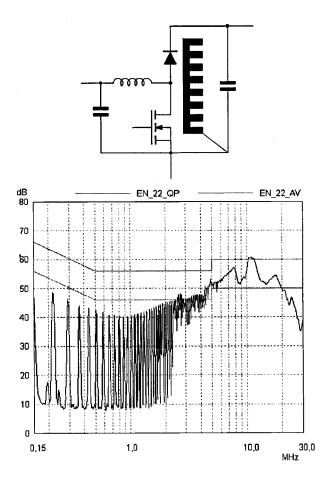


Fig. 13. Effects of heat-sink connection to the negative voltage rail not close to the MOSFET source (peak measurement).

possible to the major source of common-mode noise. For this reason, the filter capacitors are placed on the converter PCB (see Fig. 4). Their value, which must be lower than a given limit for safety reasons, depends on the parasitic capacitance of the circuit layout and, in this prototype, has been selected to be 3.3 nF.

Another important factor in reducing the generation of EMI in a switching converter is the modulation of the switching frequency [19], [20]. In developing the prototype, the shifting of the switching frequency has been simply implemented by adding to the ramp generator circuit of the controller a periodic signal derived from the rectified input voltage. In this way the modulation frequency is no longer fixed, but is modulated at 100 Hz around its nominal value (70 kHz). It is worth noting that the disturbance signal is added to the ramp generator so as to get the minimum switching frequency when the commutated current is maximum, thus obtaining also a little improvement in the converter efficiency.

IV. EXPERIMENTAL TESTS ON THE PROTOTYPE

The converter prototype has been extensively tested to reveal potential sources of EMI and to test possible solutions before the final measurements have been done. As expected, the low-frequency behavior of the PFC is very good, as can be seen in Fig. 6, where the good proportionality between line current and voltage can be appreciated. Fig. 7 describes the effect of the

snubber adopted for the gate circuit. As can be seen, the insertion of the snubber reduces the speed of the commutation and the $v_{\rm GS}$ voltage ringing at turn-on (note that the time base is different for the upper and lower parts of Fig. 7). Indeed, as shown in the upper part of Fig. 7, the $v_{\rm GPS}$ voltage peak corresponding to the conduction of power diode recovery current (observe also the $v_{\rm DS}$ voltage drop during this phase) summed to the inductor current, is almost totally removed in the bottom figure, where the gate voltage sets to the level corresponding to the inductor current without appreciable ringing. This, as will be shown in the following, strongly improves the high-frequency behavior of the converter.

The effect of the previously described switching frequency modulation is shown in Fig. 8, where the $v_{\rm DS}$ voltage spectrum is depicted. As can be seen, the effect of the switching frequency modulation is to modify the structure of the signal's spectrum. As expected, the spectrum is no longer composed of definite lines located at the multiples of the switching frequency, but is made up of large and flat bands, the biggest centered around the nominal switching frequency. The harmonics of the switching frequency are, indeed, almost totally eliminated. This turns out in a very relevant improvement of the high-frequency behavior of the converter.

V. EMI MEASUREMENTS

The developed boost PFC, as schematically depicted in Fig. 5, has been tested according to the requirements of the EMC standards, which regulate the conducted EMI levels for these kinds of electronic devices [4]–[8]. As required, the converter has been connected to a stabilized voltage source through an LISN, and spectra of the input current have been measured in the range from 150 kHz to 30 MHz under different conditions. The result of the first test on the converter is shown in Fig. 9. As can be seen, while the converter's behavior at low frequencies is pretty good, there is an excessive high-frequency content in the current spectrum. As can be noted, the low-frequency part (up to 1 MHz) of the noise spectrum is made of multiples of the switching frequency and is mainly differential mode noise. Its amplitude decreases with frequency thanks to the adopted differential mode filter. Instead, in the remaining part of the spectrum, the noise, which tends to increase with the frequency, is mainly common mode.

Adding a common-mode capacitive filter at the converter's input does not improve the situation as expected, because, as Fig. 10 shows, the differential noise increases. In fact, due to the circuit unsymmetry determined by the asymmetrical location of the boost inductor, the increased input current flows mainly in the input wire which does not include the inductor. This contributes to a differential mode current, thus worsening the low-frequency performance of the converter. Moreover, the high-frequency behavior is modified by the resonance between the common-mode capacitors at the converter input and output and the stray inductance of their connection (about 50 mm). Finally, the increased input current could possibly saturate the magnetic core of the input inductor, thus reducing the filter effectiveness.

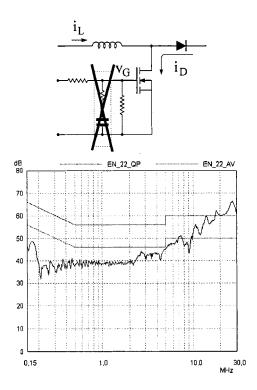


Fig. 14. Effects of gate snubber disconnection (diode reverse recovery occurs) with switching frequency modulation (peak measurement).

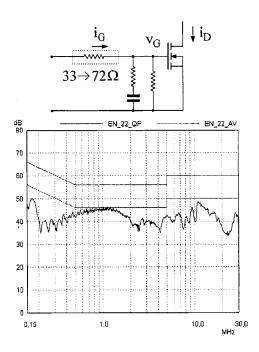


Fig. 15. Effects of gate series resistance increase with switching frequency modulation (peak measurement).

To further confirm this interpretation of the measurements, the additional common-mode filter is moved to the converter's output, in parallel with the one already located there. This determines a better low-frequency behavior, since more common-mode current can now circulate on the converter output side without affecting the LISN, but also a further worsening of the high-frequency part of the spectrum because of the resonances of the newly inserted filter with the one

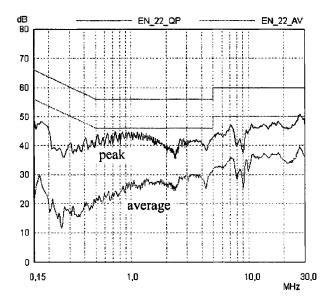


Fig. 16. Final peak and average conducted noise measurements.

already present on board and with the stray inductances of the connections, as shown in Fig. 11. This implies that it is not always recommendable to put more capacitive filters in parallel, as is often done in practice, unless it is possible to keep the length of the connections very short and avoid the resonances, which strongly limit the effectiveness of the resulting combined filter.

To improve the system's performance at high frequency, a shield connected to the MOSFET source terminal is inserted between the switch and the heat sink. As Fig. 12 shows, this provision reduces the common-mode noise and considerably improves both the low- and the high-frequency behavior of the converter because the capacitive currents coupled to the drain can now directly flow through the source without affecting the LISN. The shielding action introduced by this solution allows to reduce also the high-frequency noise, but it is necessary that the connection of the shield is done very close to the source terminal of the MOSFET. An alternative solution is tested in Fig. 13, where the connection of the heat sink to the negative rail is considered. The heat sink acts again like a shield for the whole circuit, considerably reducing the noise level in the low-frequency range. Because of the length of the connection, the effectiveness of this shielding action partially worsens in the high-frequency range. A clear drawback to this provision is that the heat sink is no longer galvanically isolated from the circuit. Moreover, the converter radiated noise tends to increase because of the large heat-sink surface.

To verify the effect of the R–C snubber adopted for the gate circuit of the power MOSFET, a spectrum measurement is performed disconnecting it from the gate, while adopting the frequency modulation technique which was previously described. As is shown in Fig. 14, the snubber disconnection determines a considerable worsening of the high-frequency part of the spectrum, which is due to the steeper transition of the $v_{\rm DS}$ voltage, which takes place at the snubber disconnection, and to the diode recovery current peak in the switch. To confirm this, the series gate resistor has been increased, further reducing the speed of

the MOSFET commutations. As shown by Fig. 15, the high-frequency part of the spectrum is improved as expected, while the low-frequency behavior of the converter is almost unchanged.

Finally, the combined action of the switching frequency modulation technique and the gate snubber circuit is shown in Fig. 16. This reports both the peak and the average measured conducted noise and represents the final setup measurements for the converter, including all the solutions which have been discussed throughout the paper. As can be seen, the low-frequency part of the spectrum is greatly improved by the adoption of the switching frequency modulation, especially in the average noise measurement. In conclusion, Fig. 16 shows how the adopted solutions allow one to achieve the full compliance of the converter conducted emission with the considered standards.

VI. CONCLUSION

This paper has presented the development of a 600-W boost PFC compliant with the high-frequency conducted EMI limits set by the EN50081 standard. Different design options were considered and experimentally tested. The effectiveness of some particular provisions, such as the snubber gate circuit or the modulation of the switching frequency, in reducing the conducted noise, were clearly demonstrated by a complete set of EMI measurements.

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