Quasi-ZVS Active Auxiliary Commutation Circuit for Two Switches Forward Converter

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Abstract: This paper presents a family of single-ended converters that adequately designed and commanded can perform ZVS turn-off and turn-on with a value near to zero namely Quasi-ZVS (QZVS) at main switches. The auxiliary circuit presents low reactive energy and is composed of one inductor, one diode and one switch, which operate with ZCS. To demonstrate the feasibility of the proposed technique, it is applied to a two switches forward converter. It is not necessary the use of a third winding in the transformer neither auxiliary Voltage sources to achieve soft switching. The implementation is possible due to the use of an appropriate command, different than it is used conventionally in two switches forward converters. Complete analysis of the operation stages, as well as the design procedures for the correct operation of the converter are presented. Experimental results obtained from a prototype of 250W/48V@100kHz demonstrate the feasibility of this Active Auxiliary Commutation Circuit (AACC) applied to two switches forward converter. Furthermore, a new concept of switching is introduced, where the main switches commutate with QZVS.

I. Introduction

A great number of researchers have concentrated efforts to obtain converters with low commutation losses. As a result, converters operating with zero voltage and/or current switching have been exhaustively studied to reduce the drawbacks of hard commutation.

Hard commutation losses are mainly linked to three factors: the reverse recovery current of diodes; the discharge of the energy stored in capacitors parallel to the switch (specially in MOSFETs); the simultaneous occurrence of voltage and current on the switch during the commutation process.

The effects associated to these three factors are minimized by the use of zero voltage switching. However, some circuits do not operate with ZVS in all operation conditions. Even if the voltage across the switch do not reaches zero, an improvement of the converter performance can be obtained, by using auxiliary circuits that reduce the voltage to values near to zero. This is the basic principle of Quasi-ZVS (QZVS): to reduce the voltage across the switch to a value as near to zero as possible.

The QZVS occurs when there is not enough energy available to reset the snubbers capacitors. The use of auxiliary circuits with low cost and low reactive energy is the main feature of QZVS.

II. The Quasi-ZVS Single-ended Family

In this section is presented the QZVS single-ended family of non-isolated (boost, buck, buck-boost, SEPIC, zeta and cúk) and isolated (flyback, forward and two switches forward) converters. The basic converters of this family are presented in Fig. 1, and the state planes of these converters are presented in Fig. 3. A family with characteristics similar to the presented one was introduced in [7] with ZVS operation. However, under certain operating conditions, ZVS is not obtained. Anyway, with an appropriate design, the commutations can occur with QZVS.

The presented converters allow QZVS in continuous conduction mode (CCM), discontinuous conduction mode (CCM) and critical conduction mode (CM). This can be seen

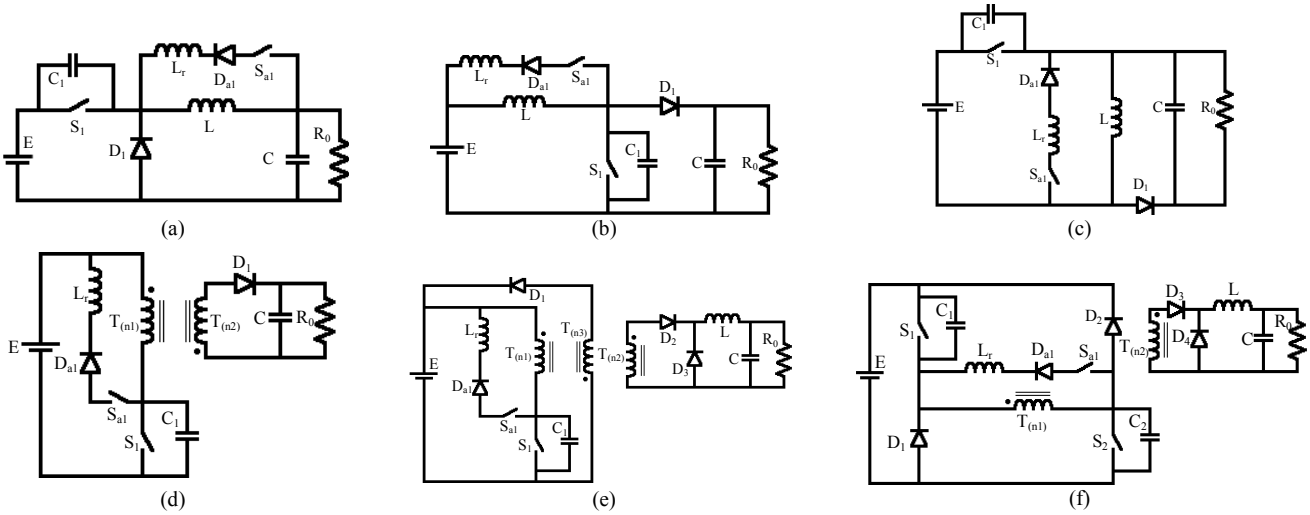


Fig. 1 – Quasi-ZVS family: (a) Buck; (b) Boost; (c) Buck-Boost; (d) Flyback; (e) Forward; (f) Two switches Forward.

in the state plane of the buck converter depicted in Fig. 2. When operating in CCM, the auxiliary circuit presents the highest reactive energy. On the other hand, in DCM the auxiliary circuit presents less reactive energy, but the commutation occurs with higher voltage level (see Fig. 2). Operating in CM the switches commutate as near of zero as possible with less reactive energy than in CCM. As a result of these features, the CM is the most adequate operation mode, in the point of view of the auxiliary switches.

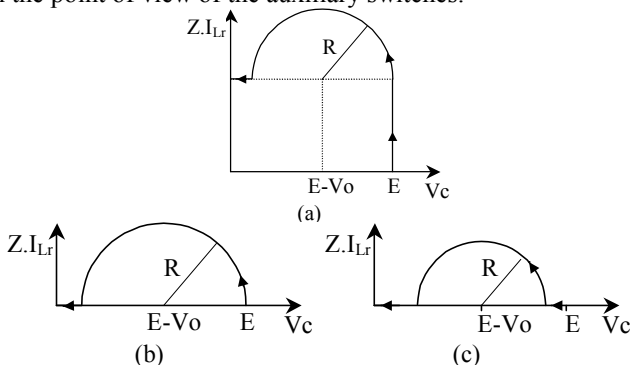


Fig. 2 – State planes of QZVS buck converter: (a) CCM; (b) CM; (c) DCM.

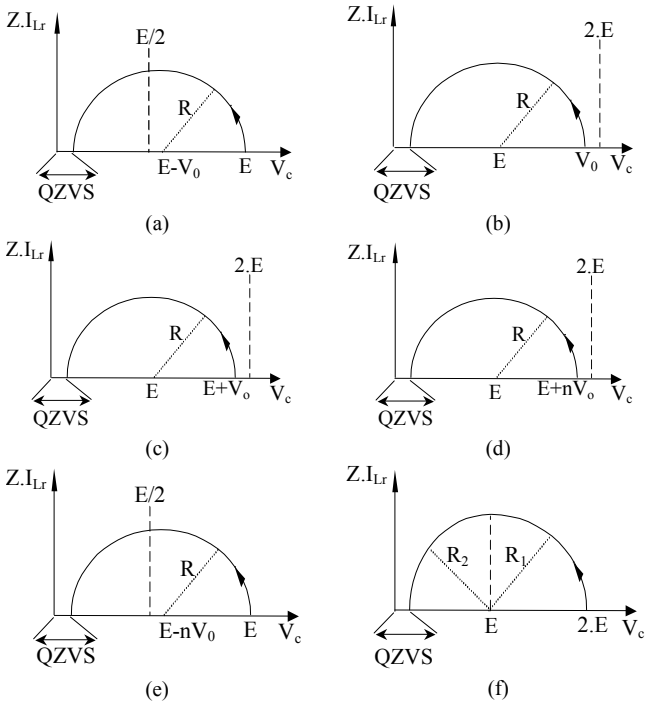


Fig. 3 – State plane of the QZVS family basic converters: (a) Buck; (b) Boost; (c) Buck-boost; (c) Flyback; (d) Forward; (e) Two Switches Forward.

For all conduction modes there are certain conditions for ZVS and QZVS operation. Such conditions are given in Table I.

In the following section will be presented the operation principle of a QZVS two switches forward converter. Soft commutation is achieved at all semiconductor devices. ZCS is obtained at auxiliary switch while main switches turn-off with ZVS and turn-on with Quasi-ZVS.

TABLE I: LIMITS BETWEEN ZVS AND QZVS.

Converter	ZVS	QZVS
Buck	Vo ≥ E/2	Vo < E/2
Boost	Vo ≥ 2.E	Vo < 2.E
Buck-Boost	Vo≥ E	Vo < E
Flyback	n.Vo ≥ 2.E	n.Vo < 2.E
Forward	n.Vo ≥ E/2	n.Vo < E/2
Two Switches Forward	Not possible	Possible

III. THE QZVS TWO SWITCHES FORWARD CONVERTER

Fig.4 presents the two switches forward converter with the AACC. This converter is composed of two main switches (S_1, S_2), two main diodes (D_1, D_2), one transformer (T_1(N1:N2)), two rectifier diodes (D_3, D_4) and two capacitors (C_1, C_2). The inductor L_d represents the leakage inductance of the transformer. The auxiliary circuit is composed of one resonant inductor L_r, one auxiliary switch S_{a1} and one diode D_{a1}.

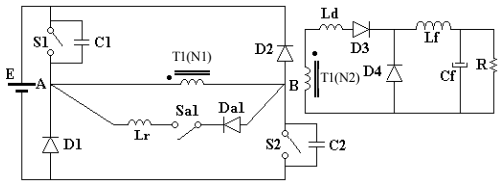


Fig. 4 – Proposed QZVS two switches forward converter.

For the appropriate operation of the auxiliary circuit, it is required that the switches operate with a command signal as shown in Fig. 5(b), different of the conventional one depicted in Fig. 5(a).

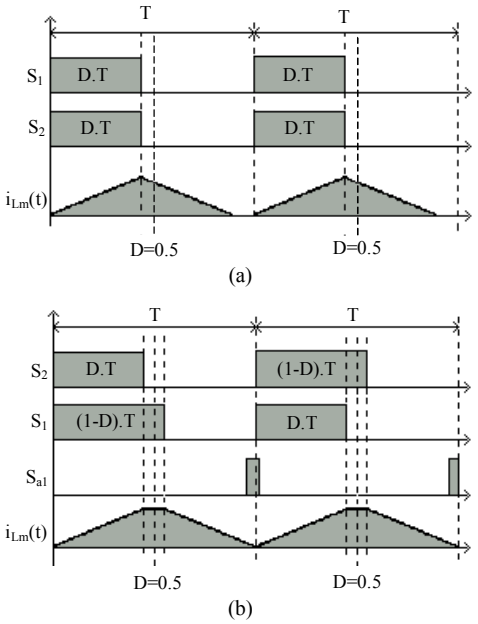


Fig. 5 – Switch gate signals and transformer magnetizing inductor current: (a) Conventional logic; (b) Proposed logic.

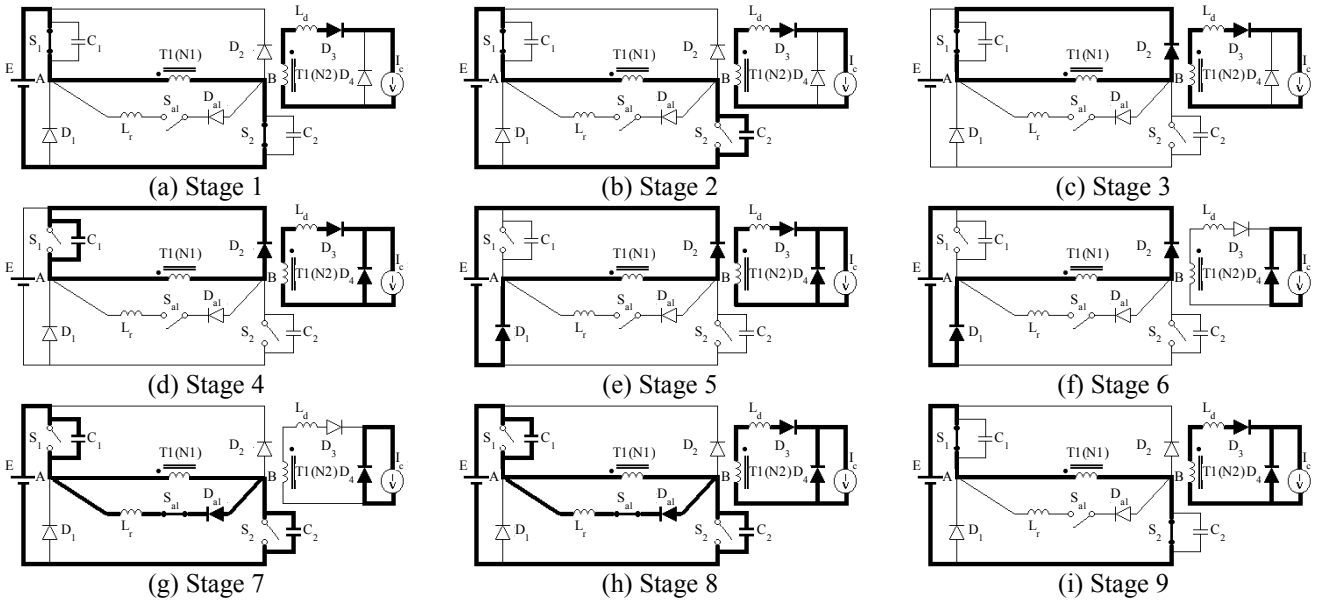


Fig. 6 – Operation stages of the proposed two switches forward converter.

It can be seen that the use of the proposed command does not modify the power transfer relation of the forward converter with two switches. It only introduces a delay time in the demagnetization process of the transformer.

In the remainder part of this section, the nine stages of the proposed converter for one operation cycle are presented. To simplify the analysis, the following assumptions are made: (i) all components are considered as ideal; (ii) the transformer is represented by leakage (L_d) and magnetizing (L_m) inductances; (iii) the output filter and the load are substituted by an ideal current source. The circuit for each stage is depicted in Fig. 6.

Stage 1 (t_0-t_1): It is initially considered that the current flowing through L_d is equal to the load current. Switches S_1 and S_2 are conducting. The dc voltage source E transfers energy to the load through S_1, T_1(N1) and S_2 in the primary side, as well as through T_1(N2), L_d and D_3 in the secondary side. The auxiliary switch S_{a1} is off. The transformer magnetizing current increases linearly due to the presence of the voltage source E across the transformer. The current through T_1 is the sum of the load current (I_{Load}) and the magnetizing current $i_{Lm}(t)$.

Stage 2 (t_1-t_2): At t_1, switch S_2 is turned off. The voltage across capacitor C_2 increases in a linear form due to the load current and due to the magnetizing current. In this way, switch S_2 is turned off with ZVS.

Stage 3 (t_2-t_3): At t_2, the voltage across capacitor C_2 reaches E Volts, and diode D_2 conducts. Transformer magnetizing current and load current freewheels through D_2 and S_1.

Stage 4 (t_3-t_4): At t_3, switch S_1 is turned off with ZVS. It starts the resonance among C_1, L_m and L_d, where the current through inductors L_d and L_m decrease and the voltage across C_1 increases. During this stage the load current is diverted from diode D_3 and the current through diode D_4 rises.

Stage 5 (t_4-t_5): At t_4 the voltage across capacitor C_1 reaches E Volts and diode D_1 conducts. It is applied –E Volts across the transformers and the magnetizing current $i_{Lm}(t)$ decreases linearly. In the secondary side, L_d inductor current decreases linearly.

Stage 6 (t_5-t_6): At t_5, inductor L_d current reaches zero and diode D_3 turns-off. The load current flows through diode D_4.

Stage 7 (t_6-t_7): At t_6, the magnetizing current $i_{Lm}(t)$ reaches zero and the auxiliary switch S_{a1} is turned on (with ZCS due to the presence of inductor Lr). It starts the resonance among the energy in capacitors C_1 and C_2 with the one in inductor L_r.

Stage 8 (t_7-t_8): At t_7, the voltages across both capacitors C_1 and C_2 are E/2 Volts. From this instant, a positive voltage is applied across the transformer, allowing diode D_3 to conduct. Unlike previous stage, the resonance process occurs among capacitors C_1 and C_2 and inductors L_r and L_d.

Stage 9 (t_8-t_9): At t_8, the voltages across both capacitors C_1 and C_2 reach a value near to zero Volts and switches S_1 and S_2 turn-on with Quasi-ZVS. The inductor L_d current increases linearly, transferring the load current from diode D_4 to diode D_3. At t_9, inductor L_d current reaches the load current value I_C.

Fig. 7 presents the main theoretical waveforms of the proposed QZVS two switches forward converter.

Special attention must be paid with the transformer magnetizing current. In stages 2 and 4, the commutations occur from the switches to the diodes, and the load current magnitude takes an important role. Whether the converter operates at no-load or even with low load current, the commutation time enlarges resulting in the increase of the effective duty cycle. In order to guarantee the transformer core demagnetization, a compensation in the duty cycle is required.

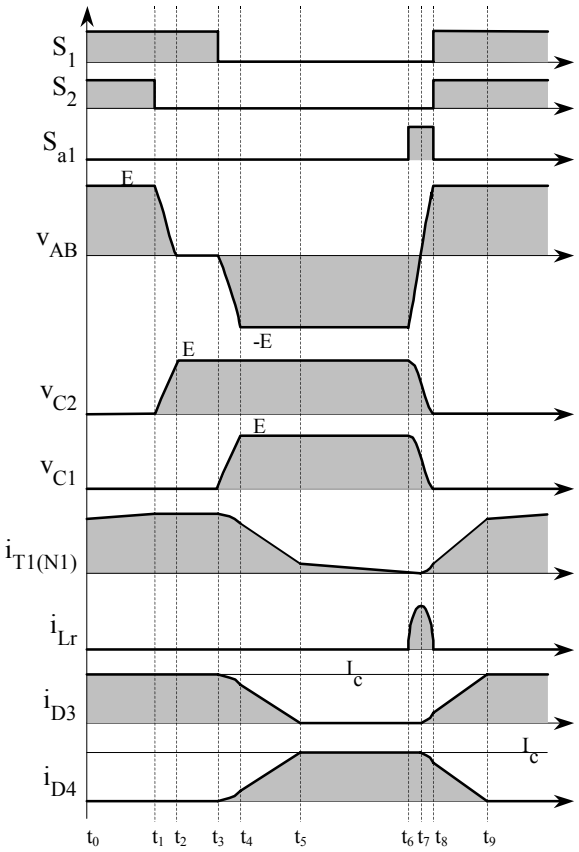


Fig. 7 – Main theoretical waveforms.

IV. Design Considerations

Regarding the switches selection, majority carrier type such as MOSFETs are indicated to be used as main switches, since their commutations are with ZVS (and Quasi-ZVS). On the other hand, the auxiliary switch S_{a1} operates with ZCS, and it is recommended the use of the minority carrier type switches, like IGBT.

A special care must be taken to design the resonant inductor L_r. In stage 8, when the resonance among capacitors C_1 and C_2 and inductors L_r and L_d occurs, the voltages across both capacitors must reach a value near to zero. This is the feature of the Quasi-ZVS.

When the voltage across the transformer reaches zero (v_{AB}=0), the load current flows through diode D_4, and L_d inductor energy starts a resonance, as it can be seen in the equivalent circuit illustrated in Fig. 8. The magnetizing inductance L_m is neglected in this analysis, because L_r is much smaller than L_m ($L_r << L_m$).

In circuit presented in Fig. 8, the capacitors C_1 and C_2 resonate with inductors L_r and L_d. In this resonance, a value near to zero is adopted (V_{QZVS}), at which main switches must turn-on. In this way, the resonant inductor value can be calculated by (1).

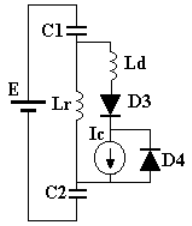


Fig. 8 – Stage 8 equivalent resonant circuit.

$$L_r \le \frac{L_d.\left(E^2 - \left(E - V_{QZVS}\right)^2\right)}{\left(E - V_{QZVS}\right)^2} \qquad (1)$$

V. Design Example

In this section is presented a design example of the proposed converter.

The converter specifications are as follows.

Input voltage: $E = 200V$,

Output power: $Po = 250W$,

Output voltage: $Vo = 48V$,

Switching frequency: $fs = 100\ kHz$,

Maximum duty-cycle: $D = 0.485$,

Transformer turn ratio: n = N1/N2 = 1.8 : 1,

Measured leakage inductance $L_d = 18\mu H$,

Defining $V_{QZVS} = 20V$,

From (1) the resonant inductor value is obtained: $Lr \le 4.22\mu H$

The value of 4.22µH is the maximum value of the L_r inductance, for which the commutations at main switches occur with 20 Volts, considering the auxiliary circuit quality factor is high. It is important to highlight that the L_d inductor is the transformer leakage inductance.

VI. Experimental Results

A prototype based on design example parameters was implemented to verify the operation principles of the proposed converter.

Table II gives the list of components and devices utilized in the prototype.

TABLE II – COMPONENTS UTILIZED IN THE PROTOTYPE.

Components	Specifications
S_1, S_2	MOSFETs IRFP450
S_{a1}	IGBT HGTP3N60C3D
D_1, D_2	BYV27C
D_3, D_4	MUR1515
D_{a1}	HFA25PB60
T_1,(N1,N2)	EE-65/26, (N_1:N_2) = 22:14 turns – Thornton
Lr	EE-30/14 - 5 turns = 3.7uH – Thornton
C_1, C_2	2.2nF

In order to implement the proposed switches command logic, an Erasable Programmable Logic Device - EPLD (EPM7128LC84-7/ALTERA) operating at 33.33MHz was used. With this device it is possible to make the demagnetizing period adequate to reset the transformer

magnetizing flux, using programmable digital logic. The use of EPLD allows obtaining a compact logic circuitry as well as a simple and flexible command circuit layout. Furthermore, during the prototype development stage, the employment of this programmable device becomes adequate because each modification in the command logic is quickly performed by software, keeping the same hardware.

Fig. 9 presents the S_{a1} gate voltage and its collector-emitter current, demonstrating that it operates with ZCS.

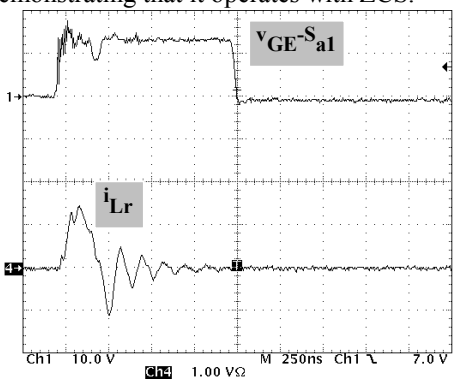


Fig. 9 – S_{a1} gate-emitter voltage and collector-emitter current.

The Quasi-ZVS of switch S_1 can be seen in Fig. 10. S_1 gate voltage is applied when the voltage across switch S_1 is near to zero, at the end of the eighth stage. In the same figure it is presented the transformer primary winding current, showing that the current increases only after the voltage reaches 100V (a half of the input voltage source). At this moment the voltage across the transformer is zero.

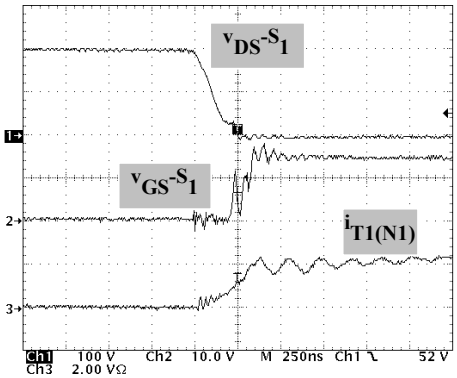
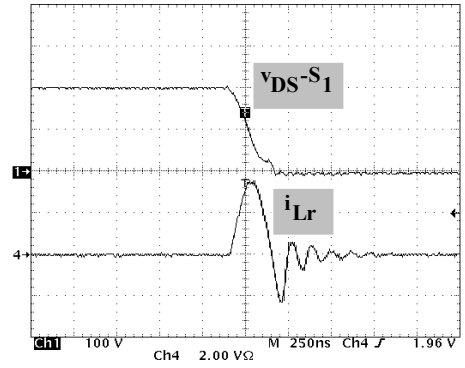
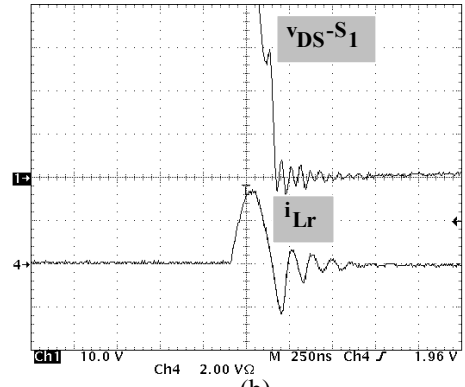


Fig. 10 – S_1 drain-source voltage, S_1 gate-source voltage and primary winding transformer current.

The resonance between capacitor C_1 and inductor L_r is shown in Fig. 11(a). A vertical zoom is presented in Fig. 11(b) to highlight the Quasi-ZVS. In this figure is possible to see the Quasi-ZVS voltage level ($V_{QZVS} \approx 26V$). This value is different of the ideal value adopted in the design example due to the losses that occurs during the freewheeling and because the quality factor of the auxiliary circuit is not high.



(a)



(b)

Fig. 11 – (a) S_1 drain-source voltage and resonant inductor current; (b) Zoom in the vertical scale.

The proposed auxiliary circuit presents low rms and average current values. This feature can be seen in Fig. 12, where the transformer primary winding current and L_r inductor current are presented.

The three-level voltage and the current in the primary side of the transformer are presented in Fig. 13.

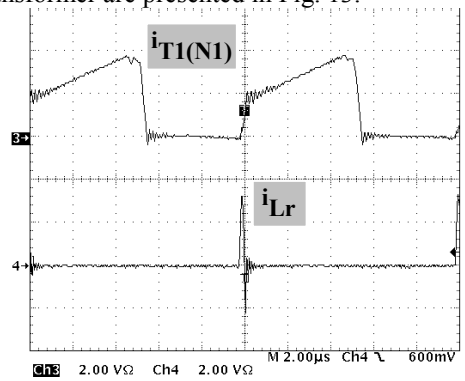


Fig. 12 – Transformer primary winding current and resonant inductor current.

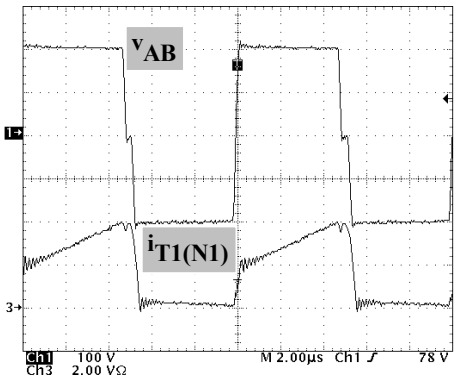


Fig. 13 – Three-level voltage and current through primary side of the transformer.

Efficiencies of the two switches forward converter with the proposed AACC and without the AACC are presented in Fig. 14. It can be seen the efficiency increase due to the use of the proposed AACC (91%) when compared to the hard converter (87%) at full load.

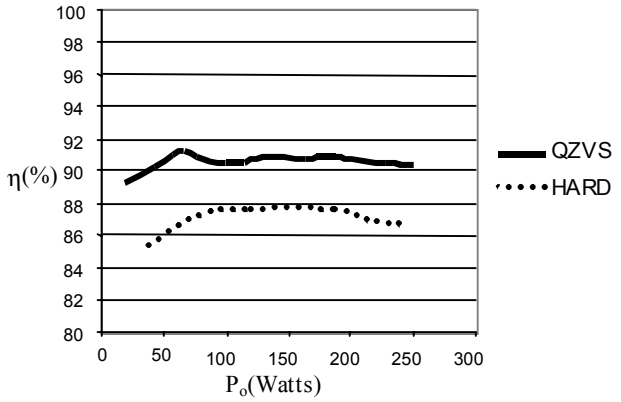


Fig. 14 – Efficiency of the two switches forward converter with AACC (Quasi-ZVS) and without AACC.

VII. Conclusions

In this paper, a family of converter with ZVS at turn-off and with Quasi-ZVS at turn-on is presented.

The auxiliary circuit is composed of few elements that present low rms and average current values. These features result in small volume and low cost auxiliary circuit. In addition, this circuit presents low commutation losses because it operates with ZCS.

Experimental results obtained from a two switches forward converters are presented to demonstrate the feasibility of the presented technique.

Inductor L_d is realized by transformer leakage inductance, therefore the inclusion of an additional inductor is not necessary.

High efficiency is achieved due to the fact that the converter operates with low commutation losses and with duty-cycle near to 50% at full-load. The implemented prototype presented 91% of efficiency at full-load.

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