A Full Bridge ZCS PWM Converter for High Voltage and High Power Applications

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Abstract- This paper presents the detailed analysis of a full bridge zero current switched (FB-ZCS) PWM converter that is suitable for high-voltage and high-power DC applications. It exhibits excellent ability to incorporate parasitic parameters, zero current turn-off characteristics for all active switches and ZVS operation for all diodes on the high voltage side. Based on the features of high-voltage power supplies, the converter utilizes parasitic components, particularly for the high-voltage transformer, and employs fixed frequency phase-shift control to implement soft-switching commutations. Steady state analysis of the converter is presented and major features of the converter are discussed. Finally, small signal model based on the averaging method is created and the simulated results for typical traveling wave tube (TWT) load are given.

I. INTRODUCTION

High-voltage DC-DC converters are widely used in different types of electronic equipment such as industrial and medical X-ray imaging, TWT R.F. generation etc. However, the design of high-voltage DC-DC converters is problematic because the large turns ratio of the transformer exacerbates the transformer non-idealities. In particular the leakage inductance and the winding capacitance can significantly change converter behavior. In switched-mode converters, the output transformer leakage inductance causes undesirable voltage spikes that may damage circuit components and the winding capacitance may result in current spikes and slow rise times. Both non-idealities can lead to greatly increased switching and snubber losses and reduced converter efficiency and reliability [2,7,10].

The choice of a converter topology for high-frequency and high-voltage applications is severely limited by the characteristics of high-voltage transformer, which is the central component of any high-voltage converter. Meanwhile, output filter inductors at high voltage side, normally, can't be used due to the high voltage drop on the inductors and reverse over-voltage across diodes caused by ringing of parasitic parameters. This suggests proper selection of low reverse-recovery time diodes to mitigate current spikes. Based on the above considerations, many power converters have been proposed in the past as a means of supplying high output voltages. Of these converters, the most commonly used approach was resonant converters [3-9].

While operating at light load, the series resonant converter (SRC) becomes virtually uncontrollable. Moreover, parasitic capacitance is not integrated into the resonant tank in the SRC [3,5,7]. The parallel resonant converter (PRC) with capacitive output filter proposed in [4] and [7-9] are relatively simple, but are difficult to control over a wide voltage conversion ratio and load ranges. In addition, saturation problems in the high-voltage transformer can occur in the full bridge implementation of the PRC. To remove the above limitations, the resonant converter with three or more resonant elements is proposed in [6]. In this converter, control and soft switching are maintained over wide load and voltage conversion ratio ranges by circulating an additional amount of reactive energy through the resonant components. Due to the increased complexity of the resonant circuits, multi-element resonant converters exhibit complex dynamic behavior, so fast and robust transient response is difficult to obtain. To realize constant frequency and ZVS operation, the improved version series resonant converters are proposed in [1] and [5]. However, in case of high power application and high power factor are required, the three-phase power factor correction converter will be employed as front-end regulator, and the intermediate DC bus voltage thus is around 800V. The minority–carrier devices such as BJTs, IGBTs and GTOs are predominantly used in this type of application. The converters with ZCS operation will be more attractive than the converter with ZVS. In addition, the rectifier diodes usually suffer from severe reverse recovery problems under high DC output voltage situation. Therefore, the operation of the rectifier diodes with ZVS is desired.

This paper presents a comprehensive study of a high-voltage version FB-ZCS PWM converter, including steady state analysis, small signal modeling, generalizing major features of the converter and simulation verification for a TWT application. The proposed converter makes use of parasitic components, including the leakage inductance and capacitance of the high-voltage transformer and the junction capacitance of the rectifier diodes, to implement ZCS operation. An additional bonus is that rectifier diodes at high voltage side operate with ZVS. These unique features, together with the use of constant-frequency phase-shift control, make the converter attractive for high-voltage and high power applications.

II. TOPOLOGY DERIVATION

A traditional FB-ZCS topology shown in Fig.1 was first described in [11], which is a dual topology of the well-known FB-ZVS-PWM converter. In Fig. 1, L_r is the resonant inductance that incorporates the leakage inductance of the transformer, and C_r is the resonant capacitor that incorporates

the junction capacitance of the rectifier diodes and the reflected winding capacitance from secondary side of the power transformer. The insertion L_{in} between input and inverter is to achieve a current-fed source.
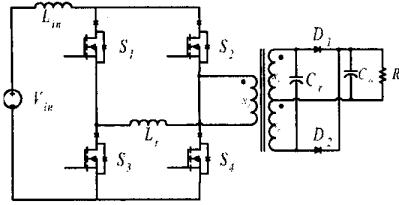

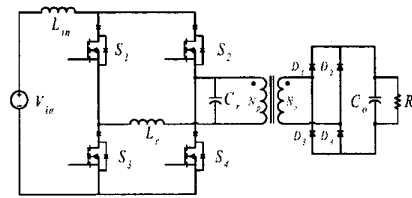Figure 1: A conventional FB-ZCS topology

Figure 2: Simplified high-voltage FB-ZCS Converter

In this paper, the target application is the traveling-wave-tube load, one extensively used in the communication industry. A practical power supply system for this application usually requires a power converter with multiple high voltage DC outputs, typically 15kV, 10 kV and 5kV etc. For the sake of simplicity, the multi-output traveling wave tube load is reduced into a single output load R (15kV, 5kW rating) in the analysis here.

Generally, in a high voltage, DC/DC converter, output-filtering inductors can't be used on the high voltage side due to high voltage drop. Therefore, only output capacitors can be used at the secondary side and thus, the converter should be current fed.. The traditional FB-ZCS topology fits this structure well. However, to obtain safe operation of transformer and high output voltage, multiple secondary rectifier circuits are needed in series to feed the high voltage load. Further, each single rectifier circuit is a full bridge configuration in order to obtain high power output. A practical schematic diagram of the high voltage FB-ZCS converter would feature a high voltage transformer with multiple same section secondary windings, series connected diodes, and a resonant tank at the low voltage side. Fig. (2.) is a simplified equivalent circuit based on the lumped parameter model of the high voltage transformer [8]. In the equivalent circuit all leakage inductors are reflected and integrated into resonant inductor L_r of the primary side, and capacitors are reflected and incorporated into resonant capacitor C_r. Similar to the FB-ZVS-PWM converter, the modified FB-ZCS-PWM converter also uses phase-shift control to obtain fixed frequency operation

III. CONVERTER OPERATION

The proposed converter has ten operation intervals during a single switching cycle. Only the intervals for a half-switching cycle will be shown here as the remaining five are symmetric. The equivalent circuit for each interval during the half-cycle is shown in Fig. 3, and key waveforms are shown in Fig. 5. The derived equations characterizing the converter's behavior during each mode are based on the following assumptions:

1) L_{in} current is ripple free and can be considered a constant current source, I_{in}
2) output voltage is a constant, V_o
3) all components are considered ideal
4) from the high voltage transformer, the leakage inductance is used as L_r and its capacitance is C_r.

The first five modes of operation over half the switching period are discussed as follows:

1). Mode I: $[t_o \leq t \leq t_1]$ -S3/S4 Overlap

Operation begins with S1, S3, S4, and D2 on at $t=t_o$. During this mode, S4 current is transferred to S3 in a non-resonant, linear fashion so that S4 can turn off with ZCS. During this mode, energy is transfer to the output. Let us assume that mode ends at $t=t_1$ when current in S4 reaches zero, $i_{Lr}(t_1)=0$, and is turned off. In this mode the resonant capacitor voltage and inductor current are:

$$i_{Lr}(t_o) = I_{in} \qquad n = \frac{N_p}{N_s} \qquad (1.)$$

$$i_{Lr}(t) = i_{sw4}(t) = -\frac{n \cdot V_o}{L_r} \cdot (t - t_o) + i_{Lr}(t_o) \qquad (2.)$$

$$v_{Cr}(t) = n \cdot V_o \qquad (3.)$$

Overlap of S3/S4 must be long enough to allow S4 current to reach zero. Evaluating (2.) at $t=t_1$ we obtain:

$$(t_1 - t_o) = \frac{I_{in}}{\dfrac{n \cdot V_o}{L_r}} \qquad (4.)$$

2.) Mode II: $[t_1 \leq t \leq t_2]$ -Input Inductor Charging Interval

With S1 and S3 both on, the input inductor stores energy. No energy is transferred from input to load. This interval duration is controlled for nominal operation and ends when S2 is turned on at $t=t_2$. No constraint on interval duration exists except that an increase in this interval duration will be accompanied by a corresponding decrease in the Mode IV interval duration since the other modes have minimum

durations to achieve ZCS and the total switching period is fixed. In this mode the resonant capacitor voltage and inductor current are:

$$i_{Lr}(t) = 0 \qquad (5.)$$

$$v_{Cr}(t) = n \cdot V_o \qquad (6.)$$

3.) Mode III: [$t_2 \leq t \leq t_3$]   -Resonant Period

S1 current is transfer to S2 in a resonant fashion. S1 and S2 overlap during this mode for the transfer. Specifically, by allowing inductor current to resonant to $-I_{in}$, S1 current goes to zero allowing ZCS. Mode III ends when S1 is turned off at $t=t_3$. In this mode the v_{Cr} and i_{Lr} are:

$$i_{Lr}(t) = -\frac{n \cdot V_o}{Z_o} \cdot \sin(\omega_o \cdot (t - t_2)) \qquad (7.)$$

$$v_{Cr}(t) = n \cdot V_o \cdot \cos(\omega_o \cdot (t - t_2)) \qquad (8.)$$

where $Z_o = \sqrt{\dfrac{L_r}{C_r}}$, the resonant impedance and $\omega_o = \sqrt{\dfrac{1}{L_r \cdot C_r}}$, the resonant angular frequency.

Overlap of S1/S2 must be long enough to allow S1 current to reach zero. Solving (7.) at $t=t_3$, $i_{Lr}(t_3) = -I_{in}$ we obtain,

$$\gamma = \omega_o \cdot (t_3 - t_2) = \sin^{-1}(\frac{I_{in} \cdot Z_o}{n \cdot V_o}) \qquad (9.)$$

4.) Mode IV: [$t_3 \leq t \leq t_4$] – C_r Discharge Interval

During this mode, the resonant capacitor discharges linearly to $-nVo$. Mode IV ends when capacitor is discharged allowing D1\D4 to conduct at t_4, mode end.

$$i_{Lr}(t) = -I_{in} \qquad (10.)$$

$$v_{Cr}(t) = -\frac{I_{in}}{C_r} \cdot (t - t_3) + n \cdot V_o \cdot cos(\gamma) \qquad (11.)$$

Mode ends when D1\D4 start conducting at $t=t_4$ and the capacitor voltage is clamped to $-nV_o$.

$$v_{Cr}(t_4) = -n \cdot V_o = -\frac{I_{in}}{C_r} \cdot (t_4 - t_3) + n \cdot V_o \cdot cos(\gamma) \qquad (12.)$$

Solving we obtain,

$$(t_4 - t_3) = \frac{n \cdot V_o \cdot C_r \cdot (1 + cos(\gamma))}{I_{in}} \qquad (13.)$$

5.) Mode V: [$t_4 \leq t \leq t_5$] – L_{in} Energy Transferred to Output

During this mode, D1\D4 are on and energy will be transferred from input inductor to output in a boost like fashion. The i_{Lr} and v_{Cr} equations are given as,

$$i_{Lr}(t) = -I_{in} \qquad (14.)$$

$$v_{Cr}(t) = -n \cdot V_o \qquad (15.)$$

The second half period, Modes VI through X, are symmetric with respect to the first five modes. Table I shows device conduction states for all ten modes.

TABLE 1
DEVICE CONDUCTION STATES

Mode	S_1	S_2	S_3	S_4	D_1	D_2	Mode Description
Mode I	X		X	X		X	S4 to S3 Overlap
Mode II	X		X				L_{in} Charge
Mode III	X	X	X				Resonant Transfer S1 to S2
Mode IV		X	X				C_r Discharge
Mode V		X	X			X	L_{in} Energy to Output
Mode VI		X	X	X	X		S3 to S4 Overlap
Mode VII		X		X			L_{in} Charge
Mode VIII	X	X		X			Resonant Transfer S2 to S1
Mode IX	X			X			C_r Charge
Mode X	X			X		X	L_{in} Energy to Output

IV. NORMALIZED STEADY STATE ANALYSIS

The steady state development above outlines the equations controlling the duration of three the five half period modes. Two additional equations are needed to solve for all mode durations. Eqs. (4.),(9.), and (13.) give the fixed duration for Modes I, III, and IV, respectively. Eqs. (16.) is derived by averaging the output current, and Eq. (17.) is obtained by noting the sum of time duration for Modes I-V equal the half period length.

$$I_0 = \frac{\frac{1}{2} \cdot (t_1 - t_0) \cdot n \cdot I_{in} + n \cdot I_{in} \cdot (t_5 - t_4)}{\frac{T_s}{2}} \qquad (16.)$$

$$\frac{T_s}{2} = (t_1 - t_0) + (t_2 - t_1) + (t_3 - t_2) + (t_4 - t_3) + (t_5 - t_4) \qquad (17.)$$

These equations can be solved then plotted to investigate converter behavior and to facilitate design. Figure (4.) shows an example of the MathCAD structure used to produce the operational curves in this paper where normalized parameters are used as follows,

$$\alpha = \omega_o \cdot (t_1 - t_0) = \frac{M}{n \cdot Q} \qquad (18.)$$

$$\beta = \omega_o \cdot (t_2 - t_1), \ \varepsilon = \omega_o \cdot (t_5 - t_4) \qquad (19.)$$

$$\gamma = \omega_o \cdot (t_3 - t_2) = sin^{-1}(\frac{M}{n \cdot Q}) \qquad (20.)$$

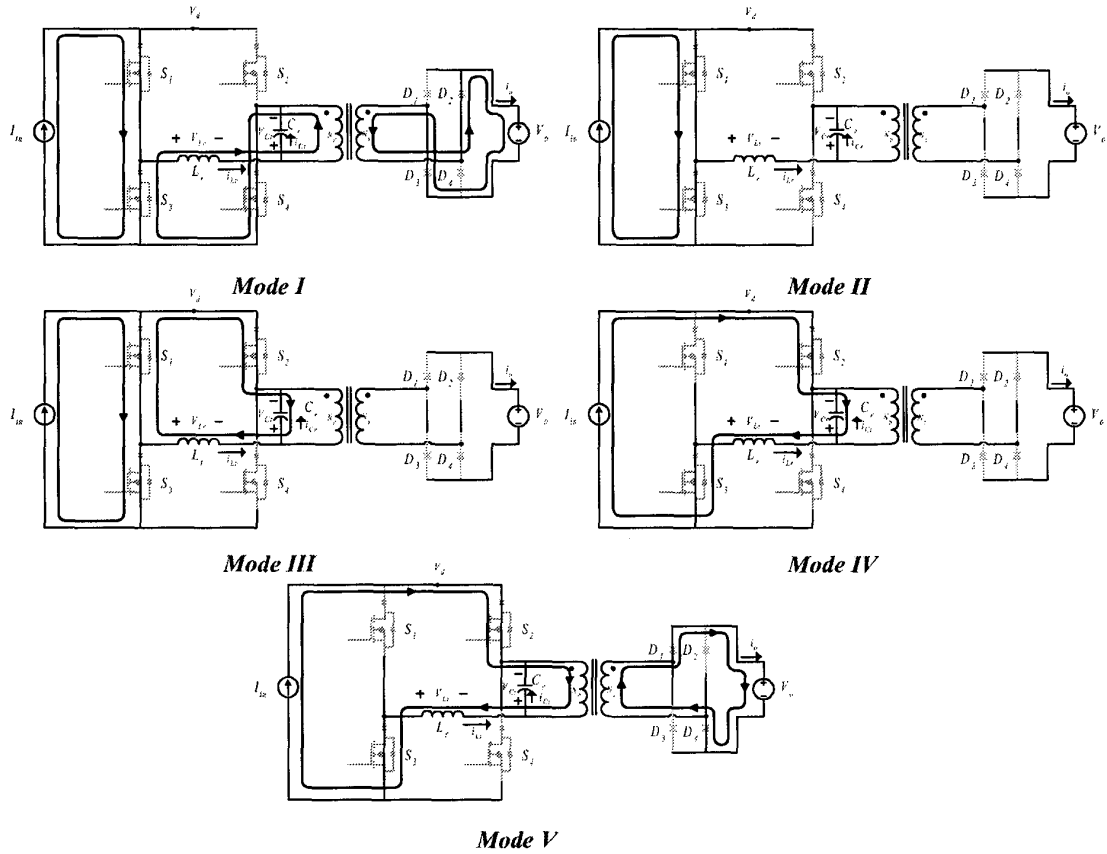*Mode I*

Mode II

Mode III

Mode IV

Mode V

Figure 3: Equivalent circuits for FB-ZCS operation

$$\delta = \omega_o \cdot (t_4 - t_3) = \frac{n \cdot Q}{M} \cdot (1 + \cos(\gamma)) \qquad (21.)$$

$$\frac{\omega_o \cdot T_s}{2} = \frac{\pi}{f_{ns}} = n \cdot M \cdot (\frac{1}{2} \cdot \alpha + \varepsilon) \qquad (22.)$$

$$\frac{\omega_o \cdot T_s}{2} = \frac{\pi}{f_{ns}} = \alpha + \beta + \gamma + \delta + \varepsilon \qquad (23.)$$

where L_r and C_r, resonant components, $M = \dfrac{V_0}{V_{in}} = \dfrac{I_{in}}{I_o}$, gain, ,

$Q = \dfrac{R_{Load}}{Z_o}$ normalized load, $f_{ns} = \dfrac{f_s}{f_o}$, normalized switching

frequency.

Given

$$\alpha = \frac{M}{n \cdot Q} \qquad \delta = \frac{n \cdot Q}{M} \cdot (1 + \cos(\gamma))$$

$$\gamma = \text{asin}\left(\frac{M}{n \cdot Q}\right) \qquad \frac{\pi}{f_{ns}} = n \cdot M \cdot \left(\frac{1}{2} \cdot \alpha + \varepsilon\right)$$

$$\frac{\pi}{f_{ns}} = \alpha + \beta + \gamma + \delta + \varepsilon \qquad \begin{array}{l} \beta \geq 0 \\ \varepsilon \geq 0 \end{array}$$

$$A(M, Q) := \text{Find}(\alpha, \beta, \gamma, \delta, \varepsilon)$$

$$A(18.75, 636.39) = \begin{pmatrix} 0.324 \\ 8.117 \\ 0.33 \\ 6.005 \\ 20.58 \end{pmatrix}$$

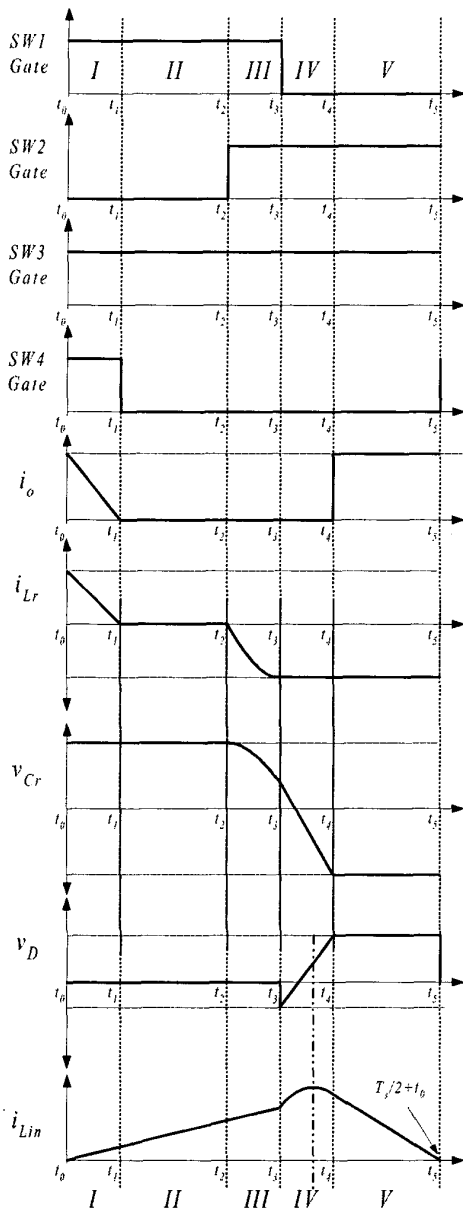Figure 4: Results of steady state analysis using MathCAD

Figure 5: Half Period Waveforms of FB-ZCS Converter

The MathCAD Solve Block is used to plot the various steady state characteristic curves. An example is shown as Fig. (6.) with additional comments regarding converter characteristics. Fig. (6.) depicts gain, M, versus the phase shift angle, β, which is the interval between S4 turn off and S2 turn on. β represents the fundamental control parameter. The curves are drawn for base values of Q_{Base}=636.4 and f_{nsBase}=.089 with n=1/11 in anticipation of the design example to be shown in the subsequent section. The curves are presented to show the qualitative relationships between load, gain, switching and resonant frequency.

Increasing β corresponds to a gain increase and is analogous to increasing D in the boost converter. From the curves, it is clear that an increase in load results in a decrease load regulation range for constant f_{ns} and Z_o, yet this decrease is not linear (load doubling yields max gain decrease from 80 to 50). A more significant decrease in regulation range comes from reducing f_{ns}.
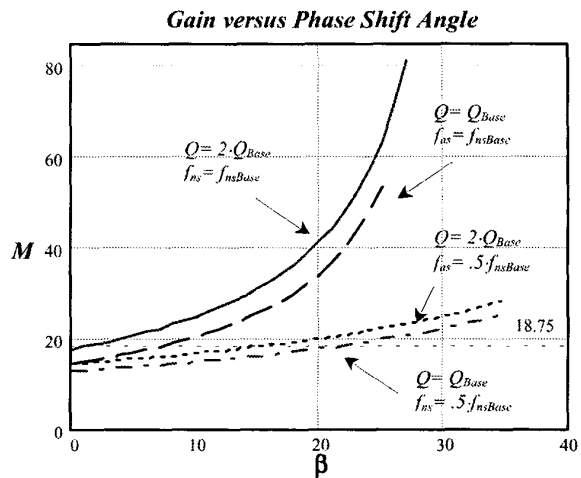
Gain versus Phase Shift Angle

Figure 6: Gain, M, vs. Phase shift angle, β for various loads

At first glance this could seem incorrect as it might appear that a smaller f_{ns} means less of the half period is taken by the resonant mode. While this is true, a smaller f_{ns} also means an increase Mode IV duration , resulting in less power transfer. As a final note on Fig. (6), we observe that the curves are plotted over differing ranges of M and β. This is a result of several factors. First, the arcsine argument of (20.) is a representation of the ZCS condition (27.) and establishes an upper limit on M for a given n and Q. Second, since the total of the five intervals equals the half period length, an increase in β means less of the half period is available for the other modes. In the limiting case, since several modes have duration fixed by operating state, β will have a fixed upper limit that is less than the half period length and is a function of load and f_{ns}. The mechanisms above effectively limit load regulation range.

V. FB-ZCS FEATURES AND DESIGN CONSIDERATIONS

5.1. Converter Features

Based on the above analysis, the features of the given converter can be summarized as follows:

(1) The active switches can be turned off with ZCS by proper phase-shift control and by the overlap time of the two upper switches or lower switches. Output rectifier diodes commute with ZVS and ZCS. This

feature is different from the traditional boost converter, where the diode suffers from severe reverse-recovery problems.

(2) Unlike the traditional resonant-type of the high-voltage DC/DC converter, the converter acts like a PWM converter except the overlap angle between upper switches or lower switches. The converter can operate with a fixed switching frequency and phase-shift PWM control techniques that are similar to existing FB-ZVS converters.

(3) Although ZCS is achieved, the topology still maintains a wide load regulation unlike other soft-switching topologies.

(4) Transformer and device parasitic can be fully utilized to achieve ZCS.

5.2. Design Considerations

A. Switch Overlap

For proper gating to regulate output voltage, it is necessary to meet certain constraints to realize ZCS. According to operation principle of the converter, for S3 and S4 ZCS operations, the S3/S4 overlap time should be longer than time to allow S3 (S4) current to reach zero in Mode I (VI). For S1/S2 ZCS operations, the S1/S2 overlap time should be longer than time to allow S1 (S2) current goes to zero in Mode III (VIII). This constraint is given by (24.) where full load conditions should be assumed to guarantee ZCS over the entire load range.

$$t_{overlap} \geq \{(t_1 - t_o)_{max}, (t_3 - t_2)_{max}\}_{max} \qquad (24.)$$

where these intervals can be obtained from (4.) and (9.)

An upper limit exists for the overlap time. Gating S1 (S2) past this limit will allow current to resonant away from zero before it is turned off. From the waveforms of Fig. (4.), note that the gating signal to S1 must be removed before v_{Cr} reaches zero or switch current will become nonzero. This constraint is given by (25.).

$$t_{overlap} \leq (t_3 - t_2) + \frac{nV_oC_r}{I_{in}}\cos(\gamma) \qquad (25.)$$

B. Selecting active switches and output rectifier diodes

Steady-state device voltage\current stress is shown in Table II, where switching transients and parasitic ringing are not considered.

TABLE II
COMPONENT VOLTAGE\CURRENT STRESS

Parameter	V_{SWI-4}	I_{SWI-4}	V_{DI-4}	I_{DI-4}	V_{CR}	I_{LR}
Max Stress Value	$n \cdot V_o$	I_{in}	V_o	$n \cdot I_{in}$	$n \cdot V_o$	I_{in}

In FB-ZCS converter, possibly the most significant limitation is the voltage and current spikes caused by switch commutation and ringing between parasitic device parameters and the resonant tank. With effective use of snubbing circuits, reasonable limits can be realized (1.5~2 times maximum device voltage/current stress shown in Table II). Preferred devices are IGBTs for high-power, high-frequency operating, high voltage stress applications. As for rectifier diodes, the maximum voltage and current stress is clamped at V_o and n I_{in} throughout operation process.

C. Selecting resonant components and turns ratio

While selecting resonant tank components, the parasitic parameters of the transformer must be considered. For the high voltage application example presented in this paper, the high voltage load is a 5kW @ 15kV and the typical leakage inductance value between the primary side and each secondary winding, reflected to primary side is in the range of 5~10 µH. Manufacturer testing data tell us that the total reflected leakage inductance is about 30uH~50µH. Therefore, for most applications, an additional resonant inductor is not needed. The spray capacitor value of the high voltage transformer can be estimated by the method introduced in [10].

ZCS operation is obtained by lateral current commutation between S1\S2 and S3\S4. The upper switches, S1\S2 commutate the input current in a resonant fashion while S3\S4 commutate current linearly. Certainly, lateral switch overlap must allow current to reach zero before turn off. A detailed discussion of switch timing will be presented in the next section, however, it is important to note that the resonant parameters are directly related to ZCS operation. From the waveforms of Fig. (5.), note that in order for ZCS to be achieved, the energy stored in C_r must be enough to drive i_{Lr} to $-I_{in}$. For the general case, this can be expressed as,

$$\frac{1}{2} \cdot L_r \cdot (-I_{inmax})^2 = \frac{1}{2} \cdot C_r \cdot ((n \cdot V_0)^2 - (n \cdot V_0 \cdot \cos(\gamma))^2) \qquad (26.)$$

In the limiting case, $\gamma=90°$, energy transfer from resonant capacitor is maximum. This maximum must be enough to drive resonant inductor current to $-I_{in}$. Therefore, for ZCS under all line and load, we have,

$$\frac{1}{2} \cdot C_r \cdot (n \cdot V_0)^2 \geq L_r \cdot (-I_{inmax})^2 \qquad (27.)$$

However, the larger the value of C_r is, the longer the discharging transition process of C_r and consequently mode IV duration takes up more of the available half period thus reducing load regulation range. In addition, the switch timing constraints are also applied to selection of resonant tank. Combining these considerations in design, a good trade-off can be obtained.

Generally speaking, the magnetic core utilization is poor, making it more difficult to realize a small turns-ratio (primary/secondary) transformer. However, the larger the turns-ratio is relatively, the larger the voltage stress of the power devices, and the more difficult it is to find suitable devices. Therefore, turns-ratio should be set while considering power IGBT device ratings.

VI. DESIGN EXAMPLE AND SIMULATION RESULTS

For a typical TWT load, the parameters are selected as follows: V_{in}=800V, V_o=15kV, P_o=5kW. The values of , f_s=20kHz, L_{in}=5mH, L_r=50uH, C_r=10nF, C_o=100nF, n=1/11 were obtained by evaluation of the gain curves of Fig. (6.) for M=18.75 considering available parasitic values, device voltage stress, and load regulation. From these parameters, the MathCAD worksheet in Fig. (4.) can be used to determine appropriate switch timing. The angular intervals at full load from Fig. (4.) are converted to time in Table III.

TABLE III
COMPONENT VOLTAGE\CURRENT STRESS

Mode I $(t_1 - t_0)$	Mode II $(t_2 - t_1)$	Mode III $(t_3 - t_2)$	Mode IV $(t_4 - t_3)$	Mode V $(t_5 - t_4)$
.22917μs	5.7395μs	.23338μs	4.2459μs	14.552μs

Evaluating Modes I and III above, we see that Mode III duration will set the required overlap time. Table III times are then used to obtain the switch timing and primary switch duty used in the PSPICE simulation schematic of our design example as shown in Fig. (7).
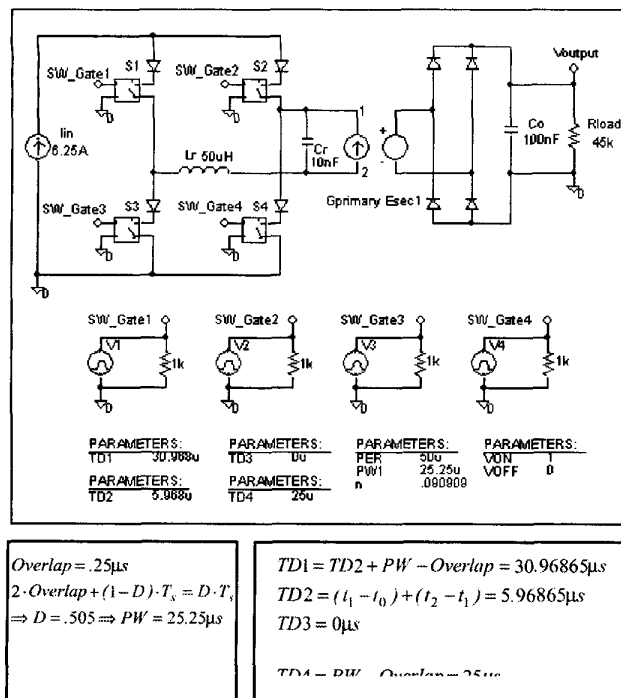

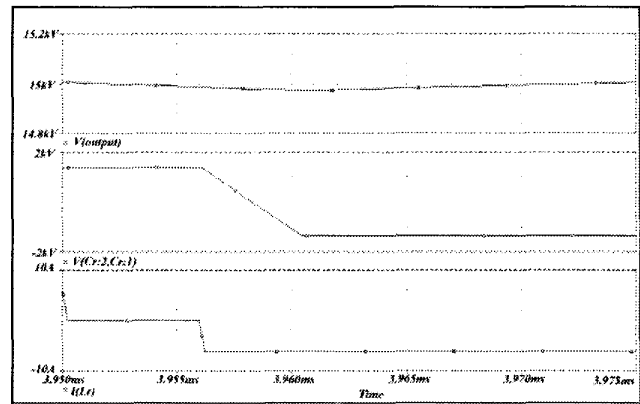Figure 7: PSPICE Simulation schematic

Figure 8: PSPICE Simulation Results (top-v_o, middle-v_{Cr}, bottom-i_{Lr})

From Fig. (8), we see that the theoretical waveforms of Fig. (4.) agree well with the simulation results. Mode duration agrees with the MathCAD calculated values and the desired output voltage is achieved.

VII. SMALL SIGNAL ANALYSIS USING AN AVERAGE MODEL

An average model of the FB-ZCS has been developed to study the small signal characteristics of the FB-ZCS converter. Figure (9.) shows the model's implementation in PSPICE.

The model is developed for a control input called PWM. The PWM control input is used to establish switch timing and spans Modes I-II duration. Although, it is desirable to control β for regulation, it is more reasonable to control $\alpha+\beta$. This is because α has variable duration that is a function of load and can end before switch turn off. Therefore, β is not strictly a function of switch gating, while $\alpha+\beta$ is distinctly the interval between S3 and S2 turn on times.

The average equations for the controlled sources given in Fig. (9.) in the model are shown are expressed by,

$$v_{dAvg} = \frac{2}{T_s} \cdot \left(\frac{n \cdot V_o \cdot \varepsilon}{\omega_o} + \frac{(n \cdot V_o)^2}{2 \cdot i_{LinAVG}} \cdot C_r \cdot (1 - cos(\gamma)^2) \right) \tag{28.}$$

$$G_o = \frac{2}{T_s} \cdot n \cdot i_{LinAVG} \cdot \left(\frac{i_{LinAVG} \cdot L_r}{2 \cdot n \cdot V_o} + \frac{\varepsilon}{\omega_o} \right) \tag{29.}$$

$$\varepsilon = (1 - Duty) \cdot \frac{T_s}{2} \cdot \omega_o - \frac{n \cdot V_o}{i_{LinAVG}} \cdot C_r \cdot (1 + cos(\gamma)) \cdot \omega_o \tag{30.}$$
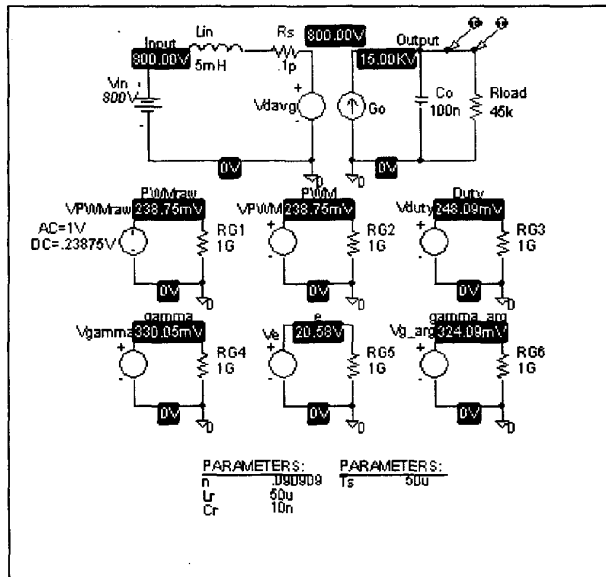
Figure 9: Average model for FB-ZCS in PSPICE with bias point solution

$$\gamma = a\sin(\frac{i_{LinAvg} \cdot Z_o}{n \cdot V_o}) \qquad (31.)$$

$$Duty = PWM + \frac{2 \cdot \gamma}{\omega_o \cdot T_s} \qquad (32.)$$

In Fig. (9.), the bias point solution for the AC Sweep is shown. Note that the model yields perfect agreement with the results of the previous section. The PWM input is the control parameter. An evaluation of the waveforms of Fig.(5.) shows that PWM does not directly correspond to D or (1-D), which are variable assignments that are made to correspond to boost like intervals. As such, the control to output frequency response will be represented as PWM to output voltage and is shown in Fig. (10.).
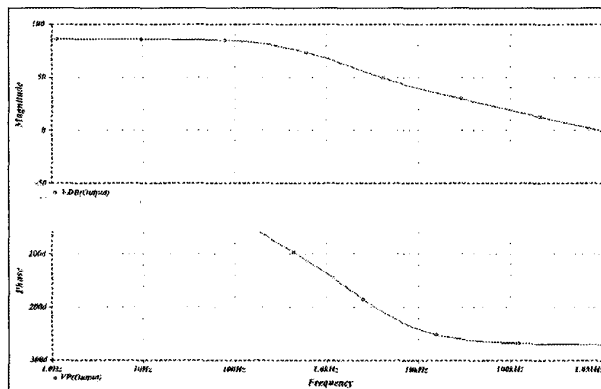

Figure 10: Control to output frequency response

Further, since the FB-ZCS converter is boost like and operated in CCM, the RHP zero is apparent here causing 270° of phase lag and a relatively high filter pole frequency.

VIII. CONCLUSIONS

This paper presents a steady state and dynamic study for Full Bridge ZCS PWM converter used in high-power, high-voltage DC application. The large signal and small signal simulation results are given. The simulation results shows the feasibility of topology in high voltage DC application. Compared with most commonly used full bridge resonant converters, the FB ZCS PWM converter has its unique merits such as with fixed frequency operation and ability to incorporate parasitic components. Detailed treatment of the average model derivation and closed loop control will follow in future publications.

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