# APPLICATION NOTE

## AN1272
UC3842 application note

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## INTRODUCTION

The UC3842 provides all the essential features necessary to the operation of the basic current mode controller. Either a forward or flyback converter may be implemented. The basic differences in these topologies determine special added requirements which, in the flyback or boost converter, relate to stability versus maximum duty cycle.

Without varying the ramp oscillator frequency with load, only a constant frequency converter is possible and this is the basis of line current mode converter circuit design example. Duty cycle is a function of load demand up to the limit imposed by the internal duty cycle clamp and, beyond this, output voltage decreases with increased output current demand.

With the current mode supply the energy supplied to the inductor or transformer primary (which is proportional to square of the primary current) is continuously monitored by the control loop. There are several different current mode topologies in use, among which are:

- Hysteretic
- Constant off time
- Constant frequency

Hysteretic converters must monitor both peak and valley current. This adds greatly to the circuit complexity but enhances control current accuracy. Constant off time requires more logic to insure variable on-time and a fixed off-time. The latter mode (constant frequency with variable duty cycle and peak current sensing) is the primary converter operating condition addressed in this application note for the UC3842.

## UC3842 Pin Functions

**Pin 1: Error amplifier output.** (See Figure 1) Closed loop gain and any additional compensation network is connected between this terminal and the inverting input, Pin 2. Resistor values in the feedback loop may range from 1kΩ to 250kΩ. Output loading must not exceed the source-sink limits stated in the data sheet. Voltage from the error amplification is fed through two diode drops, then further attenuated by a 3:1 resistive divider. This, with the 1V clamp, provides an approximate 0 to 1V reference for the current loop comparator.

**Pin 2: Error amplifier inverting input.** The non-inverting input is fixed at the reference voltage of 2.5V requiring that the feedback voltage be equal to this value under normal operating conditions. Normally a voltage divider is connected between the supply regulated output terminal and ground with a minimum of 1mA of divider current and set for 2.5V out to the error amplifier. Voltage spikes must not exceed $V_{CC}$ positive and 0.7V negative on the feedback line. Open loop testing of the UC3842 in a current mode supply may be implemented as shown in Figure 2 with a potentiometer connected between $V_{REF}$ and ground. Duty cycle may be varied then by varying V2 around the 2.5V level. A synchronous $I_{SENSE}$ signal must be supplied, as shown, to provide duty cycle turn-off.

**Pin 3: Current sense comparator.** The current sense signal provides cycle-by-cycle monitoring of primary switching current in order to provide an active duty-cycle control loop. Figure 3 shows the current sense waveform at Pin 3 versus the output waveform at Pin 6. The Pin 3 maximum voltage to provide current limiting is 1V referenced to ground. When the sense voltage reaches the 1V level, current in primary will no longer increase with increasing load at the supply output, but will allow output voltage to decrease with increased load keeping output current constant.

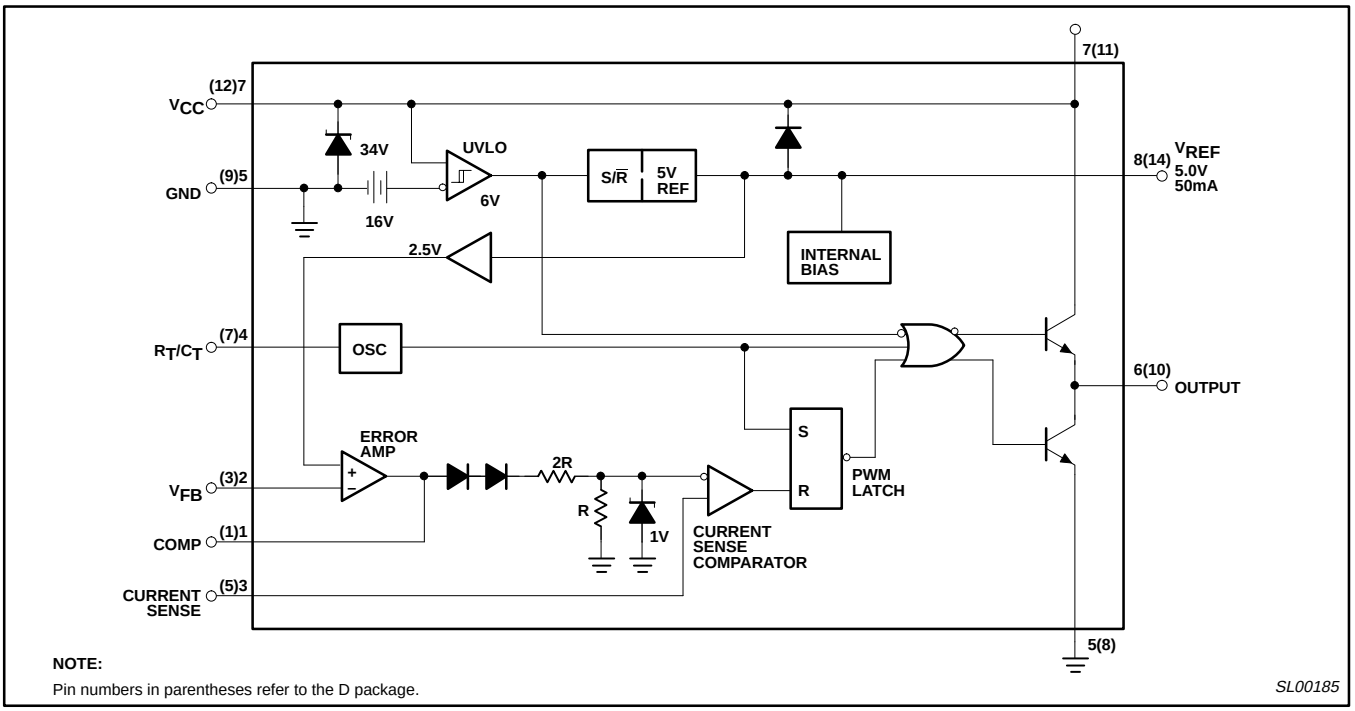
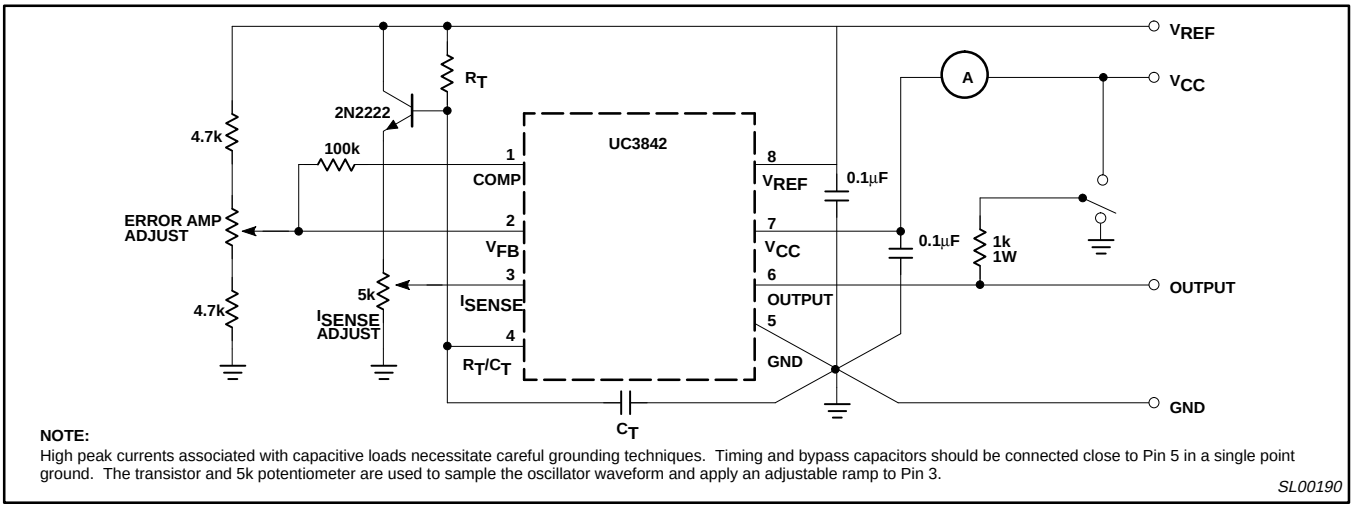



**Figure 1. UC3842 Block Diagram**




**NOTE:**
High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to Pin 5 in a single point ground. The transistor and 5k potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to Pin 3.

**Figure 2. Open-Loop Test Circuit**

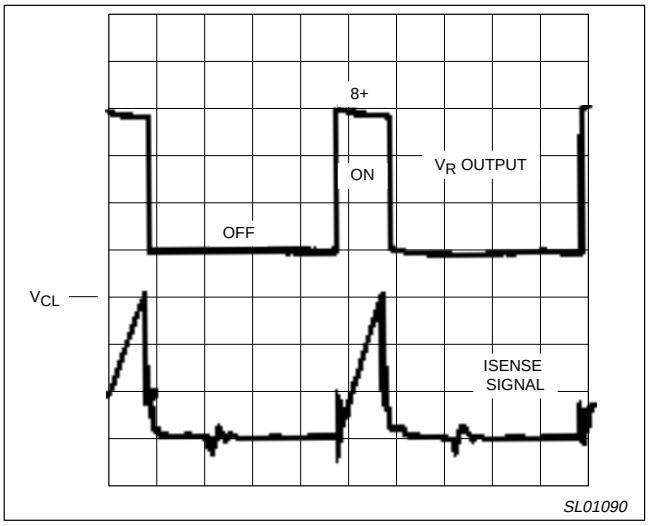



**Figure 3. Current Sense Waveform**

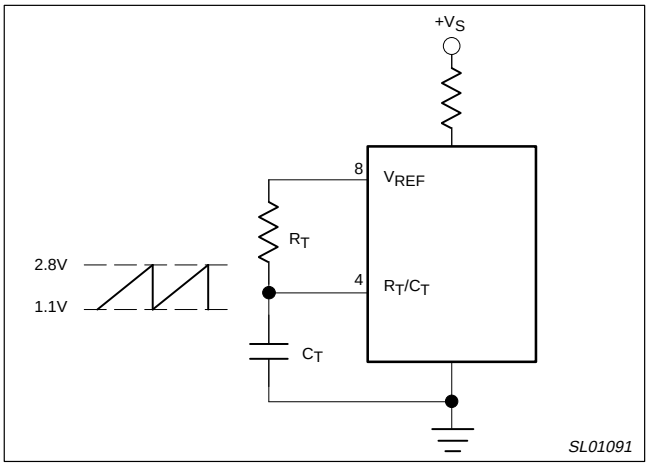



**Figure 4. Timing Circuit**

**Pin 4: Timing network, $R_TC_T$.** An R/C network is connected between $V_{REF}$ (+5.00V) and ground to provide a fixed time base for the PWM (Figure 4). Ramp peak and valley voltage will have a typical value of 1.1V to 2.8V, respectively, at room temperature. The output waveform at Pin 4 is displayed with Pin 6 output in Figure 5.

**Pin 5: Device ground.**

**Pin 6: Switching drive output.** This output stage provides a maximum of 200mA source and sink current to drive the switching device. This is ideally suited to drive a Power FET with a maximum gate capacitance of 1000pF. A minimum gate voltage of 10V is required to achieve low $R_{ON}$ with the typical Power FET. The Philips UC3842 supplies a 12V minimum output at 200mA. (Reference data sheet for specifications.)

NOTE: Bipolar power devices require high sustained base current for low $V_{CE}$ saturation, and minimum deviation. Therefore, an external driver is required for high current bipolar power devices.

**Pin 7: Device supply voltage input.** A special start-up circuit is recommended (Figure 6) to provide optimum use of the undervoltage lockout capabilities. An initial current of 1mA is necessary to start the device and to activate the internal reference when above 10V, but the output circuit will not become active until V7 reaches the 16V upper threshold. (Voltage feed will operate the device at voltages below 16V after the upper threshold has been exceeded.) This allows a 6V hysteresis range to prevent smaller supply voltage changes from triggering the low voltage lock-out mechanism. Bootstrap operation is dependent upon the dropping resistor, $R_S$, from the main supply bus to Pin 7 to provide the necessary 1mA starting current to activate the voltage reference. A storage capacitor is required as shown in Figure 7 to provide enough energy to kick the output circuit into operation without the V7 voltage decaying below 10V. This imposes a minimum value of capacitance to allow the device to start under full load conditions. The typical value required is 100μF. Also critical to successful start-up is a low impedance path from the electrolytic capacitor to Pin 7 and from the bootstrap supply on the transformer. A ceramic

bypass capacitor is recommended at Pin 7 also to further reduce false under-voltage lockout. [Note, that if a fixed voltage feed is used without a low current start-up and bootstrap supply from the transformer, the snap-off feature with supply overload will not be as readily activated by the device and if supplied from a source separate from the output transformer, will not sense low supply conditions at the transformer primary.]

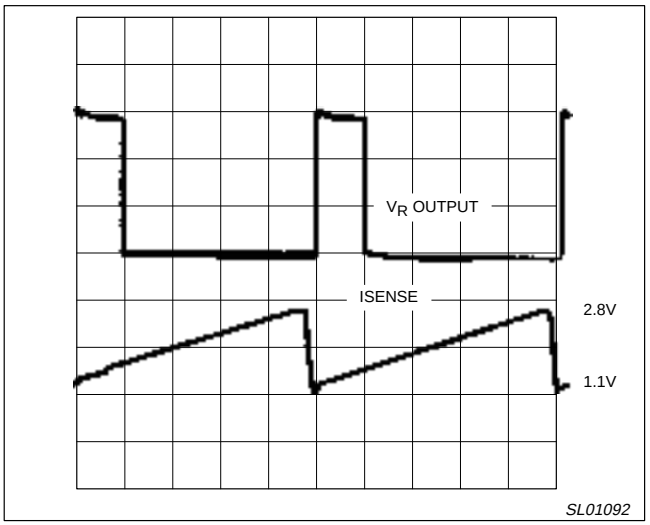



**Figure 5. Oscillator vs Output**

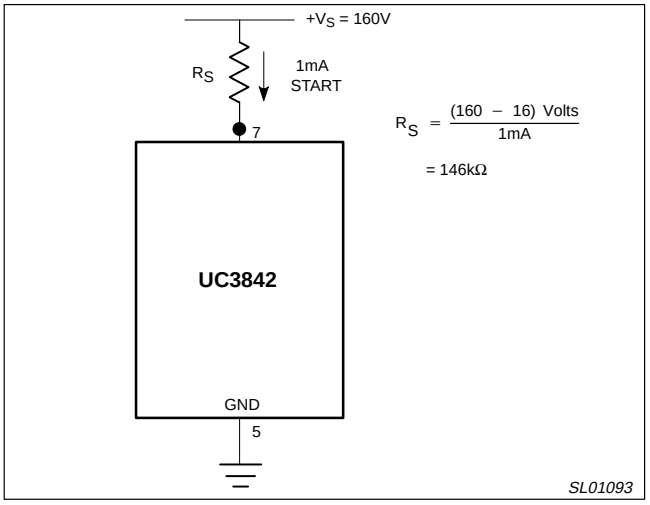



**Figure 6. Calculating the Bootstrap Resistor**

**Pin 8: Voltage reference, 5.0V.** An internal band gap reference is provided internally with an overall accuracy of +1% at 1mA external load. An extra 0.5% error results with a 20mA load. The reference has an accuracy versus temperature of 0.4V/°C. Typical loading due to the oscillator is <1mA. At start-up the internal reference only becomes active when the supply voltage exceeds the under-voltage upper threshold of 16V versus V8 (Figure 8). As the reference is activated, the UVLO logic then enables the device output transistors. Device shutdown is activated when Pin 7 voltage drops below the low level lockout threshold of 10V (Figure 9).

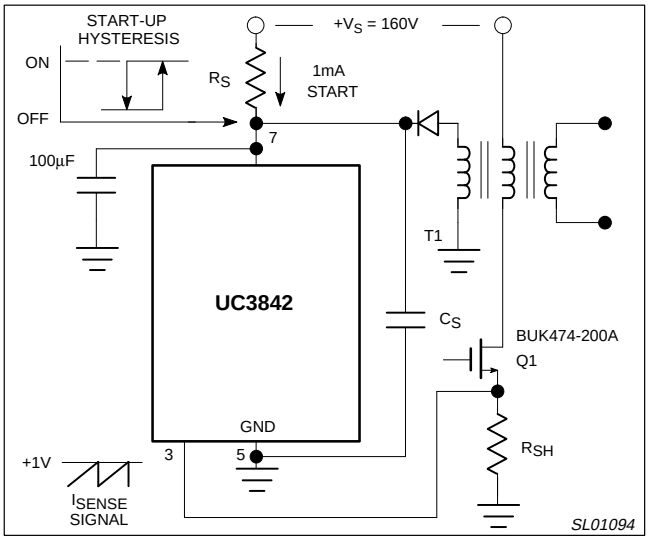



**Figure 7. Typical Output Circuit and Hysteresis**

## DESIGNING THE CONVERTER

### A 25W Flyback Example

With the flyback converter, energy is stored in the transformer primary flux field during the duty cycle on time. Primary current increases from the initial value at a rate determined by the primary inductance and the primary supply voltage. With current mode control, the maximum primary current under normal operating conditions must first be determined from the converter throughput power and estimated efficiency. For example, 25W converter with a primary supply voltage of 48V and expected efficiency of 75% will require:

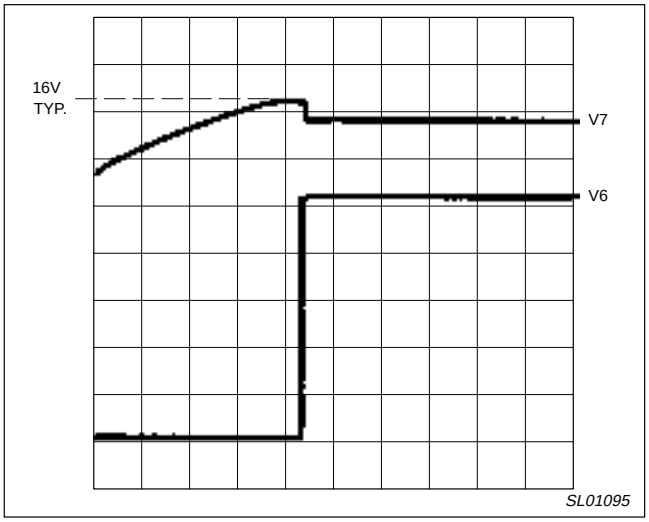



**Figure 8. Power-Up Sequence**

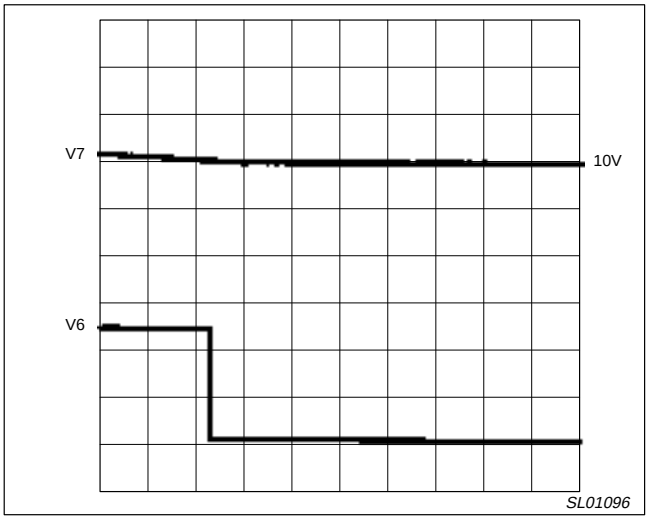



**Figure 9. Power-Down Sequence**

$$\text{Power In (avg)} = \frac{\text{Power Out (Watts)}}{\text{eff. (decimal)}} = \frac{25 \text{ Watts}}{0.75} = 33.3 \text{ Watts}$$

## Transformer Design Example

It is determined to use a Philips EC35-3C8 core set and to add the necessary gap to prevent core saturation. This calculation is derived from the core specifications as listed below for two core halves. (See Philips data on EC35 core.)

$\ell_E$ = 7.74cm, magnetic path length.
$A_E$ = .843cm$^2$, core area.
$A_L$ = 2250mH/1000T. Ind/Turn
$\mu_{AVE}$ = 1500 (approx). Permeability
(Reference Figure [14])

For a primary inductance of 200µH –

$$N_{PRI} = N_{REF}\sqrt{\frac{L_{PRI}}{L_{REF}}} = 1\ 10^3\sqrt{\frac{200\ 10^{-6}}{2.25}}$$

= 9.47Turns with zero gap core halves

However, this results in nearly 5V/turn. A value of 2V/turn is more optimal. Therefore, recalculating:

$$\frac{48V}{2V\ \text{Turn}} = 24 \text{ Turns}$$

$$L_P = \frac{(24)\ 2\ 2250mH}{1\ 10^6} = 1.3mH \text{ ungapped inductance}$$

The gap length may be calculated from maximum allowable flux, ($B_{MAX}$ = 3000 Gauss from Figure [14]) and peak current (I(DC) plus $\Delta I_{MAX}$), as follows: First find the magnetic path length, –

$$\ell_T = \frac{0.4\pi_I\ N_P\ I_{MAX}\ \mu_{AVE}}{B_{MAX}(\text{Gauss})} \text{ cm}$$

$$\ell_T = \frac{0.4(3.14)\ 24\ 3\ 1500_{AVE}}{3000} \text{ cm} = 45\text{cm}$$

Next, solve for the gap length,

$$\ell_{GAP} = \frac{\ell_T - \ell_E}{\mu_{AVE}}$$

$$\ell_{GAP} = \frac{(45 - 7.74)}{1500} = 25\ 10^{-3} \text{ cm}$$

$$\ell_{GAP_{inches}} = \frac{25\ 10^{-3}\text{cm}}{2.24\text{cm in.}} = 11 \text{ mils}$$

Note that this is the sum of two gaps in series, so use one-half this value for the shim thickness. (Two core legs in the magnetic path.) The shim (spacer) is made of mylar or other non-metallic material.

Calculating the gapped inductance of the primary –

$$L_P = \frac{0.4\pi\ N^2_P\ \mu_{AVE}\ A_E\ 10^{-8}}{\ell T(\text{cm})} = \frac{0.4\pi\ 24^2\ 1500\ 0.843\ 10^{-8}}{45}$$

= 203µH

## The Current Sense Resistor

Next, determine peak current in the primary at $D_{MAX}$ (Note: $D_{MAX}$ = duty cycle max.) Let $D_{MAX}$ equal 0.5 and $F_{SW}$, the oscillator frequency, equal 40kHz. This results in a period, T, of 25µs. Calculating $T_{ON}$, and $I_{PK}$ – requires an estimated value for primary inductance – choose LP equal 200µH. The primary supply is 48V.

$$I_{PEAK} = \frac{V_S\ D_{MAX}\ T_{ON}}{L_P} = \frac{48V\ 0.5\ 25\ 10^{-6}\text{sec}}{205\ 10^{-6}\text{H}}$$

= 2.9A

Next find the value of the shunt resistor necessary to reach the 1V current sense threshold at $D_{MAX}$ = 0.5,

$$R_{SH} = \frac{1V}{2.9A} = 0.33\Omega$$

Calculating power rating –

$$P_{SHUNT} = (2.9)^2\ (2)\ \frac{D_{MAX}}{3} = 3W(\text{ave})$$

(use 1W resistor)

## Core Losses

Core losses at 40kHz and 1500 Gauss (ave) flux are:

= (200mW/cu.cm) × 6.5cu.cm = 1.3W

48V primary – 24 turns (2 #25 cu. wire)

The circuit example is shown in Figure 11. The circuit is designed to run in the flyback mode using 48V input. The power FET is an Philips BUK474-200A rated at 200V, $V_{DS}$; 5.3A drain current maximum with 25W of power dissipation. $R_{DS(ON)}$ is 0.4Ω.

## External Synchronization

The use of external sync is necessary in certain systems such as multisync video monitors where sweep speed is locked to the SMPS converter switching rate to prevent noise transients from appearing on the screen. Other examples involve the use of multiple supplies in a distributed power system in which switching must run synchronously to prevent beat frequencies from appearing as FML on common ground buses. The circuit shown is simple and requires few parts (Figure 10). The input signal is AC coupled through a 100pF capacitor to Pin 4 of the UC3842. A pulse of 1V peak nominal amplitude and 100ns minimum is required to trigger the RC oscillator. The free running time base frequency is set to be lower than (longer period) the sync frequency by a minimum of 10% to allow reliable triggering. This then allows for statistical variations in external component tolerance and internal IC parameters. Note that the ramp amplitude will be reduced when using external sync due to the forced early termination of the charging time on the timing capacitor.

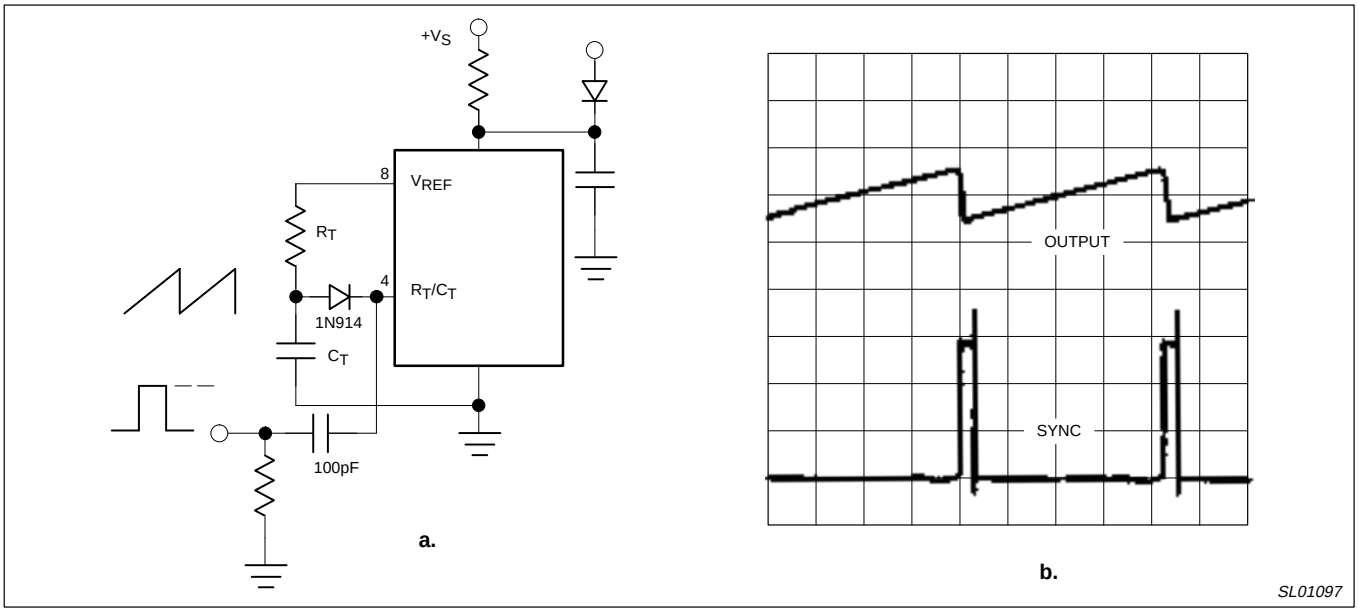



**Figure 10. External Synchronization and Waveforms**

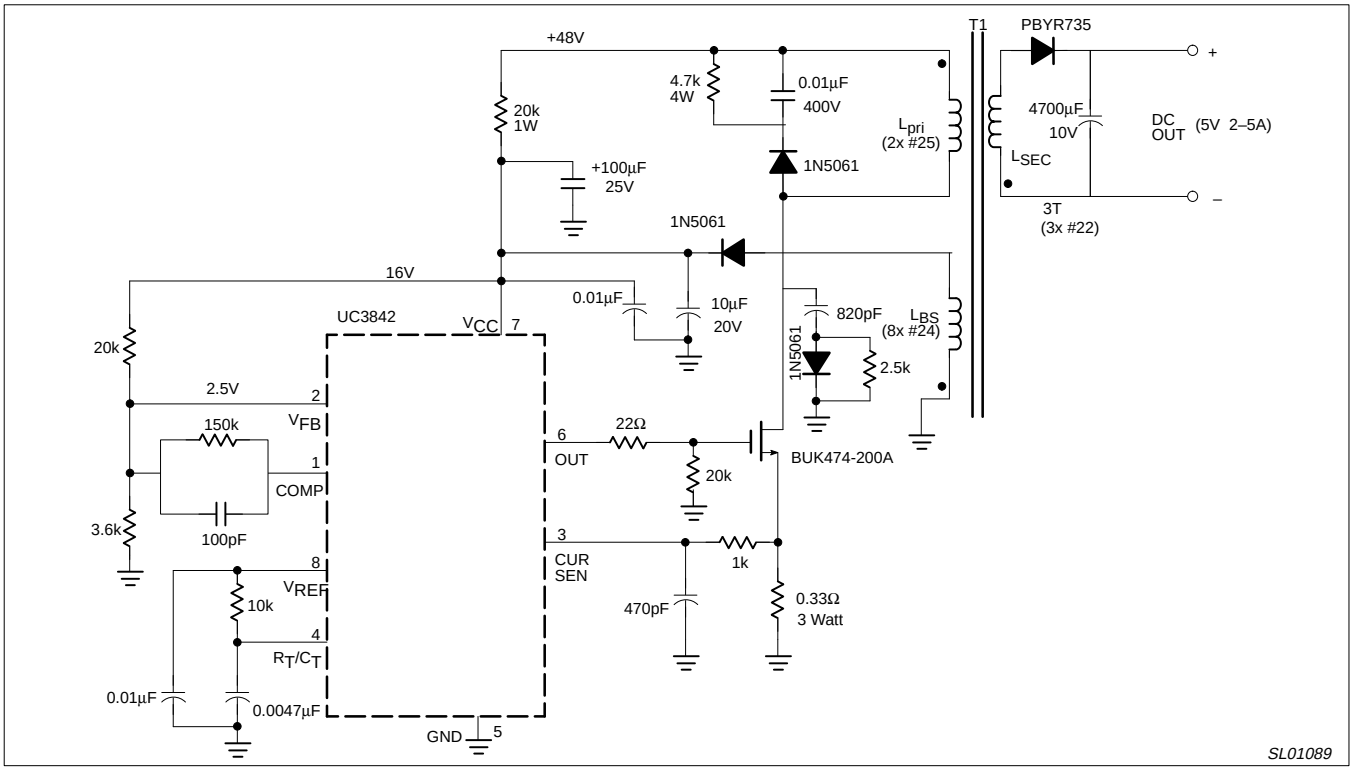



**Figure 11. Flyback Regulator with Shunt Regulated 5V Power Supply**