

# A NOVEL, LOW-COST IMPLEMENTATION OF "DEMOCRATIC" LOAD-CURRENT SHARING OF PARALLELED CONVERTER MODULES

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**Abstract** – A simple, low-cost, and robust "democratic" (autonomous) current-sharing circuit is proposed and analyzed. The circuit maintains good current sharing among the modules by properly adjusting the voltage references of the modules based on the differences between the average current of the paralleled modules and the currents of the individual modules. Design guidelines for achieving a desired current-sharing performance are given and verified on a number of dc/dc modules operating in parallel.

## 1 Introduction

Generally, the paralleling of lower-power converter modules offers a number of advantages over a single, high-power, centralized power supply. Performance-wise, the advantages include higher efficiency, better dynamic response due to a higher frequency of operation, and better load regulation. System-wise, paralleling allows for redundancy implementation, expandability of output power, and ease of maintenance. In fact, paralleling of standardized converter modules is the approach that is widely used in distributed power systems for both front-end and load converters.

When operating converter modules in parallel, the major concern is load-current sharing among the paralleled modules. A variety of approaches, with different complexity and current-sharing performance, were proposed, developed, and analyzed in the past [1] - [8]. Among these approaches, the most attractive are those which provide the desired current sharing without implementing a master/slave configuration or requiring a separate current-share controller. These "democratic" (also referred to as autonomous [2] or independent [6]) current-sharing approaches, which allow each module to operate either as a stand-alone unit or as a parallel module, make possible the implementation of true N+1 redundant systems.

Generally, democratic current sharing can be implemented using two approaches. The first approach, known as the "droop" approach [6, 7], relies on the internal (output) and/or externally added resistance of the paralleled modules to maintain a relatively equal current distribution among the modules. The droop

method can be implemented in a variety of schemes as described in [7]. It is simple to implement, and it does not require any communication (control-wire connection) between the paralleled modules. However, the major deficiency of the droop method is a poor load regulation. As a result, the droop method is not suitable for applications where a tight regulation is required.

The other method ensures the desired current sharing by adjusting the reference voltages of the voltage-feedback error amplifiers of the individual modules so that the deviations of the modules' currents from the average current are eliminated [1] - [6]. This current-sharing technique requires a single-wire communication (current-share bus) between the modules in order to provide the average current information to the current-share circuits of each module. An implementation of this current-share technique is described in detail in [5]. A modified circuit, which is used to implement an IC controller with current sharing function is presented in [6].

Generally, the "current-share-bus" technique employs an operational amplifier (current-error amplifier) in the low-bandwidth, current-share loop to generate a current-error signal which is used to adjust the reference voltage [2] - [6]. In addition, it requires sensing of the load currents (or currents proportional to the load currents) of the individual paralleled modules. To ensure the stability of the paralleled-module system, the current-share loop gain has to be properly tailored [2], [3]. Otherwise, the system may exhibit instabilities, especially during load transients [8]. However, even for a stable system, the operation of this type of current-sharing circuit may not be satisfactory due to its high sensitivity to the noise. In fact, the implementation of the circuit requires very careful layout and grounding considerations [6].

In this paper, a novel implementation of the current-share-bus technique is described. The main feature of the proposed implementation is that it does not employ the operational amplifier to generate the current-error signal. As a result, the circuit is inherently stable, robust, and cheaper to implement.

The paper also presents a detailed analysis of operation and design guidelines for achieving a desired current sharing. Finally, the proposed technique is verified on a number of experimental dc/dc modules

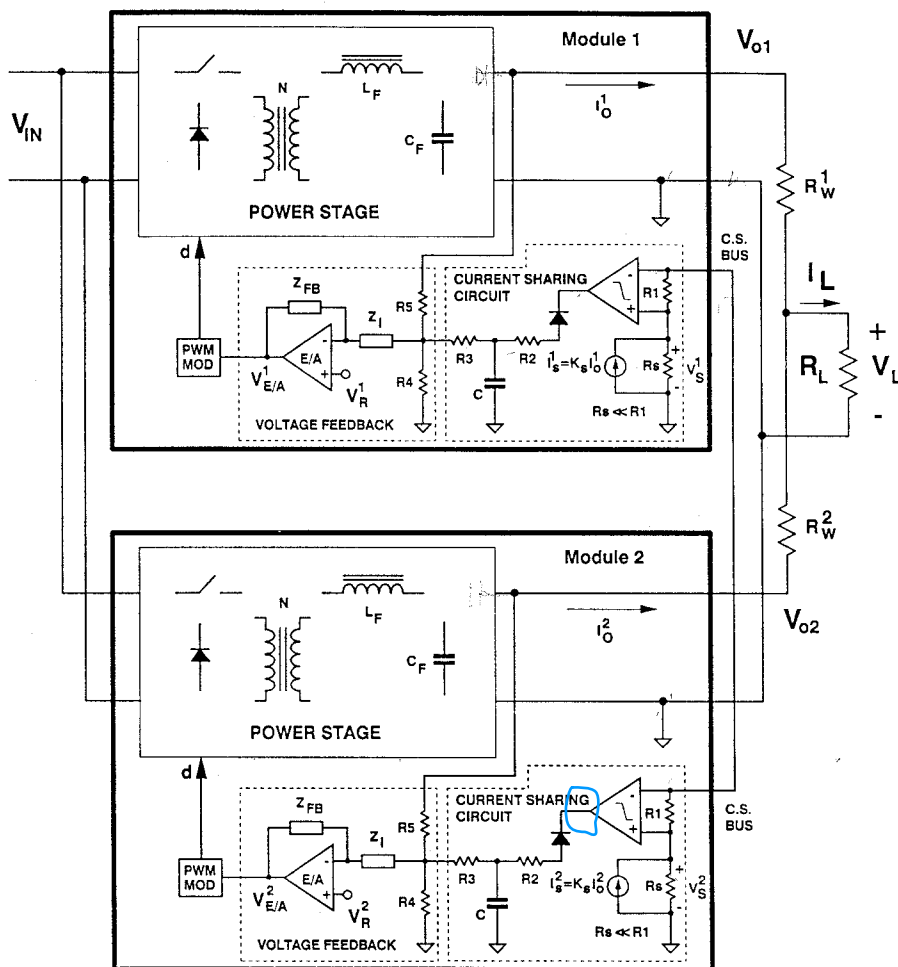


Fig. 1: Parallel connection of two dc/dc modules which employ proposed current-sharing circuits.  $R_w^1$  and  $R_w^2$  represent interconnect (cable) resistance between outputs of modules and load. If not stated otherwise, it is assumed that  $R_w^1 = R_w^2 = R_w$ .

operating in parallel.

## 2 Implementation and Analysis

The parallel connection of two dc/dc modules which employ the proposed current-sharing (CS) circuit is shown in Fig. 1. Instead of using an operational amplifier to process the current-error signal [2] - [6], the proposed circuit employs a comparator followed by a low-pass filter (passive integrator) consisting of  $R_2$ ,  $R_3$ , and  $C$ . Current source  $I_s$  represents the sensed current which needs to be proportional to the output current  $I_o$ , i.e.,  $I_s = K_s I_o$ , where  $K_s$  is the current sensing gain. If sensing resistor  $R_s$  is much smaller than  $R_1$  ( $R_s \ll R_1$ ), then the voltage across  $R_s$  is independent of  $R_1$ , and it is given by  $V_s = R_s I_s$ .

To achieve and maintain the desired current sharing, the CS circuits of the modules are connected through the current-share bus. The voltage on the

CS bus sets the desired output current of the modules.

In the next subsections, detailed explanations of operation, current-sharing accuracy, current-sharing loop stability, and effect on the output voltage of the proposed CS circuit are presented.

It should be pointed out that, although in the following analysis only the parallel connection of two modules is considered, the proposed CS approach is applicable to any number of modules connected in parallel. The only reason for focusing on the two-module parallel connection is to explain the principle of operation and the characteristics of the circuit in the simplest, easiest, and most obvious manner.

### 2.1 Principle of operation

To further facilitate the explanation of the CS operation, Fig. 2 shows only the current-sharing circuit of the modules.

Generally, the desired current distribution among

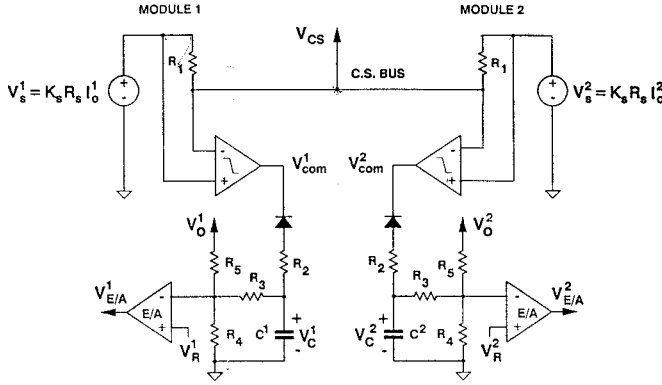


Fig. 2: Current-sharing circuits of two parallel modules shown in Fig. 1. If not stated otherwise, it is assumed that  $C^1 = C^2 = C$  and  $V_R^1 = V_R^2 = V_R$ .

the modules is achieved by comparing voltages across the sensing resistors  $V_S^1$  and  $V_S^2$  in the CS circuits of the individual modules with CS-bus voltage  $V_{CS}$ , and by appropriately adjusting the output voltages of the modules so that the differences between voltages  $V_S^1$  and  $V_S^2$ , and the CS-bus voltage are decreased to the desired levels. The output voltages are adjusted by voltages across capacitors  $C^1$  and  $C^2$ , which effectively change reference voltages  $V_R^1$  and  $V_R^2$  according to the duty cycle of the comparator-output voltages  $v_{com}^1$  and  $v_{com}^2$ .

Voltages  $V_S^1$  and  $V_S^2$  are proportional to the corresponding load currents, while the CS-bus voltage, according to Fig. 2, is

$$V_{CS} = \frac{V_S^1 + V_S^2}{2} = K_S R_S \frac{I_O^1 + I_O^2}{2}, \quad (1)$$

i.e., it is proportional to the average of the output currents of the individual modules. Therefore, the current-sharing circuit tries to maintain the output currents of individual modules equal to the average of these currents. This conclusion can be generalized for any number of modules in parallel.

Figure 3 shows the key steady-state waveforms of the CS circuit of two identical modules. Since the modules are identical, they are expected to share the load current perfectly. As can be seen from Fig. 3, the modules carry equal average output currents. However, their instantaneous output currents are different; i.e., the output-current waveforms contain 180° out-of-phase ac components. These ac current components are induced by the CS loop due to the inevitable ripple of the capacitor voltages  $v_C^1$  and  $v_C^2$ . Namely, when the comparator outputs in the CS circuits are high, capacitors  $C^1$  and  $C^2$  are charged through  $R_3$  with time constant  $\tau_{char} = CR_3$ . Similarly, when the comparators' outputs are low, the capacitors discharge through  $R_2$  with time constant  $\tau_{dischar} = C(R_2 || R_3)$ . The changes in capacitor volt-

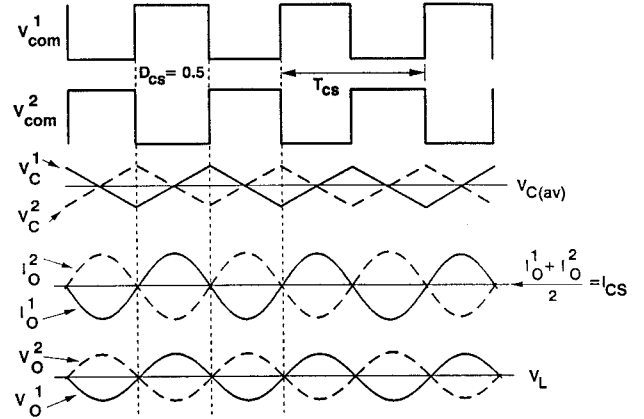


Fig. 3: Key waveforms of two identical ( $V_R^1 = V_R^2 = V_R$ ) parallel modules shown in Fig. 1 with relatively small capacitors  $C^1$  and  $C^2$  ( $C^1 = C^2 = C$ ).

ages  $v_C^1$  and  $v_C^2$  induce changes in the output voltages of the modules,  $v_O^1$  and  $v_O^2$ , which cause changes in output currents  $i_O^1$  and  $i_O^2$ .

For the two-module parallel connection, comparator outputs must be in the opposite states (i.e., if  $v_{com}^1$  is high,  $v_{com}^2$  must be low, and vice versa) because for one comparator the voltage across the sensing resistor (output current) must be higher than the CS-bus voltage, whereas for the other this voltage must be lower than the CS-bus voltage. The comparators change states when the instantaneous currents of the individual modules become equal to the average current of the modules. If the modules are identical, the duty cycles of comparator output voltages  $v_{com}^1$  and  $v_{com}^2$  are 50%. Generally, for any number of modules in parallel, at any given time, at least one of the comparators must be in the opposite state than the others.

The average capacitor voltage  $v_{C(av)} = V_C$  as a function of the duty cycle of the comparator output can be calculated from the equivalent charging/discharging circuit shown in Fig. 4 as

$$V_C = \frac{V_R}{1 + \frac{R_3}{R_2}(1 - D_{CS})} + V_F \frac{1 - D_{CS}}{\frac{R_2}{R_3} + 1 - D_{CS}} \quad (2)$$

where  $D_{CS}$  is the duty cycle of the comparator output voltage and  $V_F$  is the forward voltage drop of the

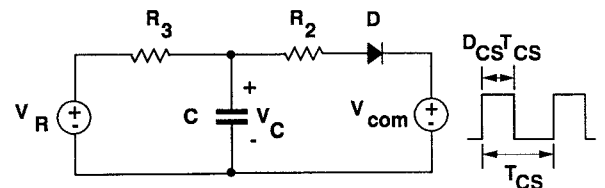


Fig. 4: Equivalent charging/discharging circuit.

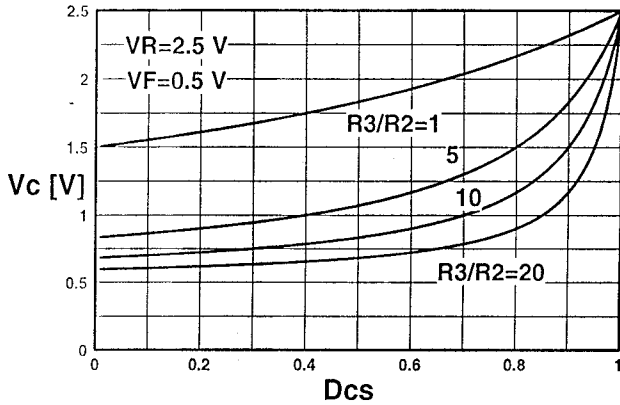


Fig. 5: Plot of  $V_C$  as function of  $D$ .

diode.

Figure 5 shows the plot of  $V_C$  as a function of  $D_{CS}$ . As can be seen, for small duty-cycle changes around  $D_{CS} = 0.5$ , the  $V_C$  dependence on  $D_{CS}$  is virtually linear for all  $R_3/R_2$  ratios. For duty cycles higher than 0.7 and  $R_3/R_2 \geq 5$ ,  $V_C$  increases rapidly toward the reference voltage ( $V_R = 2.5$  V). Finally, it should be noted that ratio  $R_3/R_2$  has no effect on  $V_C^{max} = V_R$  that occurs for  $D_{CS} = 1$ , but only on  $V_C^{min}$  that occurs at  $D_{CS} = 0$ . A smaller  $R_3/R_2$  ratio increases the  $V_C^{min}$  value, and therefore decreases the  $V_C$  range.

Furthermore, from Fig. 2, it can be derived that the output voltage of the module is dependent on the average capacitor voltage as

$$V_O = \left(1 + \frac{R_5}{R_4}\right)V_R + \frac{R_5}{R_3}(V_R - V_C) \quad (3)$$

As can be seen from Eq. (3), voltage  $V_C$  effectively changes the reference voltage of the voltage-feedback error amplifier. From Eqs. (2) and (3), the adjustment range  $\Delta V_O$  of  $V_O$ , assuming that  $R_3 \gg R_2$ , is

$$\begin{aligned} \Delta V_O &= V_O^{max} - V_O^{min} \\ &= V_O(@V_C^{min}) - V_O(@V_C^{max}) \\ &= \frac{R_5}{R_3}(V_R - V_F) \end{aligned} \quad (4)$$

Switching frequency  $f_{CS}$  of the comparators in the CS circuits, and therefore, also the ac component frequency in the output voltage and current waveforms, is determined by the frequency of the closed-loop complex poles of the output filter of the power stage. To facilitate the explanation of this claim, Fig. 6 shows the small-signal, block diagram of a module with the CS circuit.

In the circuit in Fig. 6, the CS circuit is modeled by a voltage source that represents the voltage waveform of the capacitor in the CS circuit. The ac component of this voltage source serves as the excitation signal to the close-loop circuit consisting of the error amplifier

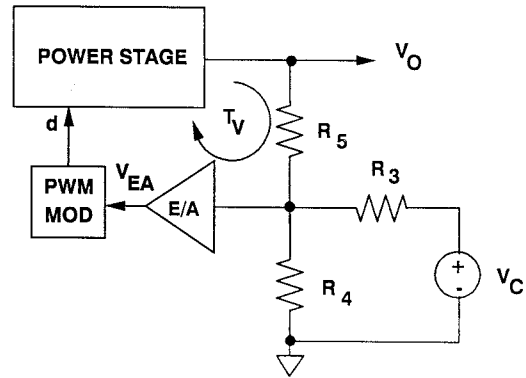


Fig. 6: Small-signal block diagram of module with current-share circuit.

(E/A), PWM modulator, power stage, and voltage divider ( $R_5$  and  $R_4$ ), which represents the output-voltage feedback loop. It should be noted that, generally, the PWM modulator can be of a current-mode type.

According to Fig. 6, a change in  $v_C$  (due to unavoidable charging or discharging of  $C$ ) will produce a response in output  $V_O$  at the frequency of the closed-loop complex poles of the power stage. As a result, the comparator in the CS circuit will switch at the same frequency. Generally, this frequency depends on the open-loop frequency of the complex poles of the power stage and the amount of feedback (E/A gain) and can be determined from the root locus plot of the voltage feedback loop.

Finally, Fig. 7 shows the key waveforms of the parallel connection of the two modules with the mismatched reference voltages (i.e.,  $V_R^1 > V_R^2$ ). As can be seen, the frequency of the ac current and voltage components is the same as for the case of equal references (Fig. 3). However, the duty cycles of the comparators are not equal. As a result, the average voltages of  $C^1$  and  $C^2$  are different, i.e.,  $V_C^1 > V_C^2$ .

## 2.2 Accuracy of current sharing

As illustrated in Fig. 3, the current sharing of two identical modules is, as expected, perfect. However, the modules which are not identical exhibit a current-sharing error, as can be seen in Fig. 7 for modules with slightly mismatched reference voltages. Namely, the difference in the reference voltages (or, generally, any other source of mismatching) calls for different average voltages of capacitors  $C^1$  and  $C^2$  to correct the mismatching. To obtain the required average capacitor voltages  $v_{C(av)}^1$  and  $v_{C(av)}^2$ , the duty cycle of comparator voltage  $v_{com}^1$  must be different than that of  $v_{com}^2$ . Since the comparators compare the instantaneous load currents of the individual modules with the average current of the modules, the only way to generate different duty cycles is to have the current waveforms shifted in the opposite directions with respect

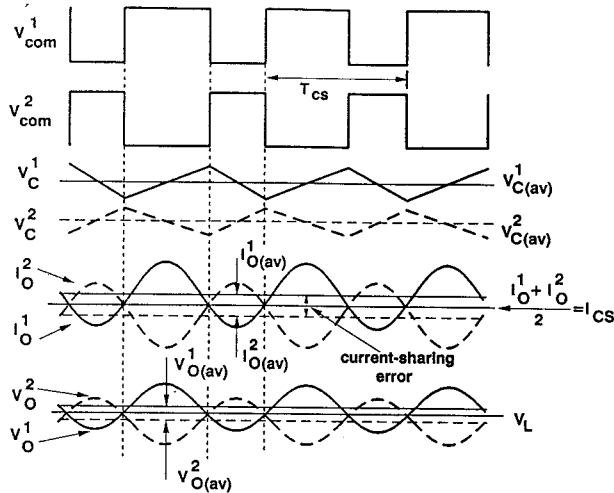


Fig. 7: Key waveforms of two parallel modules with mismatched references ( $V_R^1 > V_R^2$ ) and relatively small capacitors  $C^1$  and  $C^2$  ( $C^1 = C^2 = C$ ).

to the average current of the modules. If  $V_R^1 > V_R^2$ , the  $I_O^1$  waveform has to move up, and the  $I_O^2$  waveform has to move up for the same distance with respect to the average current level of  $I_{CS} = (I_O^1 + I_O^2)/2$  as can be seen from Figs. 3 and 7. Since the ac components of the output voltages are  $v_O^1 = R_w^1 i_O^1$  and  $v_O^2 = R_w^2 i_O^2$ , where  $R_w^1 = R_w^2 = R_w$  are the resistances of the cables connecting the individual outputs with the load as shown in Fig. 1, the output voltages also shift with respect to each other, as can be seen from Fig. 7. The shifting of the waveforms not only introduces a difference in the duty cycles of the comparators, but also introduces a difference between the dc components of individual output currents, i.e., creates a current-sharing error. This error is smaller if the ac components of the individual output currents are smaller. Since, according to Fig. 6, the magnitude of the ac output-current component is proportional to the magnitude of the ac component of capacitor voltages  $v_C^1$  and  $v_C^2$ , the current-sharing error can be controlled by proper selection of the capacitor values. Generally, larger values of  $C^1$  and  $C^2$  are required for higher accuracy.

Figure 8 shows the waveforms of the same two modules as in Fig. 7, but with larger capacitors  $C^1 = C^2 = C$ . As can be seen, the ac components of capacitor voltages  $v_C^1$  and  $v_C^2$  are very much reduced. As a result, the ac components of the output currents, and consequently, the current-sharing error are also reduced compared to Fig. 7.

### 2.3 Stability

Due to the presence of the comparator in the CS loop, the CS loop is inherently stable if the voltage-feedback loop is stable within the range of the effective voltage

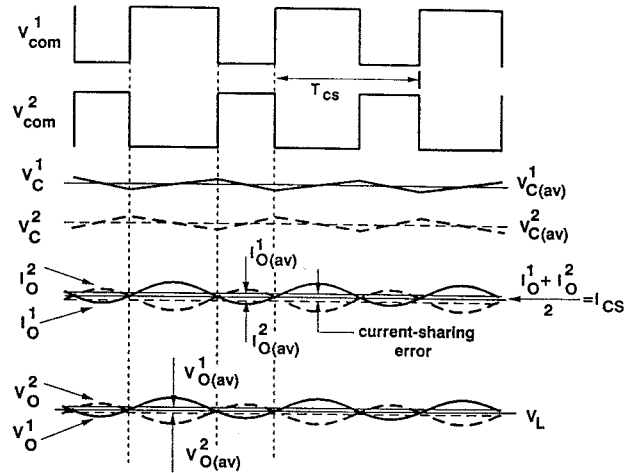


Fig. 8: Key waveforms of two parallel modules with same mismatched references ( $V_R^1 > V_R^2$ ) as in Fig. 7 and five times larger capacitors  $C^1$  and  $C^2$  ( $C^1 = C^2 = C$ ) compared to those in Fig. 7.

reference change. Namely, according to Fig. 6, the magnitude of the ac component of the output current (voltage) is dependent on the gain of the voltage-feedback loop and the magnitude of the ac component of capacitor voltage  $v_C$ . Since the magnitude of the ac component of  $v_C$  is bounded and independent of the CS loop gain, it follows that the magnitude of the ac component of the output current is proportional to the magnitude of the ac component of  $v_C$ , if the voltage-feedback loop is stable. As pointed out earlier, the magnitude of the output current ac component can be controlled by properly selecting charging  $\tau_{char}$  and  $\tau_{disch}$  time constants.

### 2.4 Effect on output voltage

As shown in Fig. 3, when two identical modules are connected in parallel, their effective reference voltages will change for the same amount because the CS-loop comparators will switch with 50% duty cycle. Therefore, the output voltages of the modules after paralleling will stay equal but will assume different values than before paralleling. As a result, the load voltage will also change due to the paralleling. Whether the output voltages after paralleling will be higher or lower than before paralleling depends on the output-voltage adjustment procedure before paralleling. If the output voltages are adjusted while the CS bus is held low, the output voltages will increase after the paralleling. If the CS bus is held high during the output-voltage adjustment, the output voltages will decrease after the paralleling. To help explain this claim, Fig. 9 shows the load regulation curves of two identical modules for the above-mentioned adjustments of the output voltage. The separation of

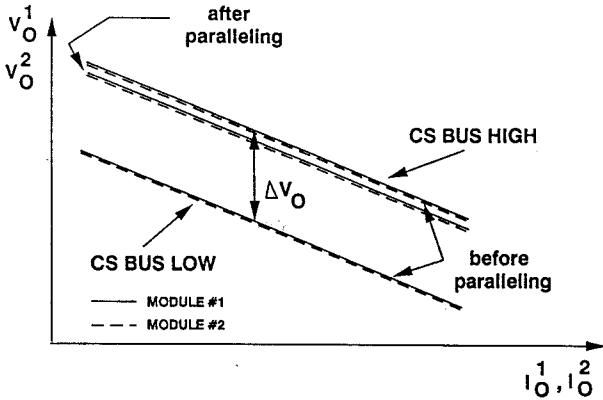


Fig. 9: Load regulation lines for two identical modules before and after paralleling. For clarity, lines are shown slightly apart, although for identical modules they actually coincide.

the curves before paralleling  $\Delta V_O$  for the adjustments with low and high  $V_{CS}$  can be calculated from Eq. (4). Since the modules are identical, the corresponding curves for both modules coincide with each other. When the modules are connected in parallel, capacitor voltages  $V_C^1$  and  $V_C^2$  change for the same amount due to 50% duty cycle operation, causing the output voltages to shift equally from their values before paralleling, as shown in Fig. 9.

As can be seen from Fig. 5,  $V_C$  at  $D_{CS}=0.5$  is only slightly different than  $V_C$  at  $D_{CS}=0$  if  $R_3/R_2 \gg 1$ , i.e., when  $V_{CS}$  is held high. However,  $V_C$  at  $D_{CS}=0.5$  is much lower than  $V_C$  at  $D_{CS}=1$ , i.e., when  $V_{CS}$  is held low. As a result, the shift of the output voltages after paralleling is smaller if the adjustment is done when the CS bus is held high and the ratio  $R_3/R_2$  is selected to be high ( $\geq 10$ ). This is seen clearly in Fig. 9, where the load regulation lines of the modules after paralleling are closer to the regulation lines that correspond to the adjustment with the CS bus held high.

This conclusion can be generalized for any number of modules in parallel. Of course, the voltage shift depends on the number of modules, adjustment procedure, and the output-voltage adjustment range given by Eq. (4). Generally, the voltage shift decreases as the number of modules increases.

### 3 Design Guidelines

The design of the CS circuit requires a proper selection of resistors  $R_S$ ,  $R_1$ ,  $R_2$ , and  $R_3$  and of capacitor  $C$ .

The value of  $R_S$  is determined by the choice of the sensing network and its gain. While the resistive sensing is a viable approach to sensing low currents, the transformer sensing is a more practical approach to

sensing larger currents. In fact, for modules that employ a current-mode control, the existing current sensing device can be also used for the CS loop sensing. To avoid the dependence of the sensed voltage  $V_S$  on the value of  $R_1$ ,  $R_1$  should be selected much larger than  $R_S$ . A good choice is to select  $R_1$  ten to twenty times larger than  $R_S$ . Finally, it should be noted that  $R_S$  and  $R_1$  need to be high-precision (small tolerance) resistors since the differences in their values affect the accuracy of current sharing.

Resistors  $R_2$  and  $R_3$ , for given voltage divider resistors  $R_4$  and  $R_5$ , set the range of the output voltage. This range must be within the specified regulation range,  $V_O^{min} - V_O^{max}$  of the modules. Assuming that  $R_3 \gg R_2$  and that the adjustment range of the output voltage is equal to the regulation range, i.e.,  $\Delta V_O = V_O^{max} - V_O^{min}$ ,  $R_3$  can be calculated by solving Eq. (3) as

$$R_3 = R_5 \frac{(V_R - V_F)}{V_O^{max} - V_O^{min}}. \quad (5)$$

To satisfy  $R_3 \gg R_2$ ,  $R_2$  should be selected at least 10 times smaller than  $R_3$ .

With the above calculated values for resistors  $R_2$  and  $R_3$ , the CS circuit can maintain the desired current sharing for mismatched modules whose output voltages before paralleling are within the specified regulation range when their CS-bus lines are held low, as long as the cable resistances that connect the outputs of individual modules to the load ( $R_w$  in Fig. 1) are the same. Otherwise, this range can be smaller or larger, depending on the cable resistance differences [8].

As described in Sec. 2.2, the value of capacitor  $C$  determines the accuracy of the current sharing. Generally, higher values of  $C$  result in better current sharing. However, the transient response of the CS loop becomes slower as the value of  $C$  is increased. As a result, the dynamic current-sharing performance may degrade for excessively large values of  $C$ . Therefore, the minimum value of  $C$  which meets the desired accuracy spec should be taken. To determine this value analytically, it is necessary to know the closed-loop gain of the voltage-feedback loop at the current-share loop frequency. Without resorting to the computation of this gain, a good rule-of-thumb value for the capacitor selection is that the capacitor voltage peak-to-peak ripple should be kept below 1% of the dc level to achieve current-sharing accuracies of around 1%.

Finally, the selection of the comparator in the CS circuit does not require any special considerations. Since the CS loop is a slow loop, the comparator speed is not critical, and therefore, a cheap, all purpose comparator can be used. In fact, to further reduce the component count, an open-collector comparator without a pull-up resistor can be used. The operation of the CS circuit is identical with that with the comparator with a pull-up resistor, except that the comparator output voltage  $v_{com}$  in the high state follows the ca-

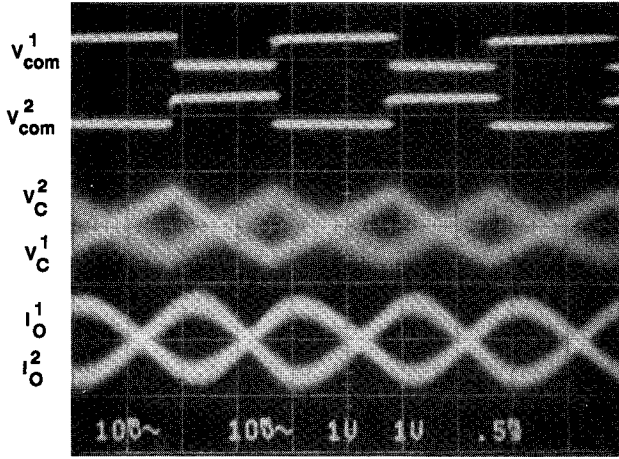


Fig. 10: Oscilloscope waveforms of key signals of two experimental modules connected in parallel with identical references  $V_R^1 = V_R^2 = 2.5$  V and  $C^1 = C^2 = C = 330$  nF at  $V_{in} = 48$  V and  $I_L = 10$  A. Scales:  $v_{com}$  - 1 V/div;  $v_C$  - 50 mV/div;  $I_O$  - 0.1 A/div.

capacitor voltage instead of being pulled up all the way to the rail voltage. Lastly, since the comparator does not have any hysteresis, it requires a filter at the input terminals to eliminate false triggering due to the noise.

## 4 Experimental Evaluation

To evaluate the performance of the proposed CS circuit, three identical experimental 5V/15A, dc/dc forward converters operating at 300 kHz were built for the input voltage range from 40 V to 60 V. The following components for the CS and the voltage-feedback control circuits, according to labeling in Fig. 1, were used:  $R_S = 0.1$  K,  $R_1 = 1$  K,  $R_2 = 4.3$  K,  $R_3 = 100$  K,  $C = 220$  nF,  $R_4 = R_5 = 10$  K,  $Z_I = R_I = 1$  K, and  $Z_{FB} = C_{FB} = 22$  nF. The values of the major components of the power stage are: turns ratio of the transformer  $N = 2.5$ , filter inductor  $L_F = 15$   $\mu$ H, and  $C_F = 4700$   $\mu$ F. The control was implemented using the current-mode controller UC3825. The information about the output current was obtained indirectly by measuring the primary current. The sensing was done by using the same current transformer which was used to implement the current-mode control.

Figure 10 shows the oscilloscope waveforms of two experimental modules connected in parallel. As can be seen, the frequency of the current-share loop is around 500 Hz, which represents the frequency of the closed-loop complex poles of the power stage (note that natural undamped frequency of open-loop complex poles of the power stage is  $f_O = 1/\sqrt{L_F C_F} \approx 600$  Hz). The waveforms in Fig. 10 are in good agreement with those in Fig. 3 except that in the oscilloscope, the crossovers of the load-current

waveforms occur before the moments the comparators change states. This is caused by the delay introduced by an RC noise-filtering network at the input of the comparators. With reference to Fig. 2, this filter consists of resistor  $R_n = 10$  K, connected in series with the positive input of the comparator and capacitor  $C_n = 10$  nF, connected right across the comparator input terminals.

Table 1 summarizes the current-sharing measurements for two paralleled modules with mismatched references ( $V_R^1 = 2.5$  V,  $V_R^2 = 2.45$  V) without and with the current-sharing circuits connected. As can be seen, the CS circuit dramatically improves the load-current distribution among the modules. The relative current-sharing error,  $|I_{O(dc)}^1 - I_{O(dc)}^2|/(I_L/2)$ , when the CS buses are not connected is in the 20% to 135% range, depending on the load current. With the CS-busses connected, the current-sharing error decreases significantly. For  $C^1 = C^2 = 330$  nF, the current-sharing error reduces to 7.2% at light load ( $I_L = 5$  A) and to 0.8% at full load ( $I_L = 30$  A). As explained earlier, larger values of  $C^1 = C^2$  decrease the ac components of the output currents ( $I_{O(ac)}^1$ ,  $I_{O(ac)}^2$ ), and, consequently, give better current-sharing accuracies. For  $C^1 = C^2 = 1.5$   $\mu$ F, the current-sharing accuracy is better than 1% in the entire load range. At the same time, the measurements of the dynamic current sharing during large load transients (from 10% to 100%) showed no noticeable increase in the current-sharing error.

Finally, Table 2 summarizes the experimental results for a parallel connection of three experimental modules with the mismatched reference voltages ( $V_R^1 = 2.5$  V,  $V_R^2 = 2.475$  V, and  $V_R^3 = 2.45$  V). As in the case of two paralleled modules, the CS circuit dramatically decreases the current-sharing error. Without the CS buses connected, the current-sharing error is in the 26% to 176% range. However, when the CS busses are connected, the current sharing error reduces to 10.4% at light load ( $I_L = 7.5$  A) and to 2.2% at full load ( $I_L = 45$  A). It should be noted that in the entire load range, the maximum absolute current-sharing error  $\max |I_{O(dc)}^i - I_{O(dc)}^j|$  is less than 330 mA.

The larger relative current-sharing errors in the three-module parallel connection compared to those in the two-module connection are caused by small differences in the power stage parameters of Module #3 compared to the other modules. Namely, as pointed out earlier, in the experimental converters, the measurements of the output currents were done indirectly by sensing the primary currents. As a result, any mismatching of the power stage parameters such as, for example, transformer magnetizing inductance and turns ratio and/or efficiency, introduces errors in the output currents of the modules. If the output currents are directly measured, the differences in the power stage parameters do not affect the accuracy of the current sharing.

Without CS Bus Connected						With CS Bus Connected													
						C=330 nF						C=1.5 μF							
$I_L$ (A)	$I_o^1$ (A)	$I_o^2$ (A)	$V_o^1$ (V)	$V_o^2$ (V)	Error (%)	$I_{o(dc)}^1$ (A)	$I_{o(ac)}^1$ (A)	$I_{o(dc)}^2$ (A)	$I_{o(ac)}^2$ (A)	$V_o^1$ (V)	$V_o^2$ (V)	Error (%)	$I_{o(dc)}^1$ (A)	$I_{o(ac)}^1$ (A)	$I_{o(dc)}^2$ (A)	$I_{o(ac)}^2$ (A)	$V_o^1$ (V)	$V_o^2$ (V)	Error (%)
5	4.19	0.81	4.99	4.91	135.0	2.59	0.09	2.41	0.09	5.11	5.10	7.2	2.50	0.03	2.50	0.03	5.10	5.10	0.00
10	6.65	3.35	4.99	4.91	66.0	5.10	0.09	4.90	0.09	5.11	5.10	4.0	5.01	0.03	4.99	0.03	5.11	5.10	0.40
15	9.10	5.90	4.99	4.91	42.6	7.61	0.08	7.39	0.08	5.11	5.10	2.9	7.52	0.03	7.48	0.03	5.11	5.10	0.53
20	11.54	8.46	4.99	4.91	30.8	10.12	0.08	9.88	0.08	5.11	5.10	2.4	10.04	0.03	9.96	0.03	5.11	5.10	0.80
25	13.95	11.05	4.99	4.90	23.2	12.62	0.08	12.38	0.08	5.11	5.10	1.9	12.55	0.02	12.45	0.02	5.11	5.10	0.80
30	16.34	14.66	4.99	4.90	17.8	15.12	0.08	14.88	0.08	5.11	5.09	0.8	15.04	0.02	14.96	0.02	5.11	5.10	0.53

Table 1: Measured current-sharing performance of two paralleled experimental modules with mismatched references ( $V_R^1=2.5$  V,  $V_R^2=2.45$  V). Relative current-sharing error in % is defined as  $[|I_{O(dc)}^1 - I_{O(dc)}^2| / (I_L/2)] 100\%$ .

Without CS Bus Connected								With CS Bus Connected						
								C=1.5 μF						
$I_L$ (A)	$I_o^1$ (A)	$I_o^2$ (A)	$I_o^3$ (A)	$V_o^1$ (V)	$V_o^2$ (V)	$V_o^3$ (V)	Error (%)	$I_o^1$ (A)	$I_o^2$ (A)	$I_o^3$ (A)	$V_o^1$ (V)	$V_o^2$ (V)	$V_o^3$ (V)	Error (%)
7.5	2.02	0.54	4.94	5.00	4.96	5.09	176.0	2.54	2.61	2.35	5.09	5.09	5.09	10.4
15.0	4.57	3.10	7.33	5.00	4.96	5.09	84.6	5.06	5.10	4.84	5.09	5.09	5.09	5.2
22.5	7.11	5.70	9.69	5.00	4.96	5.09	53.2	7.58	7.58	7.34	5.09	5.08	5.09	3.2
30.0	9.66	8.32	12.02	5.00	4.95	5.09	37.0	10.11	10.06	9.83	5.09	5.08	5.09	2.8
37.5	11.87	11.70	13.93	5.00	4.99	5.09	17.8	12.62	12.56	12.32	5.08	5.07	5.09	2.4
45.0	13.05	17.00	14.95	5.00	5.12	5.09	26.3	15.13	15.07	14.80	5.08	5.07	5.09	2.2

Table 2: Measured current-sharing performance of three paralleled experimental modules with mismatched references ( $V_R^1=2.5$  V,  $V_R^2=2.475$  V,  $V_R^3=2.45$  V). Relative current-sharing error in % is defined as  $[\max |I_{O(dc)}^i - I_{O(dc)}^j| / (I_L/3)] 100\%$ .

## 5 Summary

A simple, low-cost, and robust "democratic" current-sharing circuit is proposed and analyzed. Detailed explanations of operation, current-sharing accuracy, current-sharing loop stability, and the effect on the output voltage of the proposed circuit are presented. The current-sharing performance of the proposed scheme is evaluated experimentally on the parallel connection of two and three, 5V/15A, forward converter modules.

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