AN1757
APPLICATION NOTE

SWITCHING FROM THE L6561 TO THE L6562

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1.0 INTRODUCTION

Conceived on the same core of the L6561 and pin-to-pin compatible with it (see fig. 1), the L6562 is the new ST's Transition Mode (TM) controller for high Power Factor Corrector stages: the replacement can be done with minimum or no modification of a stage designed with the L6561.
As the building blocks of these two IC's are the same (fig. 1), one can design with the L6562 using the guidelines given for L6561, in particular in the ST Application Note 966 ("L6561, enhanced transition mode power factor corrector"). All the documentation produced for L6561 can be easily adapted to the L6562 ([1] [2] [3] [4]).

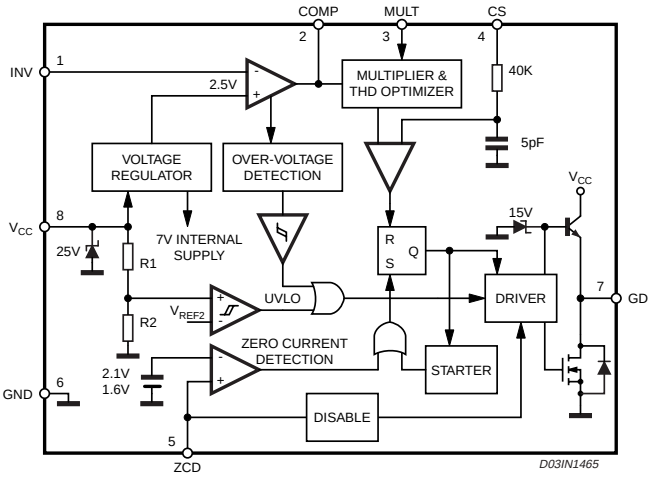
The first paragraph of this Application Note is dedicated to explain the differences in terms of Electrical Characteristics between these two controllers: it will be clear that these modifications do not require component changing when switching from L6561 to L6562.
Besides providing good results in term of power factor, this new IC considerably reduces the Total Harmonic Distortion (THD) without need for external components: an innovative circuit improves the behavior of the system reducing the conduction dead-angle that occurs to the AC input current near the zero-crossings of the line voltage (paragraph 3) making easier the compliancy with regulation.

The increased gate driver capability (typically 600mA sourcing and 800mA sinking) makes the L6562 suitable for a wide range of applications (with output power up to 300W).Based on that, L6562 can be fit the following applications: Lighting, IEC61000-3-2 compliant SMPS (TV, Desktop, PC, Monitors…), hi-end AC-DC adapter/ charger, entry level server & web server.

2.0 L6562 VS. L6561: ELECTRICAL CHARACTERISTICS DIFFERENCES

A series of tables will follow highlighting the differences between L6561 and L6562 in terms of Electrical Characteristics; at the end of each section, a short description explains the impact of these differences on the application and the consequent benefits.

Figure 1. Block Diagram



ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test condition	L6561			L6562			Unit
			Min	Typ	Max	Min	Typ	Max	
SUPPLY VOLTAGE									
V_{CC}	Operating range	After turn-on	10.3		18	10.3		22	V
V_Z	Zener voltage	for L6561: I_{CC}=25mA for L6562: I_{CC}=20mA	18	20	22	22	25	28	V

The supply voltage upper limit is extended to 22V (min.) to provide more headroom for supply voltage changes. This also makes it easier to fit the supply voltage of the L6562 to that of the cascaded DC-DC converter control IC.

SUPPLY CURRENT									
Symbol	**Parameter**	**Test condition**	**L6561**			**L6562**			**Unit**
$I_{START-UP}$	Start-up current	before turn-on (V_{CC} =11V)	20	50	90		40	70	µA
I_Q	Quiescent current	After turn-on		2.6	4		2.5	3.75	mA
I_{CC}	Operating Supply Current	@ 70KHz		4	5.5		3.5	5	mA
I_Q	Quiescent current	During OVP (either static or dynamic) or V_{ZCD} ≤150mV			2.1			2.2	mA

The consumption of the chip has been reduced providing an advantage in terms of power dissipation on the start-up resistors, if used, and consumption of the self-supply circuit.

MULTIPLIER INPUT									
Symbol	**Parameter**	**Test condition**	**L6561**			**L6562**			**Unit**
K	Gain	V_{MULT} =1V, V_{COMP}=4V	0.45	0.6	0.75	0.5	0.6	0.7	1/V

The improved control process allows reducing the statistical spread of this parameter; this change does not impact on the application design but improves reliability of IC's quiescent point

ERROR AMPLIFIER									
Symbol	**Parameter**	**Test condition**	**L6561**			**L6562**			**Unit**
I_{COMP}	Source Current	V_{COMP}=4V, V_{INV}=2.4V	-2	-4	-8	-2	-3.5	-5	mA
V_{COMP}	Upper clamp voltage	I_{SOURCE}=0.5mA		5.8		5.3	5.7	6	V
	Lower clamp voltage	I_{SINK} = 0.5 mA		2.25		2.1	2.25	2.4	V

The improved control process allows reducing the statistical spread of this parameter; this change does not impact on the application design but improves reliability of IC's quiescent point.

CURRENT SENSE COMPARATOR									
Symbol	**Parameter**	**Test condition**	**L6561**			**L6562**			**Unit**
$td_{(H-L)}$	Delay to Output			200	450		200	350	ns
	Current sense offset			0	15				mV
		V_{COMP}=0V					30		mV
		V_{COMP}=2.5V					5		mV

The **maximum propagation delay** (Delay to output) of the current loop has been reduced: this provides advantages at both light load (lowering the minimum duty cycle) and heavy load (reducing the amount of peak inductor current exceeding the programmed value).

Offset of the current sense comparator: in the L6561 it depends on the manufacturing process; in the L6562 such parameter is kept under control because it defines the amount of correction introduced by the internal THD corrector circuit (see paragraph "3. THD optimizer circuit").

ZERO CURRENT DETECTOR									
Symbol	**Parameter**	**Test condition**	**L6561**			**L6562**			**Unit**
V_{ZCDH}	Upper clamp voltage	for L6561: I_{ZCD}=-3mA for L6562: I_{ZCD}=-2.5mA	4.7	5.2	6.1	5.0	5.7	6.5	V
I_{ZCDsrc}	Source current capability		-3		-10	-2.5		-5.5	mA
I_{ZCDsnk}	Sink current capability		3		10	2.5			mA
V_{ZCDen}	Restart threshold							350	mV
I_{ZCDres}	Restart current after disable		-100	-200	-300	30	75		µA

Upper clamp voltage: the change does not have impact on the application design; it just reflects a change of internal structure that reduces temperature drift.

The **source and sink current capabilities** for the L6562 are lower than the relevant in the L6561: this is the effect of the reduced spread of these two parameters. From the application design point of view this leads to a higher value for the minimum resistance connected between the auxiliary winding and the ZCD pin (R6 in the schematic of Figure 5). Generally this is not a key issue because the value for this resistor is kept much higher than the minimum calculated, to achieve optimum MOSFET turn-on.

The **restart threshold,** not specified in the L6561 though present, is specified in the L6562.

The **restart current after disable** has been reduced to limit IC consumption while disabled.

STARTER									
Symbol	**Parameter**	**Test condition**	**L6561**			**L6562**			**Unit**
t_{START}	Start Timer period		70	150	400	75	130	300	µs

The improved control process allows reducing the statistical spread of this parameter; this change does not impact on the application design

OUTPUT OVERVOLTAGE									
Symbol	**Parameter**	**Test condition**	**L6561**			**L6562**			**Unit**
Hys.	Dynamyc OVP Hysteresys						30		µA

This parameter, not specified in the L6561 though present, is specified in the L6562

ELECTRICAL CHARACTERISTICS (continued)

GATE DRIVER									
Symbol	**Parameter**	**Test condition**	**L6561**			**L6562**			**Unit**
V_{OH}	Dropout voltage	$I_{Gdsource}$ = 20 mA		0.7	1		2	2.6	V
		$I_{GDsource}$ = 200 mA		1.2	2		2.5	3	V
V_{OL}		I_{GDsink} = 200 mA			1.5		0.9	1.9	V
tf	Current fall time			40	100		30	70	ns
tr	Current rise time			40	100		40	80	ns
V_{Oclamp}	Output clamp voltage	$I_{GDsource}$ = 5mA; Vcc = 20V	not present			10	12	15	V
(*)	I_{GD} Sink Current	V_{CC} =3.5V V_{GD} = 1V	5	10					mA
(*)	UVLO saturation	Vcc = 0 to Vccon, I_{sink}=10mA						1.1	V

Dropout voltage: this is a fixed offset due to the internal driver structure that has been changed.

Current Rise and fall time: the driver modification has led to a lower driver dynamic resistance and the effect is the reduction of fall and rise time of the driver current.

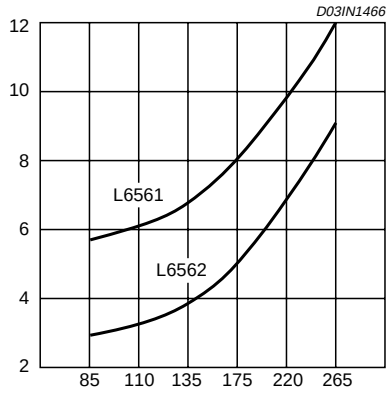
Output Clamp voltage: the high-level voltage of this pin is clamped at about 12V to avoid excessive gate voltages in case the pin is supplied with a high Vcc.

(*): the aim of this feature is to avoid undesired MOSFET turn-on due to spurious spikes when the IC is under UVLO condition. In the L6561 this feature is characterized through the current that the GD pin is able to sink under the given test conditions.
For the L6562 it is guaranteed that over the whole UVLO range, the GD pin is able to sink up to 10mA without exceeding 1.1V, a voltage definitely lower than the turn-on threshold of the MOS.

3.0 THD OPTIMIZER CIRCUIT

The L6562 is equipped with a special circuit that reduces the conduction dead-angle occurring to the AC input current near the zero-crossings of the line voltage (crossover distortion). In this way the THD (Total Harmonic Distortion) of the current is considerably reduced, as shown in fig. 2.

Figure 2. L6562 vs. L6561: THD



A major cause of this distortion is the inability of the system to transfer energy effectively when the instantaneous line voltage is very low. This effect is magnified by the high-frequency filter capacitor placed after the bridge rectifier, which retains some residual voltage that causes the diodes of the bridge rectifier to be reverse-biased and the input current flow to temporarily stop.

To overcome this issue, the circuit embedded in the L6562 forces the PFC pre-regulator to process more energy near the line voltage zero-crossings as compared to that commanded by the control loop. This will result in both minimizing the time interval where energy transfer is lacking and fully discharging the high-frequency filter capacitor after the bridge.

Figure 3 shows the THD corrector circuit block diagram and the waveforms in the significant points; the multiplier has two inputs: the first one is a fraction of the rectified input voltage and the second one is the output of L6562 error amplifier. The multiplier output is the product of these two quantities and (ideally) is a rectified sinusoid whose peak amplitude decreases by increasing the input voltage.

This waveform represents the threshold that the current sense voltage must cross to trigger the PWM comparator (see fig. 1).

Essentially the THD improvement circuit artificially increases the ON-time of the power switch with a positive offset added to the output of the multiplier in the proximity of the line voltage zero-crossings. This offset is reduced as the instantaneous line voltage increases, so that it becomes negligible as the line voltage moves toward the top of the sinusoid.

The effect of the circuit is shown in the figure 4, where the key waveforms of a standard TM PFC controller are compared to those of the L6562.

To maximally benefit from the THD optimizer circuit, the high-frequency filter capacitor after the bridge rectifier should be minimized, compatibly with EMI filtering needs. A large capacitance, in fact, introduces a conduction dead-angle of the AC input current in itself - even with an ideal energy transfer by the PFC pre-regulator - thus making the action of the optimizer circuit little effective.

Figure 3. THD corrector: block diagram

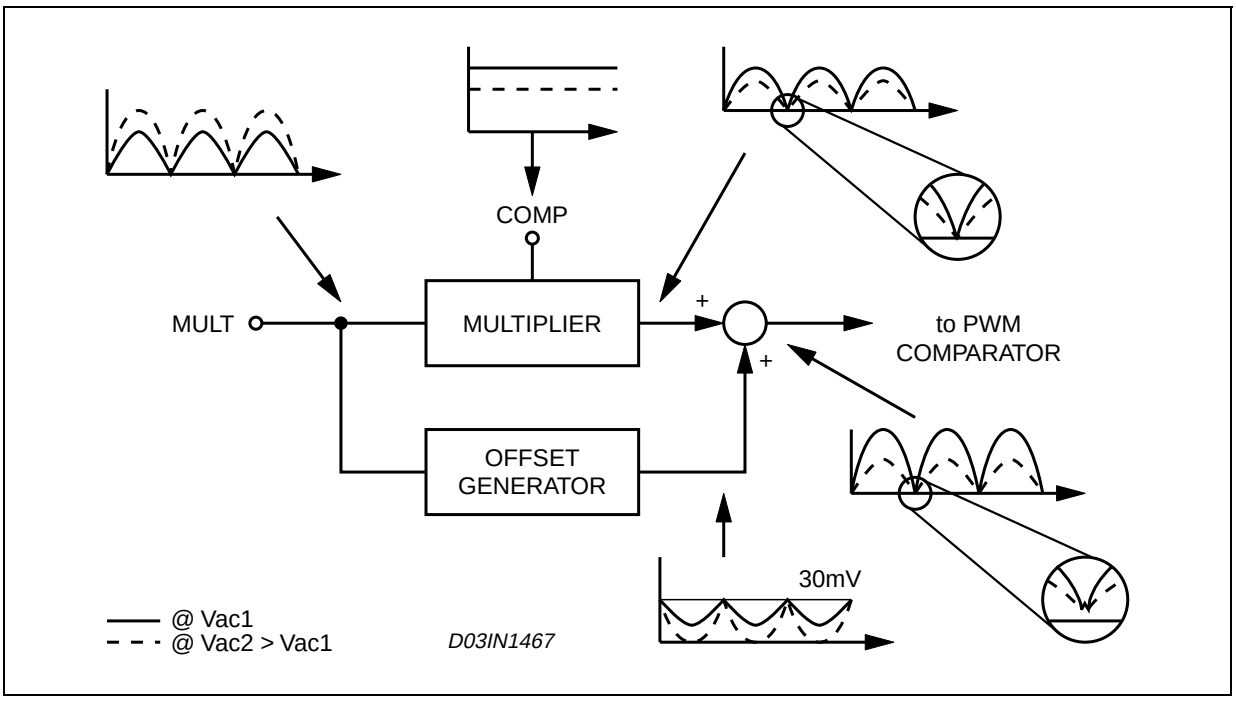


Figure 4. Effect of THD optimizer circuit

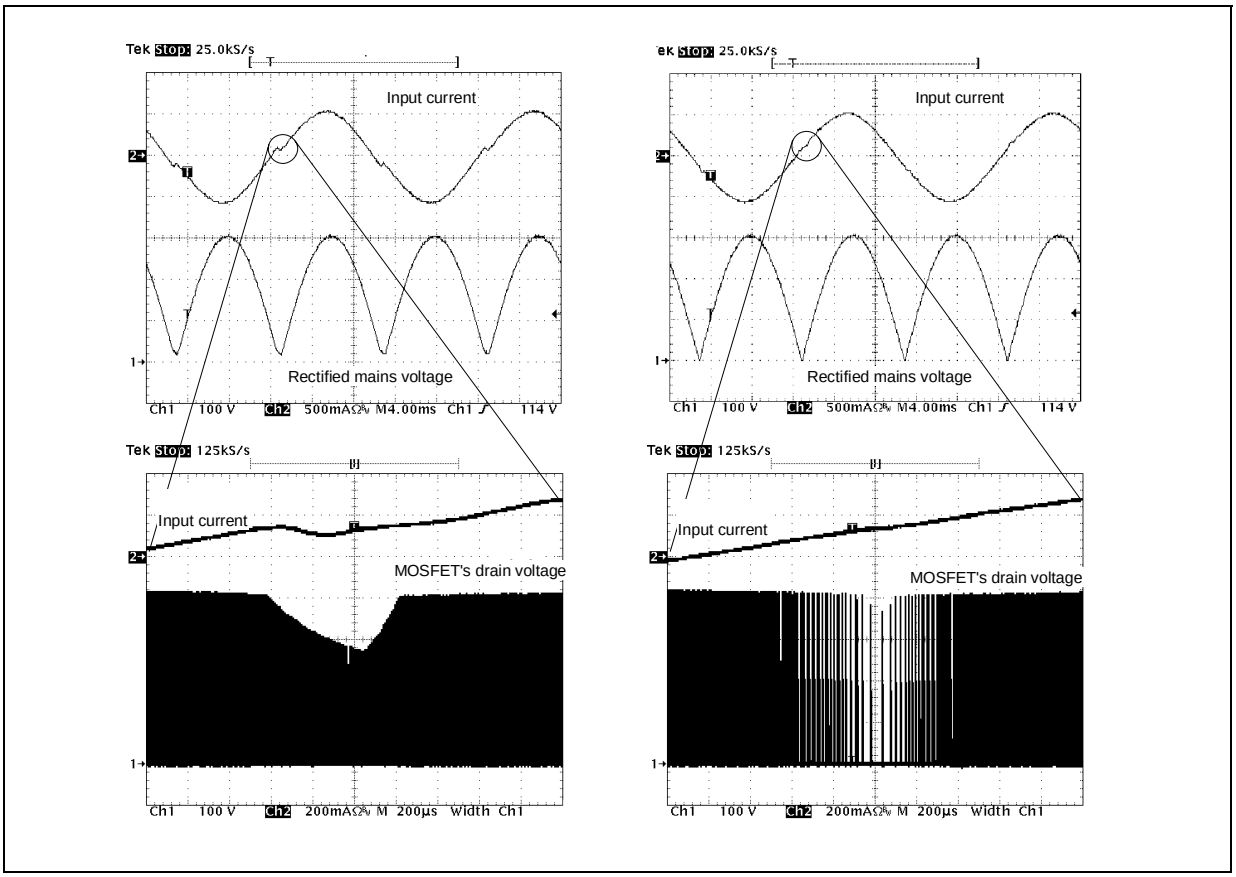
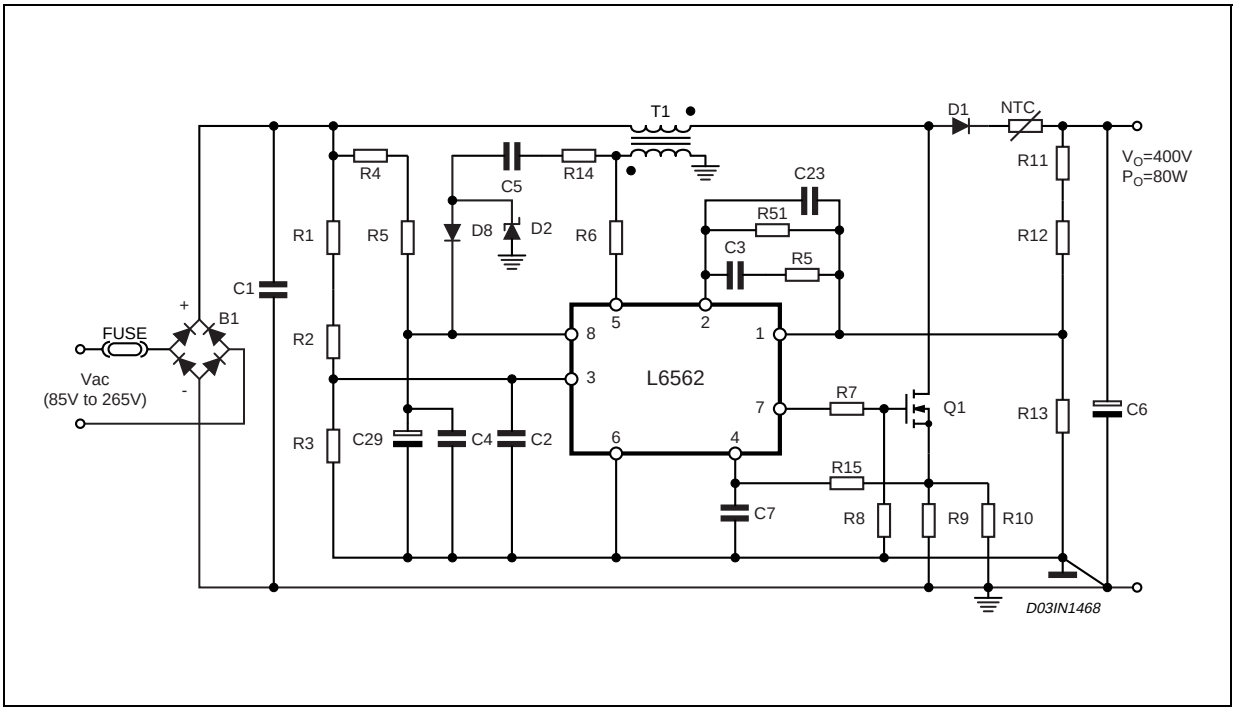


Figure 5. EVAL6562N-80 schematic



PART LIST

R1	750kΩ 1%	R14	100Ω, 5%	C6	47µF, 450V
R2	750kΩ 1%	R15	shorted	C7	N.A.
R3	10kΩ 1%	R50	12kΩ	C23	330nF
R4, R5	180kΩ 5%	R51	N. A.	C29	22µF, 25V
R6	68kΩ 5%	NTC	2.5	D1	STTH1L06
R7	33Ω	C1	0.47µF 400V	D2	1N5248B
R8	47kΩ	C2	10nF	D8	1N4148
R9, R10	0.82Ω, 0.6W	C3	0.68µF	Q1 (TO220)	STP8NM50
R11, R12	750kΩ 1%	C4	100nF	BRIDGE	DF06M
R13	9.53kΩ, 1%	C5	12nF	FUSE	4A/250V

T1: Boost Inductor Spec (ITACOIL E2543/E)

- E25x13x7 core, 3C85 ferrite
- 1.5mm gap for 0.7mH primary inductance
- Primary: 105 turns (20 x 0.1mm)
- Secondary: 11 turns (0.1mm)

Figure 6. EVAL6562N-80: efficiency (left, in %) and Power Factor (right) vs. input voltage

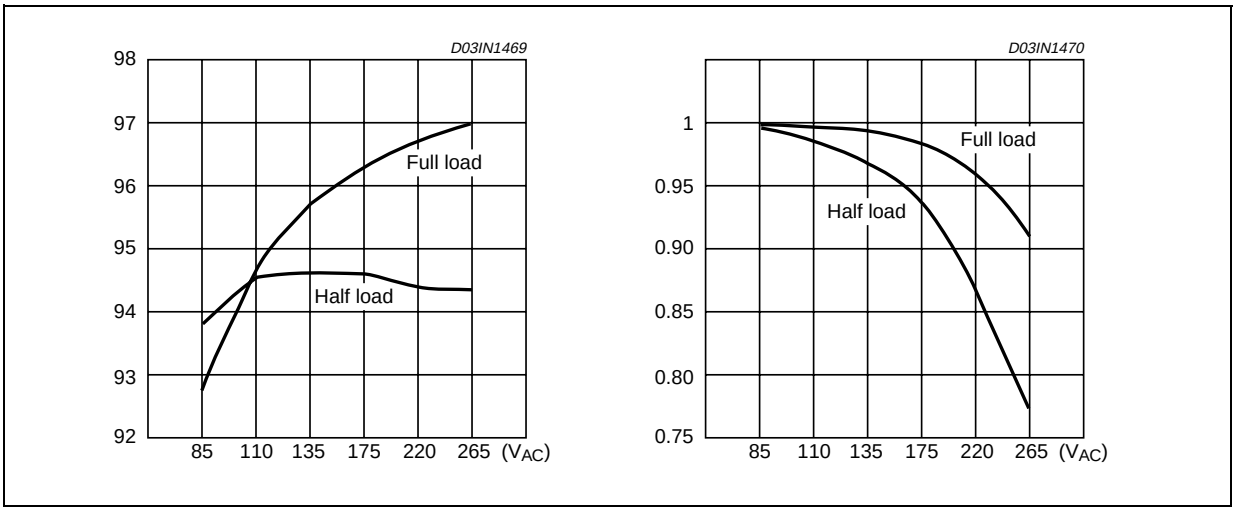
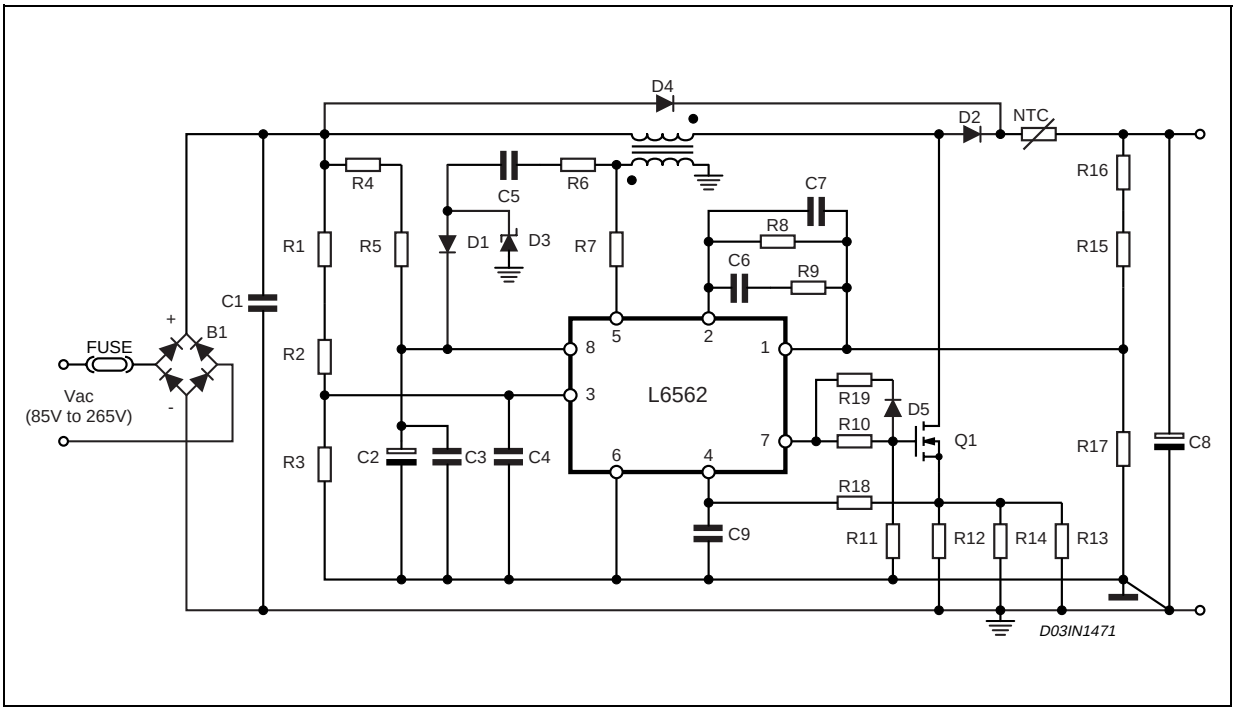


Figure 7. EVAL6562N-250 schematic



PART LIST:

R1, R2	910kΩ 1%	R17	9.53KΩ, 1%	C9	OPEN
R3	13kΩ 1%	R18	SHORT	D1	1N4148
R4, R5	180kΩ 5%	R19	SHORT	D2 (DO-201AD)	STTH3L06
R6	100Ω 5%	C1	1µF, 400V	D3	ZENER 18V
R7	47kΩ 5%	C2	22µF, 25V	D4	1N5406
R8, R11, R14	OPEN	C3	100nF	D5	1N4148
R9	20kΩ	C4, C5	10nF	Q1 (TO220)	STP20NM50
R10	33Ω, 5%	C6	680nF	BRIDGE	STBR606 (ST)
R12, R13	0.33Ω, 1W	C7	220nF	FUSE	4A/250V
R15, R16	750KΩ, 1%	C8	100µF 450V	NTC	2.5

HEATSINKER: Aavid Thermalloy Max Clip S508

T1: Boost Inductor Spec

- ETD34, 3C85 ferrite
- 1.8mm gap for 180 H primary inductance
- Primary: 46 turns (20 x 0.1mm)
- Secondary: 6 turns (0.1mm)

L6562-250W demo board evaluation:

Figure 8. PF vs. Input Voltage

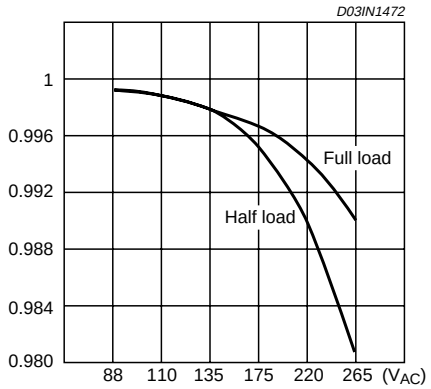


Figure 10. Efficiency (%) vs. Input Voltage

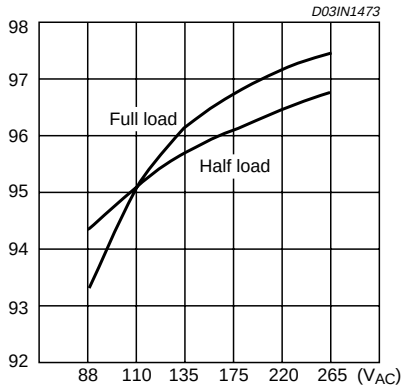
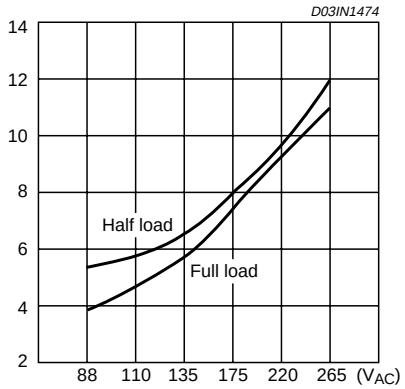


Figure 9. THD vs. Input Voltage



REFERENCES

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AN1059: "DESIGN EQUATIONS OF HIGH - POWER - FACTOR FLYBACK CONVERTERS BASED ON THE L6561"

AN1060: "FLYBACK CONVERTERS WITH THE L6561 PFC CONTROLLER"

AN1089: "CONTROL LOOP MODELING OF L6561 - BASED TM PFC"