CS3842AAN/D

Single CS3842A Provides Control for 500 W/200 kHz Current-Mode Power Supply

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APPLICATION NOTE

INTRODUCTION

With the introduction of the CS3842A PWM IC, current–mode is possible for power supplies of a wide range of output power levels. It's low cost makes the CS3842A particularly attractive in low power DC to DC converter applications. But because this IC can provide a high output current (1.0 A peak, 200 mA average), it is also capable of driving large power MOSFETS which can switch high amounts of power.

Current–Mode vs. Voltage–Mode Control

In a switching power supply, the output voltage is controlled by varying the conduction duty cycle of the power switch(es). Traditionally duty cycle control was done by comparing the amplified difference of the output voltage feedback signal and a fixed stable reference to the sawtooth waveform derived from an oscillator. This constitutes the basic voltage mode control (VMC) scheme.

VMC was later improved by allowing a sample of the input voltage to vary the slope of the sawtooth waveform. This feed forward scheme provided excellent line regulation in most of the popular circuit topologies. However, the task of compensating voltage mode converters has not been simple due to its resonant peak and 40 dB/decade roll off associated with the output LC filter.

In current mode control, (CMC) the control signal represents the peak inductor current and forms a second loop in the circuit (Figure 1). The advantages of current mode control are:

- Instantaneous correction to line voltage variations; the inductor current slope varies with input voltage.
- Stable power supply designs; the pole associated with the inductor is eliminated.
- Equal current sharing in paralleled power stages when both share the same control signal and have the same current sense circuits.
- No current limit amplifier is needed.
- Flux balancing exists in push–pull circuits.

Disadvantages:

- Slope compensation is required for peak versus average inductor current error and for compensating instabilities associated with load disturbances in single ended topologies operating at greater than 50% duty cycle.
  Premature shutdown due to the turn on current spike caused by the reverse diode recovery of the output free wheeling diode.
- Runaway conditions when half bridge topology is operated in current–mode control.

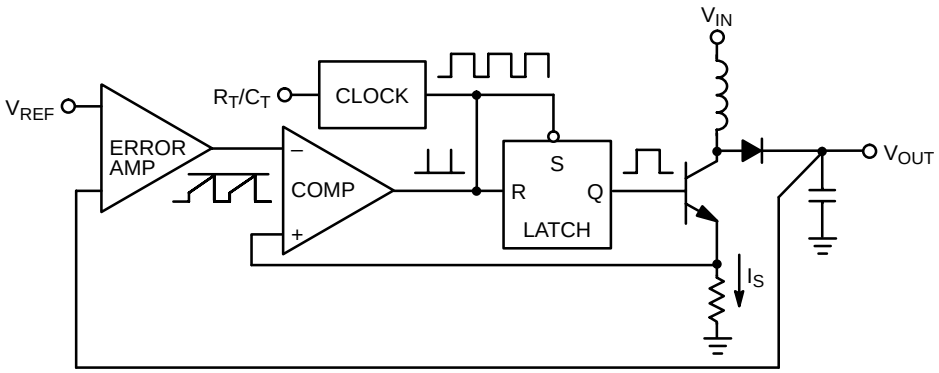
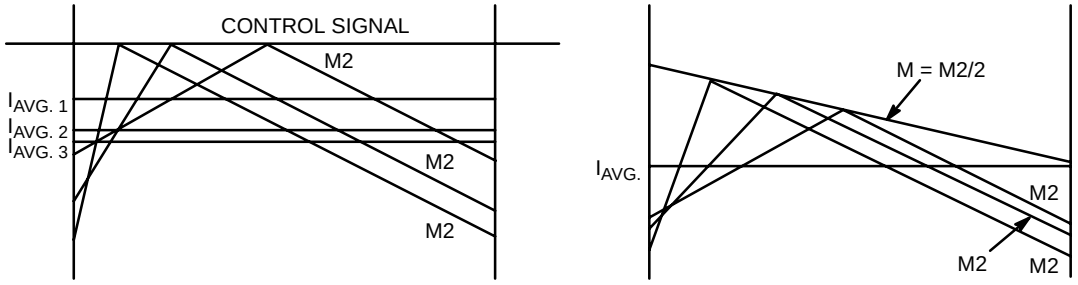


Figure 1. Basic Circuit Using Current–Mode Control



(a) Peak vs. Average Current Error

(b) $I_{AVG.}$ is Constant for Varying Duty Cycle, (Constant Load)

Figure 2. Peak Current Detection is Used to Keep I_{AVG} Constant for Varying Duty Cycles

If the current sense signal is properly filtered, noise induced problems including the turn on spike can be avoided. By deliberately adding more slope to the current sense signal, or subtracting it from the control voltage signal, the instability due to greater than 50% duty cycle operation can be overcome. Slope compensation aids in reducing uncertainty at the point of trigger in the PWM comparator when shallow current ramps are involved. It also helps the peak current appear higher than the turn–on spike. This eliminates premature shutdown.

Figure 2a illustrates how peak current detection in current mode control produces a change in the average current by relying on the feed forward property of current mode to compensate for line voltage variations. If a slope equal to one–half the negative going inductor current slope is added to the current sense signal, or subtracted from the control signal, this error is corrected (Figure 2b).

Current–Mode Control With the CS3842A

Figure 3 shows a CS3842A block diagram containing the basic functions necessary to implement current–mode control. This device will operate from 10 V to 30 V from a low impedance voltage source or can be current fed if the current is limited to less than 30 mA. The CS3842A is designed to be driven from the rectified line voltage for start–up, requiring a current of only 0.5 mA(typ). An auxiliary supply voltage is needed when the device is used as in Figure 4. When operating with a supply voltage between 10 V and 16 V, a bootstrap circuit provides more than 16 V to overcome the device's under–voltage lockout circuit turn–ON threshold. The wide hysteresis band (6.0 V) accommodates variations in the input voltage.

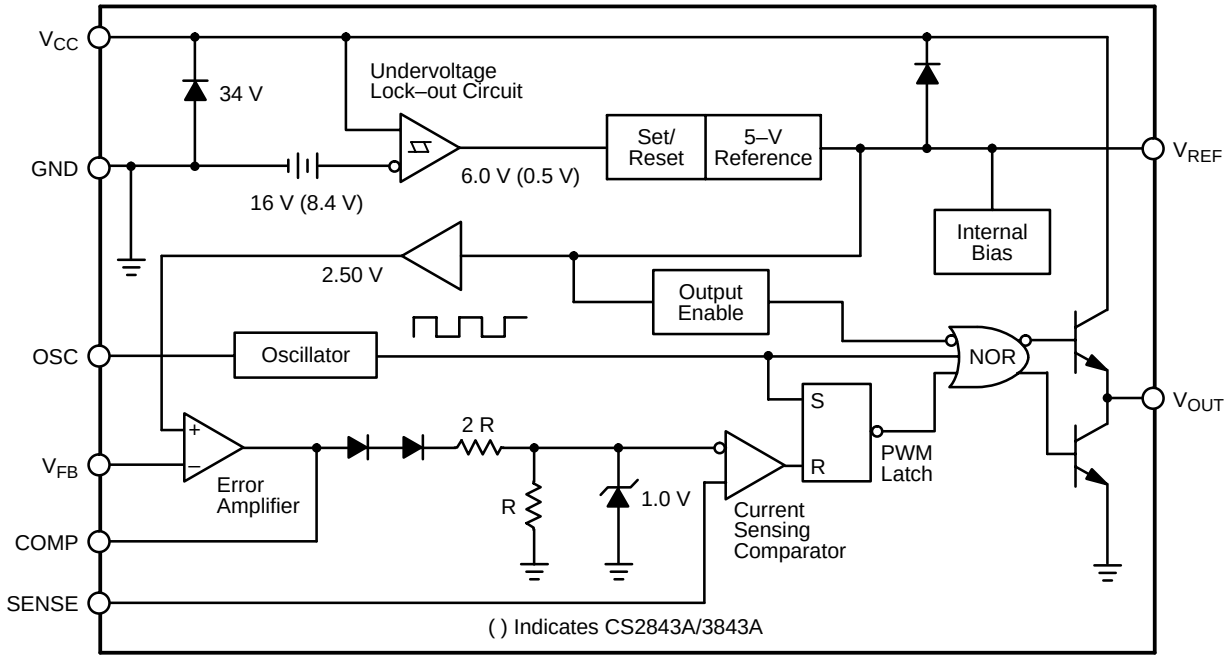


Figure 3. CS3842A/3843A Block Diagram

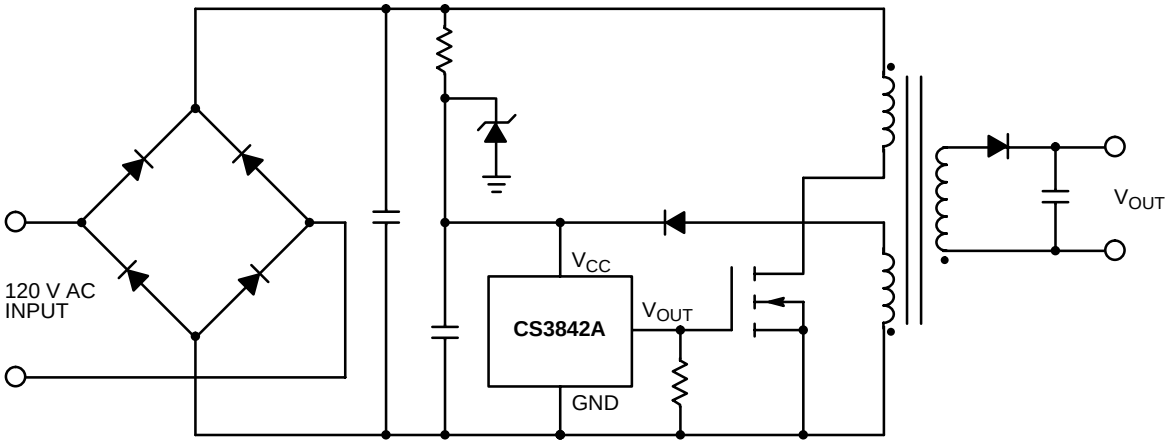


Figure 4. Common Off–Line Operation of CS3842A

The Oscillator Section

After V_{REF} is stabilized, the timing capacitor, C_T charges through R_T to about 2.7 V, and then discharges to about 1.1 V for every cycle of the oscillator. Since C_T must begin charging from 0 volts instead of 1.1 V on the first cycle, the ON time is longer than in subsequent cycles.

To avoid this ON time discrepancy the CS3842A latches the output in its low state until the end of the first cycle (Figure 5). The internal current source which discharges C_T is trimmed to provide an accurate maximum duty cycle clamp without relying on external timers to synchronize the oscillator. The timing components can be selected, to set the frequency of the oscillator, and the maximum duty cycle.

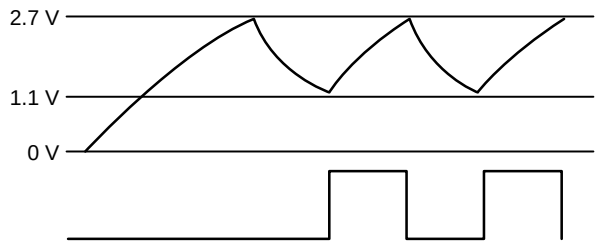


Figure 5. The First Pulse is Blanked Out Because it Exceeds the Maximum Duty Cycle Clamp

Typical waveforms illustrating CS3842A operation are shown in Figure 6. During the discharge time of the OSC waveform, the oscillator internally disables the output to limit the maximum duty cycle. When V_{IN} increases, the slope of the switch current (the combination of the inductor current slope referred to the primary, the transformer magnetizing current, and any slope compensation) increases such to provide instant duty cycle correction without using the error amplifier's dynamic range. If a step increase in load current occurs, the error amplifier shifts the control line to a higher level to allow the inductor to conduct more current. Since the rate of change of the current on the inductor is fixed by the voltage applied, (if the peak current does not intersect the control line) the duty cycle clamp will time out first and prevent the conduction time from exceeding the maximum ON time. Since the output voltage drops due to the load increase, the down–slope of the inductor current decreases, allowing the current pulse to quickly converge to a steady state value.

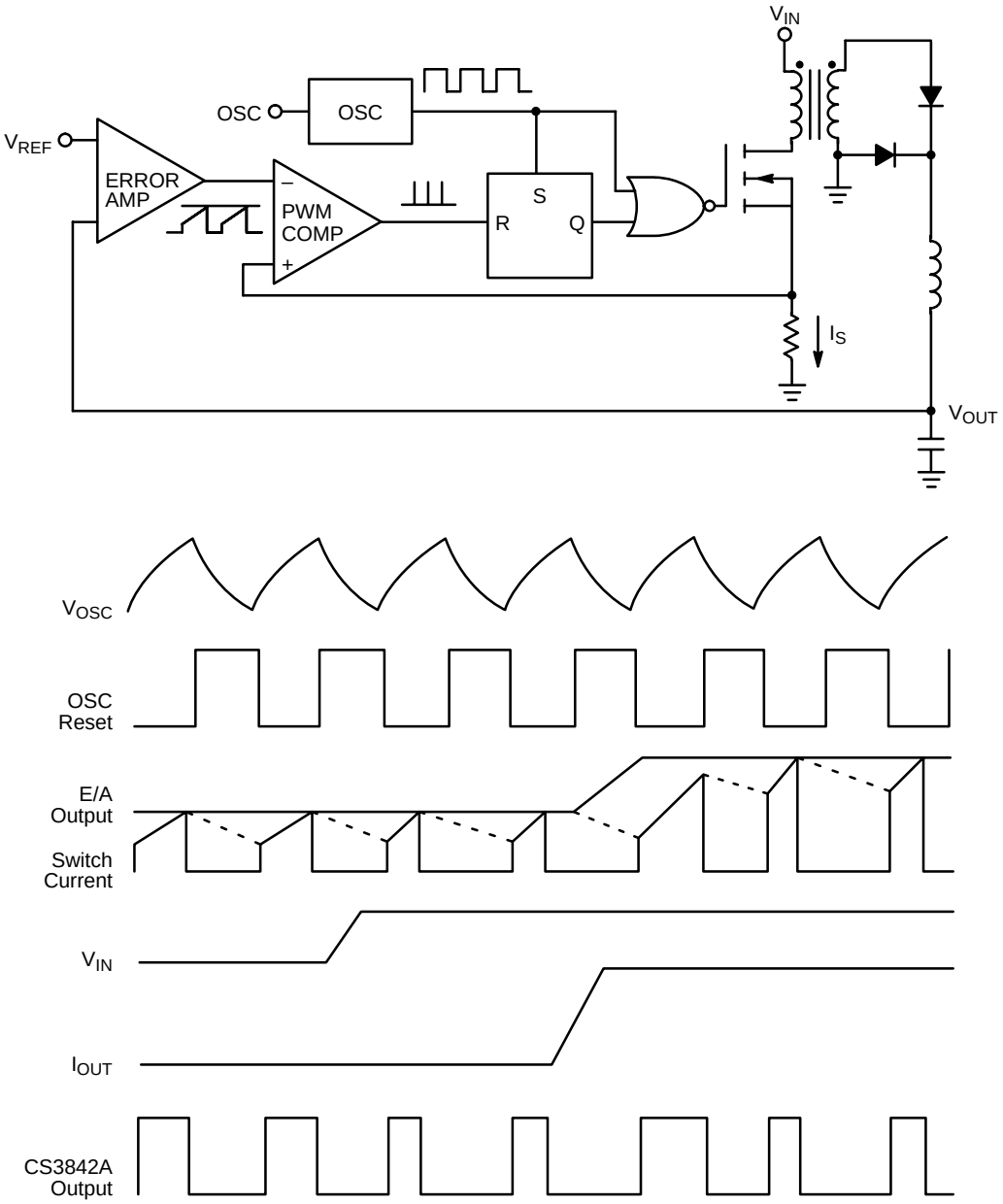


Figure 6. CS3842A Typical Waveforms

Applying the CS3842A

A 500 W, 200 kHz power supply was designed by combining the high frequency operation of the oscillator with the high current drive capability of the CS3842A. A two transistor forward converter was chosen. The advantages of this topology are:

- the voltage rating for the MOSFETs is reduced to one–half that of a single transistor forward converter (450 V compared to 900 V);
- snubber networks are required only for load line shaping of the MOSFETs;
- the energy stored in the leakage inductance is effectively returned to the input via clamp diodes;
- the ripple current rating on the output filter capacitor is less than in flyback converters.

One notable disadvantage of this topology is the limit on the maximum duty cycle which results in less efficient transformer utilization. The complete schematic of the power supply is shown in Figure 7.

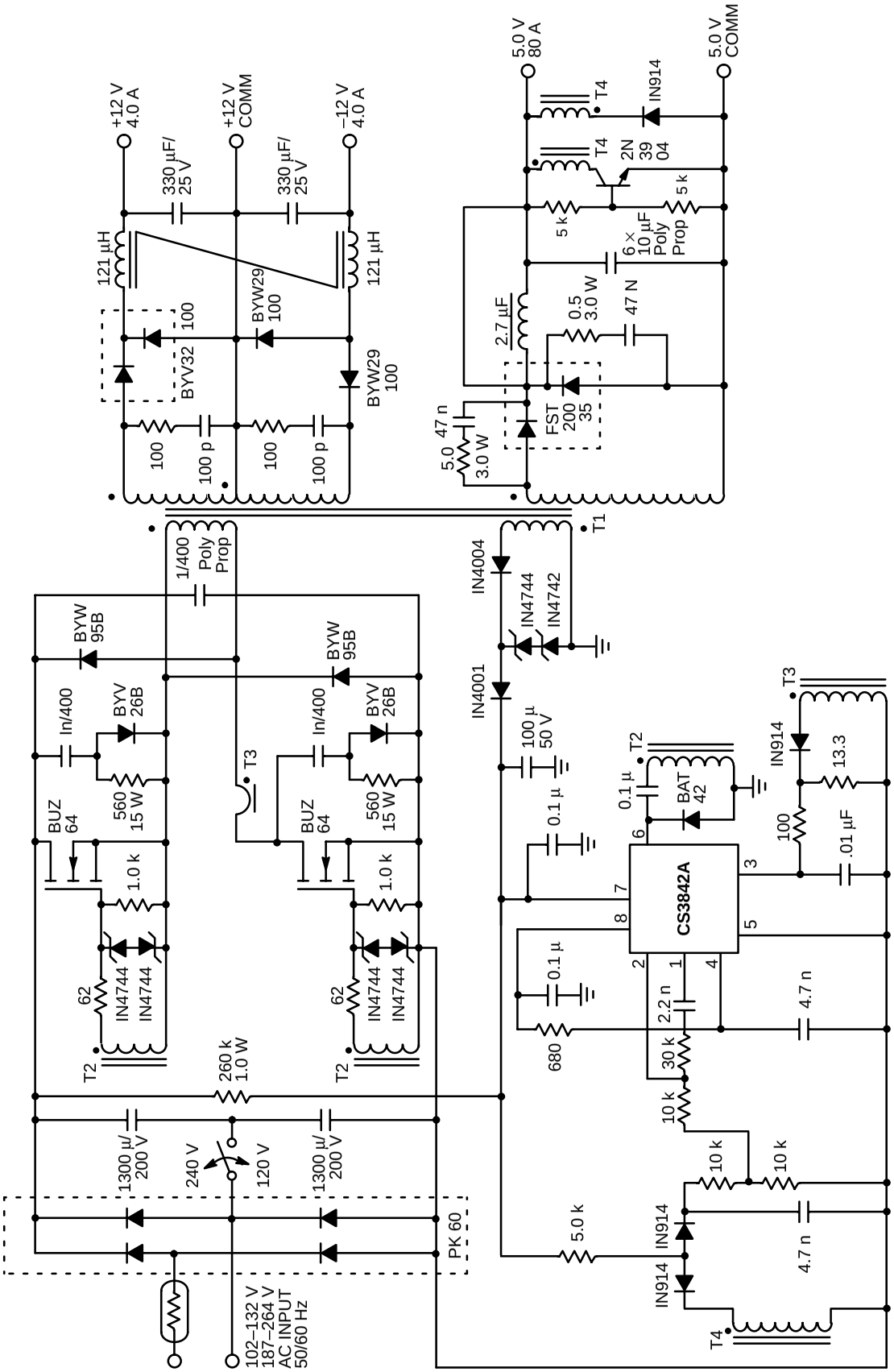


Figure 7. Schematic of 500 W, 200 kHz Power Supply

Input Section

To determine the required capacitance, the input power should be approximately known and this can be done by making an estimate of the power losses expected in the circuit.

Expected Losses

Schottky Diodes: (80 A)(.55 V) . . . . . 44 W
Power MOSFETs: Assume 5% of P_{OUT} . . . . . 25 W
Diodes on a 12 V Output. (two diodes conduct at any one time: (0.8 V)(4.0 A)(2) . . . . . 6.0 W
Power Transformer: . . . . . 20 W
Inductors: (Estimate) . . . . . 10 W
Snubbers, Control Ckt, etc: . . . . . 20 W
Total Estimated Losses . . . . . 125 W
Expected Input Power . . . . . 625 W

Since the AC input voltage is rectified, the capacitors must deliver energy at twice the line frequency.

$$E_{IN} = \frac{P_{IN}}{2f} = \frac{625}{(2)(60)} = 5.21 \text{ JOULES} \quad (1)$$

The minimum peak voltage expected is

$$187 \times \sqrt{2} - 2 + 262 \text{ V}$$

The 2.0 V accounts for 2 diode drops on the input bridge. If we assume initially the capacitor valley voltage to be 200 V then from

$$E_{IN} = \frac{1}{2} C_{eq}(V_{pk}^2 - V_{min}^2) \quad (2)$$

$$C_{eq} = 364 \ \mu F$$

or C = 728 μF because the two capacitors are in series.

Anticipating tolerances and going through some iterations to find a commercially available capacitor that would meet the ripple current requirements, two Sprague 1300 μf/200 V 36DX series capacitors were selected.

The valley voltage is recalculated using Eqn. (2) and found to be 229 V. The capacitor conduction time is then determined.

$$t_c = \frac{\cos^{-1}(V_{min}/V_{pk})}{2\pi f} = 1.35 \text{ ms} \quad (3)$$

The instantaneous maximum capacitor charging current is

$$I_{chg} = C_{eq}(V_{pk} - V_{min})/t_c = 15.9 \text{ A} = I_{pk} \quad (4)$$

Assuming a rectangular shaped charging current pulse, the RMS value is:

$$I_{chg} = I_{pk}\sqrt{2ft_c} = 6.4 \text{ A} \quad (5)$$

The DC current is

$$I_{dc} = I_{pk}(2ft_c) = 2.58 \text{ A} \quad (6)$$

Since the DC component of the current is zero in the capacitors, the RMS value of the charging current becomes

$$I_{rms} = \sqrt{I_{chg}^2 - I_{dc}^2} = 5.86 \text{ A} \quad (7)$$

The discharge current is determined as follows

$$I_{dis} = I_{in}\left(\frac{T}{2} - t_c\right)\frac{2}{T} = \frac{P_{IN}}{V_{pk}}\left(\frac{T}{2} - t_c\right)\frac{2}{T} = \frac{P_{IN}}{V_{pk}}\left(\frac{1}{2f} - t_c\right)2f = \frac{P_{IN}}{V_{pk}}(1 - 2t_c f) \quad (8)$$

Substituting in to equation 8, we get I_{dis} = 2.0 A. The total RMS capacitor current is

$$I_{rms_{tot}} = \sqrt{I_{rms}^2 + I_{dis}^2} = 6.19 \text{ A}$$

The manufacturer's maximum RMS current specified at 85°C and 120 Hz is 3.15 A. At less than 55°C, this value is multiplied by a factor of 2 or 6.30 A. This is still acceptable in most commercial applications. Higher valued capacitance reduces the charging capacitor duty cycle, increases the RMS current in the capacitors, and increases the peak charging current, which puts severe stress on the input rectifiers.

Repeating the above calculations for 50 Hz input frequency, the RMS current comes out to be 5.92 A, still within the capacitor's specifications.

The input bridge rectifier must be chosen to handle the peak capacitor charging current and the DC current into the power supply. Surge current limiting during start–up should also be provided.

Power Transformer Design

Operating at 200 kHz, the criteria for core selection is a complicated process, and beyond the scope of this paper. Core losses and winding losses due to AC resistance increase with increasing frequency and contribute to a higher temperature rise in the transformer. The core chosen is a Magnetics Inc. PQ4040, P material. The turns ratio is:

$$n = \frac{(V_{IN(min)} - 2V_T)D_{max}}{V_{OUT} + V_L + V_f} \quad (10)$$

where:

$V_{IN(min)}$ = the minimum dc voltage above which the power supply regulates,

V_T = the drain to source ON voltage across a MOSFET at full load,

D_{max} = the maximum duty cycle,

V_{OUT} = the output voltage,

V_L = dc resistance voltage drop in the filter choke at full load, and

V_f = forward drop across the Schottky diode at full load.

$$n = \frac{(200 - 6)(0.45)}{5 + 0.2 + 0.6} = 15$$

Note that $V_{IN(min)}$ is lower than the input capacitor valley voltage in order to provide some hold–up time.

The saturation flux density for P material at high temperature is a little above 3000 Gauss. To prevent core saturation due to a sudden load step increase at high line, and to keep the core losses down, a safe value of 1500 Gauss is used. The minimum primary turns for a forward converter limited by 50% duty cycle is given by:

$$Np \geq \frac{V_{IN(min)} \times 10^8}{2\Delta B_{max} A_e f_s} \quad (11)$$

where:

A_e = effective core area (cm^2)

f_s = switching frequency, or

$$Np > \frac{200 \times 10^8}{2(1500)(2.01)(2 \times 10^5)} = 17\ T$$

To obtain the right voltages for the number of turns and to fit the wire effectively in the bobbin, the primary uses 30 turns composed of six #24 AWG wires in parallel. Using 5 wires in parallel as opposed to a single larger wire reduces the AC resistance in the wires caused by the skin effect. To minimize the primary leakage inductance, a split primary is used to completely surround the main secondary. A four turn auxiliary winding of #30 AWG is wound on top of the primary, separated by tape, to provide good coupling with the primary. This is again repeated in the second primary half and the two paralleled auxiliary windings.

The secondary consists of two turns of two 16–mil copper foil strips 0.9” wide. The ±12 V secondary is a split 10 turn winding consisting of two #19 AWG wires. Shields were also placed between the primary and the main secondary to return any noise coupled by parasitic capacitance in the windings. The transformer was designed to provide adequate line isolation. A summary of the transformer data is:

Winding	Turns
Primary	30
5.0 V secondary	2
+12 V secondary	5 each
Auxiliary	4

The auxiliary winding provides power to the CS3842A when the IC is in operation. The two zener diodes on the auxiliary supply circuit clamp the voltage on the reset cycle to a maximum of 27.8 V, or 208.5 V on the primary side.

To determine the power available in the auxiliary winding, the magnetizing current is calculated. For the PQ–4040, P material, the inductance factor, AL, given is 5020 mH/1000 turns. The primary inductance is 5020(30/1000)2 = 4.5 mH. The magnetizing current is then

$$I_{mag} = \frac{V_{min} D_{max}}{L_p f_s} = \frac{(200)(.45)}{(4.5 \times 10^{-3})(2 \times 10^5)} = 100\ mA \quad (12)$$

In the auxiliary winding, the current is scaled proportionally to the turns ratio, therefore

$$I_{aux} = (7.5)(100\ mA) = 750\ mA$$

Averaging this current over one cycle gives a current of

$$I_{aux}(1 - D_{.x})/2 = 200\ mA$$

If the reset voltage is 27.8 V during $(1 – D_{max})$, the power available is about 3.15 W.

If the control circuit needs more power than the auxiliary winding can provide, the reset voltage will start to drop. To correct this problem, a small gap may be placed in the transformer core. If the energy is more than required by the control circuitry, a bleeder resistor should be added to protect the zener diodes from excessive power dissipation.

Output Filter Design

During t_{OFF}, a voltage equation around the loop indicated by the current direction in Figure 8 is:

$$V_L = V_{OUT} + V_F = \frac{L\Delta I_L}{t_{OFF}} \quad (13)$$

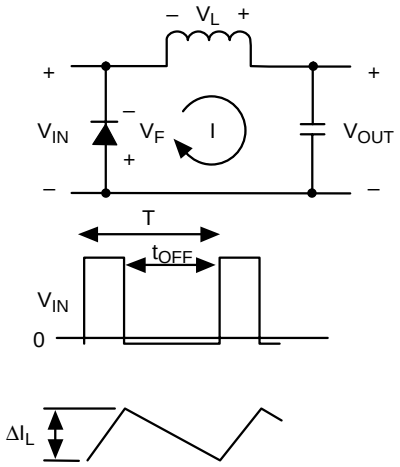


Figure 8. The Output Filter Circuit

The maximum OFF time is determined during the minimum duty cycle.

$$D_{min} = \frac{V_{IN(min)}D_{max}}{V_{IN(max)}} = \frac{194\ V(0.45)}{370\ V} = 0.23 \quad (14)$$

$$t_{OFF} = (1 - D_{min})T_S = 3.85\ \mu s \quad (15)$$

If we select the inductor ripple current, ΔI_L = 8.0 A, then the value of inductance required is, from equation (13).

$$L = \frac{V_L T_{OFF(max)}}{\Delta I_L} = \frac{(5.6)(3.8 \times 10^6)}{8} = 2.7\ \mu H \quad (16)$$

The maximum DC current through the inductor is 80 A. We determine the LI^2 product requirement.

$$LI^2 = (2.7 \times 10^{-6})(80)^2 = 17.3\ mJ \quad (17)$$

This value is used in selecting the core size. The core selected here is a Ferroxcube EC–52–3C8. EC cores are very popular because they provide adequate space for large wire sizes required for low voltage and high current applications. Because the windings are not totally enclosed by the core better cooling is possible.

The required inductance factor can be calculated from

$$A_L = \frac{(BA_e)^2 \times 10^{-4}}{LI^2} \quad (18)$$

For a flux density of 1500 Gauss:

$$A_L = \frac{[(1500)(1.8)]^2 \times 10^{-4}}{17.3} = 42\ mH/1000\ Turns$$

The ampere–turns required is

$$NI = \frac{10BA_e}{A_L} = \frac{10(1500)(1.8)}{42} = 643\ At \quad (19)$$

dividing by the current the number of turns required is

$$N = 643/80 = 8\ T$$

The gap required is

$$l_g = \frac{0.4\pi N^2 A_e(10^{-8})}{L} = \frac{0.4\pi(8)^2(1.8)(10^{-8})}{2.7 \times 10^{-6}} = 0.536\ cm\ or\ 0.211\ in \quad (20)$$

The core can be gapped by grinding the center post. You can select a gapped core like the EC52G–3C8(2X) which has a 180 mil gap and grind it to size. Another method is to add spacers between the outer posts of the core. The following relation can be used to convert the required center post gap, l_g, to the length of an equivalent gap using spacers, l'_g

$$l'_g = 0.3643 l_g \quad (21)$$

Substituting the required value of l_g we obtain l'_g = 77 mils.

In order to be able to carry the full load current, two strips of 16 mil by 1 inch copper foil was used.

Filter capacitance is calculated as,

$$C = \frac{\Delta I_L}{8 f_S \Delta V_{pp}} \quad (22)$$

where V_{pp} is the peak–to–peak output voltage ripple desired. For this application, 80 mV was chosen. Therefore

$$C = \frac{8}{8(2 \times 10^5)(0.08)} = 62.5\ \mu F$$

The ESR required is:

$$R_{ESR} = \frac{V_{pp}}{I_L} = \frac{0.08}{8} = 10\ m\Omega \quad (23)$$

Six 10 μF polypropylene capacitors are used yielding a combined ESR of 1.5 mΩ.

Current Sense Calculation

The peak current on the primary is the sum of the peak inductor currents of the secondaries referred to the primary by their turns ratios plus the magnetizing current or

$$I_{pri(pk)} = \frac{84}{15} + 2\left(\frac{4.5}{6}\right) + 0.1 = 7.2\ A \cong 7.5\ A$$

Because this current would require a 5 watt current sensing resistor to develop a 1 volt signal amplitude, a current transformer was used with a turns ratio of 100.

$$I_{CS} = 7.5/100 = 75\ mA$$

The required current sense resistor becomes

$$R_{CS} = 1/0.075 = 13.3\ \Omega$$

A low pass filter was used to smooth out high frequency noise coupled to the current sense signal.

Closed Loop Design

The zero associated with the capacitor bank ESR is at

$$f_{ESR} = \frac{1}{2\pi(1.5 \times 10^{-3})(60 \times 10^{-6})} = 1.77 \text{ MHz}$$

The two load resistance extremes in the main output are:

$R_{O(min)} = 5.0 \text{ V}/80 \text{ A} = 0.0625 \ \Omega$
$R_{O(max)} = 5.0 \text{ V}/5.0 \text{ A} = 1.0 \ \Omega$

Note that the voltage feedback loop looks only at the 5.0 V output. The output capacitor bank and the load resistance form a moving pole with corner frequencies at

$$f_{p(max)} = \frac{1}{2\pi R_{O(min)} C} = 42 \text{ kHz} \quad (24)$$

$$f_{p(min)} = \frac{1}{2\pi R_{O(max)} C} = 2.65 \text{ kHz} \quad (25)$$

The output–to–control signal is expressed as

$$\frac{V_O}{V_C} = \frac{I_L}{V_C} R_O H_f(S) = \frac{nn' R_O}{3R_{CS}} \left(\frac{1 + S R_{ESR} C}{1 + S R_O C} \right) \quad (26)$$

where:
n = primary to second turns ratio
n′ = current sense transformer turns ratio.

At maximum load

$$\left. \frac{V_O}{V_C} \right|_{f \rightarrow o} = \frac{15(100)(0.0625)}{3(13.3)} = 2.35, \ 7.42 \text{ dB}$$

At minimum load

$$\left. \frac{V_O}{V_C} \right|_{f \rightarrow o} = \frac{15(100)(1)}{3(13.3)} = 37.6, \ 31.5 \text{ dB}$$

For good overall stability, the unity gain loop crossover should be chosen at a frequency less than one–fourth the switching frequency. Selecting the crossover frequency to be 42 kHz, the error amplifier is required to provide –7.42 dB gain at crossover. The compensation network is shown in Figure 9. By letting the error amplifier gain cross unity at 2.65 kHz, a good overall gain bandwidth product with adequate phase margin is possible. Calculating the corner frequency for the zero, we have.

$$7.42 = -20(\log 2.65 - \log f_z)$$

Solving for f_z we get 6.23 kHz.

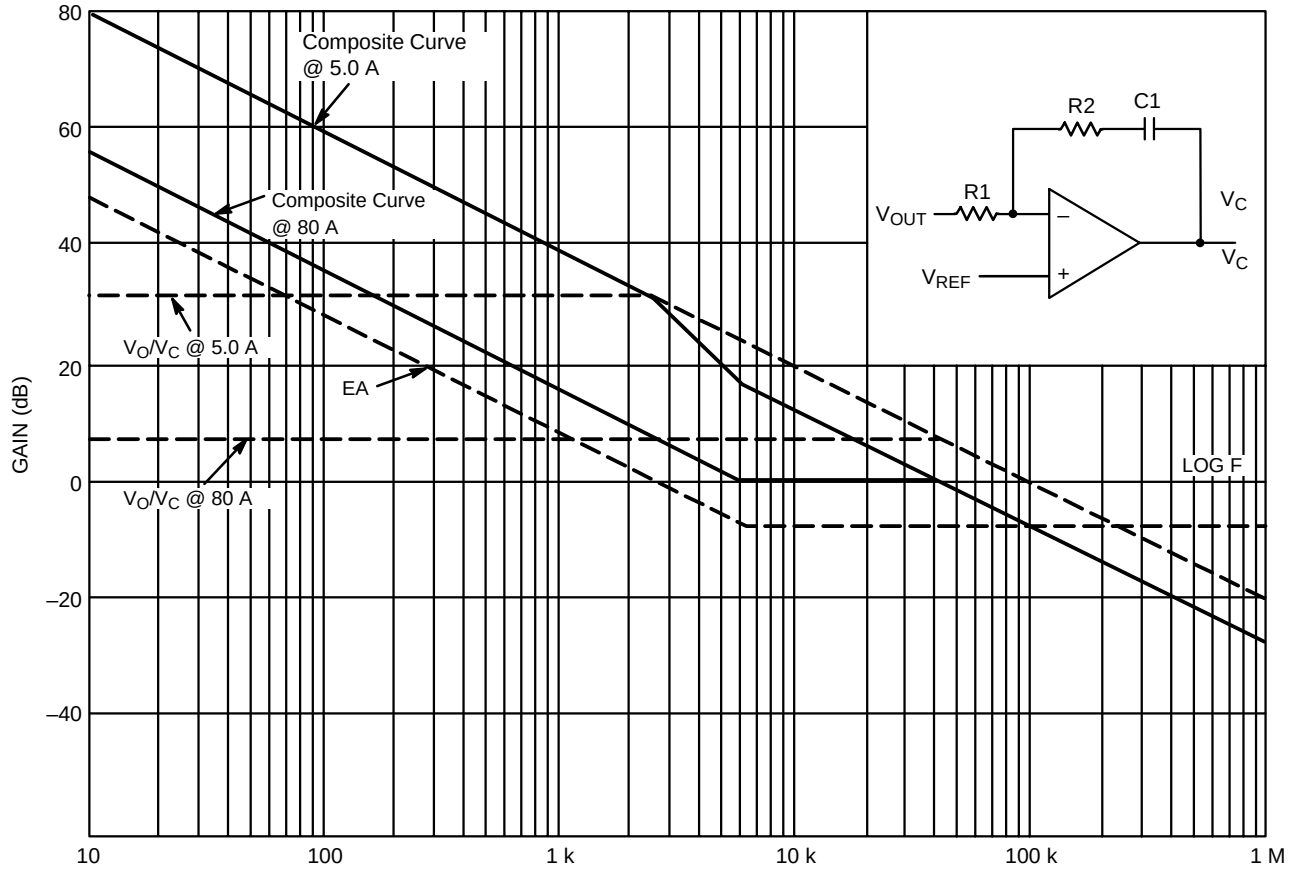


Figure 9. Frequency Response Diagram for Power Supply. Inset E/A Configuration

To provide –7.42 dB, the attenuation ratio should be 0.4256. The error amplifier output is attenuated by a factor of 3 inside the CS3842A. Choosing C_1 to be 2.2 nf and R_1 = 10 kΩ, R_2 becomes 11.6 kΩ. The gain frequency response curves are shown in Figure 9.

To provide isolated output voltage feedback to the error amplifier a small signal transformer, T4, is used. This transformer is switched at 200 kHz by using the power transformer's 5.0 V secondary output to drive a transistor. On the secondary side of T4, one diode is used to rectify the output while another diode is is used to cancel the effect of the first diode.

Other Considerations

When designing high power converters, the combined effect of high power with high frequency requires a very careful layout. All the high di/dt paths must be identified. They must be short, and away from the control circuit.

Bypassing the input DC bus should be done right at the power MOSFETs while low level bypassing should be done at the V_{CC} input of the CS3842A. The feedback signals, especially the one from the voltage feedback, go to the high impedance input of the error amplifier and can not be bypassed without affecting the amplifier's dynamic performance. The use of a separate low level ground is recommended.

When using the CS3842A to drive inductive loads, as in the case of transformer coupled drive circuits, there is a tendency to drive the output pin below ground, thus interfering with the IC's operation. To correct this problem, a low power Schottky diode should be connected from pins 5 to 6 to clamp the output. When the oscillator is used as a maximum duty cycle clamp, the noise on the R_T/C_T should be minimized.

Slope compensation is not required in this application because the duty cycle is < 50% and the filter on current sense signal prevents the turn on spike from prematurely tripping the PWM comparator. To operate efficiently at light loads and reduce the ripple current on the output capacitors, the inductor current ripple is made small. Shallow inductor current ramps also reduce the peak to average inductor error to a negligible amount.

Figures 10, 11, and 12 show some characteristic waveforms of this power supply.

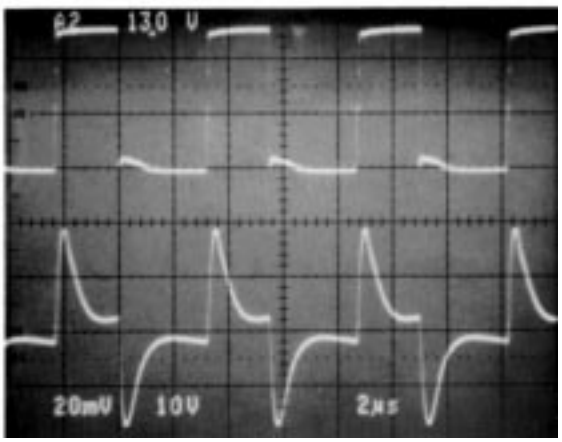


Figure 10. CS3842A Output Voltage and Current (200 mA/div)

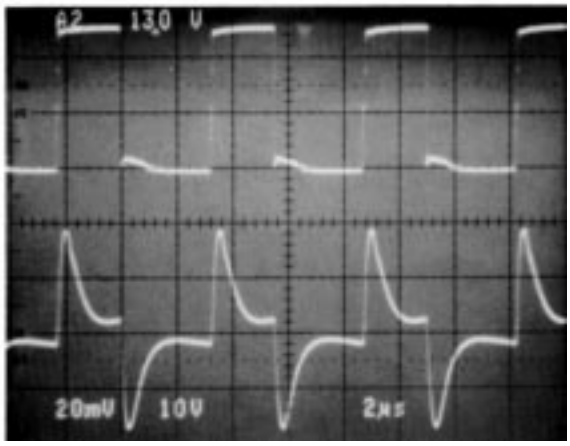


Figure 11. V_{DS}(Top), I_D(Bot.) (0.5 A/div) Low Load

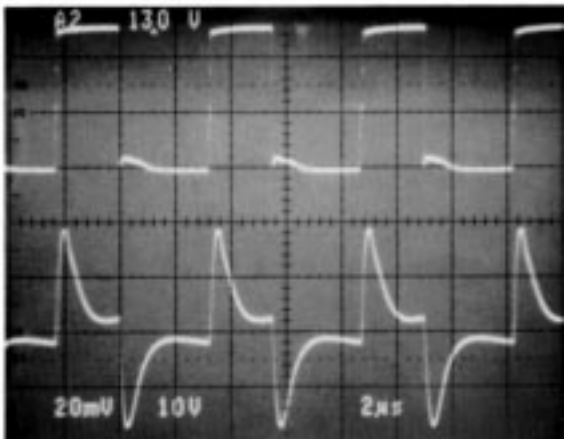


Figure 12. V_{DS}(Top), I_D(Bot.) (2.0 A/div) High Load

Magnetics

T1	Core:	Magnetics Inc. P–44040–UG
	Pri:	30T 6× #24AWG split around main secondary
	Aux:	4T #30AWG in parallel
	Sec (5.0 V)	2T 2× .016 × .9 Cu. foil
	Sec (+12 V)	10T C.T. 2 × #19
T2	Core:	Ferroxcube 846XT250–3C8
	Pri:	16T #22
	Secondaries:	14T #22
T3	Core:	Ferroxcube 768XT188–3E2A
	Pri:	IT
	Sec:	100T, #32
T4	Core:	Ferroxcube 768XT188–3E2A
	Pri:	8T #27
	Sec:	8T #27
	Ter:	4T #27
L1	Core:	Ferroxcube EC52–3C8
	Winding:	8T 2× .016 × 1 Cu. foil 77 mil gap on all three posts
L2	Core:	Ferroxcube 2616PA250–3B7
	Winding:	22T 5× (2 #27 in parallel)

References

1. B. Holland, “Modeling, Analysis and Compensation of the Current Mode Converter,” Proceedings of Powercon 11, Paper 1–2, 1984
2. C. Deisch, “Simple Switching Control Method Changes Power Converter Into a Current Source,” **PESC ’78 Record** (IEEE Publication 78CH1337–AES), pp 300–306.

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