A New Driving Scheme for Synchronous Rectifiers: Single Winding Self-Driven Synchronous Rectification

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***Abstract*—Single winding self-driven synchronous rectification (SWSDSR) approach is a new driving circuit that overcomes the limitations of the traditional driving schemes, becoming an interesting alternative to supply new electronic loads as microprocessors. Traditional self-driven synchronous rectification (*SDSR*) technique has shown very good performance to improve efficiency and thermal management in low-voltage low-power dc/dc converters, however it can not be extended to the new fast dynamic, very low voltage applications.**

***SWSDSR* scheme is based on an additional winding in the power transformer (auxiliary winding). It allows for maintaining the synchronous rectifiers (SRs) on even when the voltage in the transformer is zero, which is impossible to do in traditional self-driven approaches. It also makes possible to drive properly the SRs even in very low voltage applications, 1.5 V or less.**

Coupling of the windings strongly affects the performance of the *SWSDSR* technique. The influence of the coupling between the different windings is analyzed through simulations of different transformers designed for the same application. Models of transformers are generated with a finite element analysis (FEA) tool. Goodness of the SWSDSR scheme is validated through experimental results.

***Index Terms*—DC–DC converters, high efficiency, low voltage.**

I. Introduction

NEW ELECTRONIC loads demands very low supply voltages (3.3 V, 1.5 V, 1.2 V, etc.) as well as very fast power converters capable of regulating properly the supply voltage during load steps [1]. Low supply voltage means low efficiency of the power supply due to the semiconductors voltage drops. Synchronous Rectification is necessary to achieve high efficiency in these low output voltage applications [2].

When the load steps are very aggressive, Interleaving of several synchronous Buck converters [3] is probably one of the best options to supply these new loads. In fact, 4-interleaved synchronous Buck is becoming widely used to supply the new microprocessors. Main drawbacks of synchronous Buck derived solutions are related with the high currents needed at the input since input voltage is low, which mainly affects the size of the input filter and the efficiency of the whole power system.

Topologies with transformer are another alternative to supply low voltage loads. Although the dynamic response achievable with these topologies can be no so good as the reached by the interleaved synchronous Buck, they are also an interesting solution since input voltage is higher.

When topologies with transformer are used in these applications, one of the more important issues is how to drive the synchronous rectifiers (SRs). This paper presents a new self-driven synchronous rectification (SDSR) scheme very interesting for the new low voltage, fast dynamic specifications, it is the single winding self-driven synchronous rectification (SWSDSR) approach.

Traditional SDSR scheme has been successfully used in 3.3 V output voltage applications [4]–[9] where the transformer is unsymmetrically driven. However, it is not recommended in topologies where the transformer is symmetrically driven (Fig. 1) because transformer voltage presents dead times and SRs are off during these times, flowing the output current through the body or external diodes.

On the other hand, the new dynamic response specifications lead to use topologies that drive symmetrically the transformer [10] and [11] as Half Bridge, Push Pull, etc. The dynamic response of topologies that drive unsymmetrically the transformer is worst since there is a risk of saturating the transformer during the load steps. Thanks to the proposed SWSDSR approach, SRs can be properly driven in those topologies with a better dynamic response (half bridge, push pull). This new scheme is based on an additional winding of the power transformer and keeps both SRs on even when the voltage in the transformer is zero.

This new scheme is very promising for low output voltage applications but its performance is highly dependent on coupling among all the windings (primary secondary and auxiliary). Influence of the main parameters is analyzed theoretically and through simulations. Different transformers with different interleaved structures are designed and compared in a half bridge converter with SWSDSR. Transformers are modeled using a finite element analysis (FEA) tool [12], [13] and the whole power stage is simulated to study the influence of the windings coupling on the performance of this topology. Simulation results are compared and validated with experimental results. Two prototypes have been tested to validate the applicability of this new driving scheme.

II. Traditional Driving Approach

Traditional self-driven synchronous rectification scheme has been widely used in 5 V and 3.3 V output voltage applications

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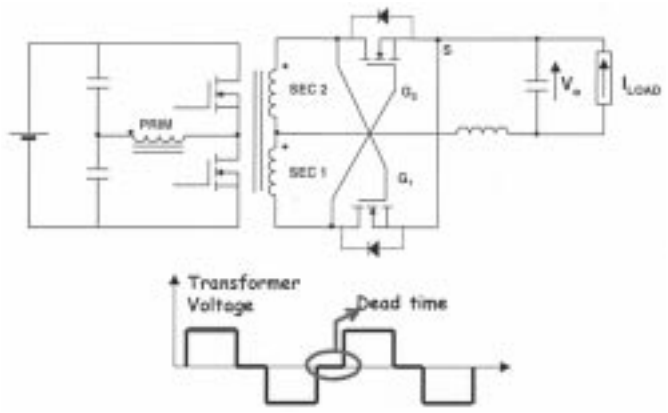

Fig. 1. Half bridge topology with self-driven synchronous rectification and corresponding transformer voltage.

with forward [5]–[8] and half bridge with complementary control [9] topologies. Fig. 1 shows the half bridge topology with the traditional *SDSR* scheme; the power transformer drives the *SRs* by means of the secondary winding. However, when output voltage is lower (1.5 V, 1 V, ...), auxiliary windings are necessary to drive efficiently the SRs since the secondary winding would drive the SRs with a very low voltage. The traditional SDSR scheme with auxiliary windings presents two disadvantages:

- both auxiliary windings have to be very well coupled with the secondary winding, complicating the design of the transformer;
- gate-source voltage (V_{GS}) is negative when the device is off, increasing the driving losses.

The main drawback of the traditional SDSR scheme, with or without auxiliary windings, is that SRs are off when transformer voltage is zero (Fig. 1), flowing the output current through the body diodes. Therefore, the traditional SDSR schemes are more appropriate in topologies with fast transitions in the transformer voltage (from negative to positive and viceversa). Traditional SDSR schemes are highly efficient in topologies as forward with active clamp, half bridge with complementary control, etc. but not in other topologies where the transformer voltage presents dead times (half bridge, push pull, etc.).

III. Single Winding Self-Driven Synchronous Rectification Approach

The *Single Winding Self-Driven Synchronous Rectification* scheme, shown in Fig. 2, consists on an additional winding of the transformer connected to the gates of both SRs and one diode paralleled between the gate and the source of each SRs. The whole voltage of the auxiliary winding is applied to the gate-source of the SRs that is conducting while the gate-source voltage of the SR that should be off is clamped to -0.6 V by the corresponding diode. Therefore, gate-source voltage is roughly zero when the SR is off.

When a transition in the transformer voltage occurs, the same current flows through both parasitic capacitances of the SRs, charging one while discharges the other. Thanks to this fact, SWSDSR scheme presents two important advantages:

- Theoretically, all the energy stored in one capacitance is transferred to the other, reducing the driving losses.
- Moreover, and probably most important, if there are dead times in the voltage waveform of the power transformer, both SRs conduct during these times (Fig. 2). This is again because any discharge of one MOSFET means a charge of the other, being both gate capacitances charge at the same voltage while the transformer voltage is zero. Although the gate voltage during this time is half of the maximum voltage, the new low on-resistance MOSFETs are fully on at both levels.

This new self-driven scheme works properly only if the transformer voltage is symmetrical because energy handled by each parasitic capacitance has to be the same. Hence, this new scheme is applicable to any topology that drives symmetrically the transformer (push–pull, half bridge, etc.) even for a wide input voltage range. It is also applicable to forward with active clamp and half bridge with complementary control only if the duty cycle is 50%.

Performance of this circuit is highly dependent on the coupling among the windings. When one SR is off, the diode between gate and source must clamp its gate voltage around -0.6 V. However, if auxiliary winding is not well coupled, gate voltage of the *SR* can be slightly positive instead of being clamped to -0.6 V. This unbalance can lead to keep the SRs on when they should be off, especially if MOSFETs have a low threshold voltage. It is partially solved connecting equalizing resistors of high ohmic value between gate and source, as shown in Fig. 3. Anyway, this unbalance can be avoided in the design of the transformer, guaranteeing a good coupling between the auxiliary winding and the rest of windings. In the following sections, the influence of the main parameters of this circuit is analyzed theoretically and through simulations.

IV. Testbench Converter

To analyze the influence of the main parameters on the performance of the single winding self-driven synchronous rectification technique, a low-voltage converter has been simulated and actually tested with different transformers. It is a half bridge topology with SWSDSR (Fig. 3). Main specifications of the prototype are shown in Table I. The prototype is built on a standard multilayer PCB (12 layers). Copper thickness is 70 μm and insulator thickness is 170 μm.

The prototype uses a low profile transformer (EE18 core) integrated in the multilayer PCB. The turns ratio is (8 : 1 : 1 : 4). Interleaving techniques are used in order to improve the coupling among the windings. The four windings of the transformer are shown in Fig. 3: there is one primary winding (PRIM), two secondary windings (SEC1 and SEC2), and one auxiliary winding (AUX) that is used to drive the Synchronous Rectifiers.

The prototype has been tested with two planar transformers: Transformer A and Transformer B (Fig. 4). The magnetic core (EE18) and the PCB technology are the same for both transformers. Transformer A has an additional winding on the right, which is used to generate the auxiliary voltage in the real converter. Interleaving techniques have been used in both trans-

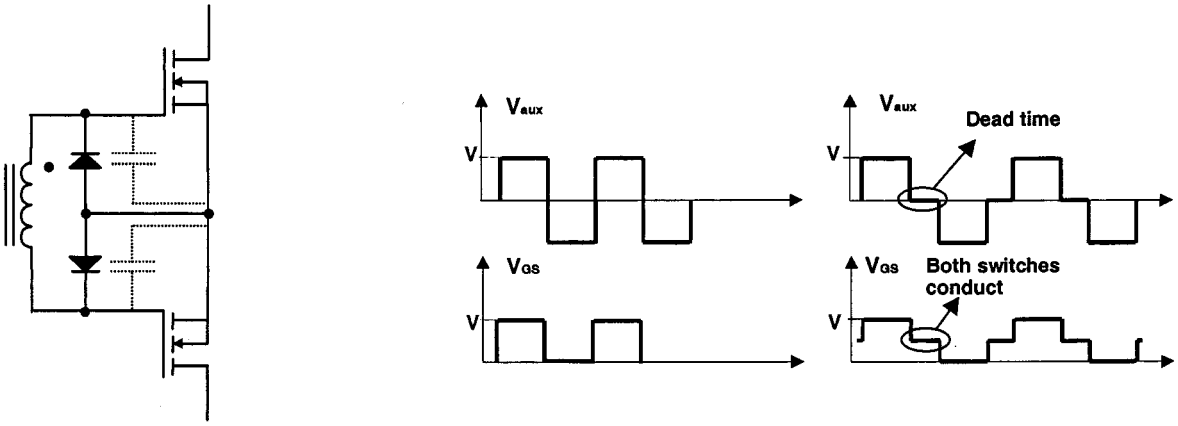

Fig. 2. SWSDSR scheme and corresponding voltage waveforms.

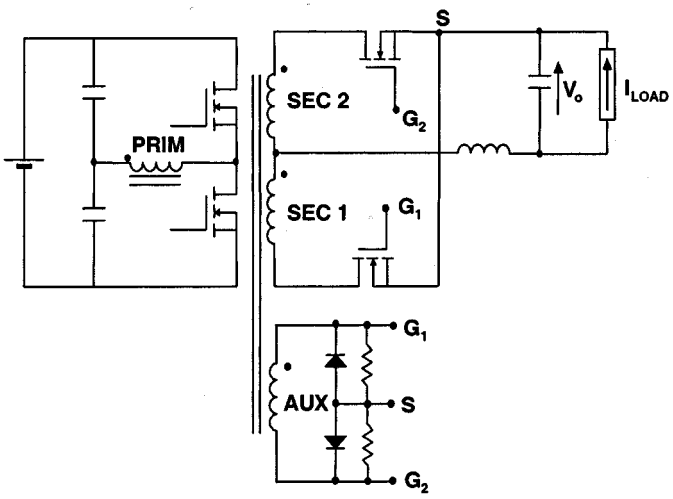

Fig. 3. Half bridge topology with single winding self-driven synchronous rectification (SWSDSR).

TABLE I
SPECS OF THE TESTBENCH CONVERTER

Input voltage range	36 V – 72 V
Output voltage	1.5 V
Output power	15 W
Dimensions	50 mm ×30 mm ×10 mm
Switching frequency	100 kHz
Maximum efficiency	87 %

formers, however, it is clear that Transformer B has a better interleaving than Transformer A.

Transformer A has a bad auxiliary–primary coupling, the short circuit inductance measured between the auxiliary and primary windings is around 140 nH at 150 kHz. However, Transformer B has a good auxiliary–primary coupling, the short circuit inductance is around 30 nH at 150 kHz.

Fig. 5 shows the gate-source voltage waveforms of the *SRs* measured with both transformers. As expected, MOSFETs are on even during the dead times.

Fig. 5 also shows that using the bad-coupled auxiliary winding (Transformer A), V_{GS} is slightly positive (1 V) when the corresponding switch has to be off. However, when the auxiliary winding is well coupled (Transformer B), the circuit works properly and V_{GS} is -1 V because the diode clamps the voltage. In the next section, this behavior is analyzed.

V. INFLUENCE OF MAIN PARAMETERS

Coupling between auxiliary and primary windings affects strongly the performance of this circuit. In this section, the influence of this coupling as well as the influence of other parameters (parallel resistors, gate parasitic capacitance of *SRs*, etc.) on the goodness of this circuit are analyzed theoretically and validated with experimental results.

As explained, if auxiliary winding is not well coupled, there exists some risk of switching on the *SRs* when they should be off. In order to understand this problem, a simplified circuit is analyzed (Fig. 6). The transformer is represented as an ideal pulse voltage source, with a series resistor R_S and a series inductance L that models the coupling between the primary and the auxiliary winding.

In case of a bad coupling, the value of the inductance is high, and the transition of the gate voltage could be as shown in Fig. 7. During the transition, a resonance between the leakage inductance and gate capacitances takes place. Due to the high frequency of the resonance, the diode has no time to clamp the voltage (time interval A, in the same figure), and the voltage can be positive, charging partially the gate when the MOSFET should be off.

Assuming that gate parasitic capacitance, C, of both *SRs* is the same and it is constant, the study of the resonant transition can be done with the equivalent circuit shown in Fig. 8. The resistor R_P is the resistor connected in parallel with the *SRs*. The voltage source V_B is the step voltage that imposes the power transformer when a MOSFET of primary is switched on. Using this equivalent circuit allows a simplified analysis in a first approach, but it describes very well the influence of each parameter. Conclusions obtained with this analysis are validated through experimental results.

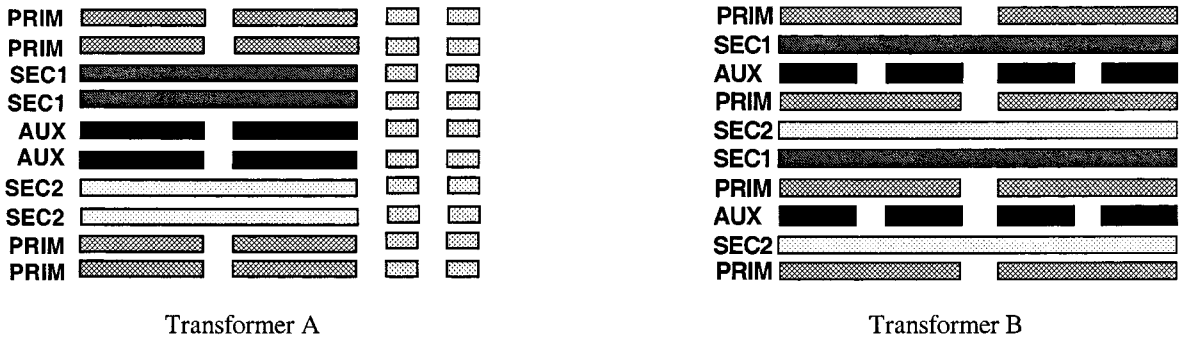

Fig. 4. Interleaved structure of transformers actually tested: (a) Transformer A and (b) Transformer B.

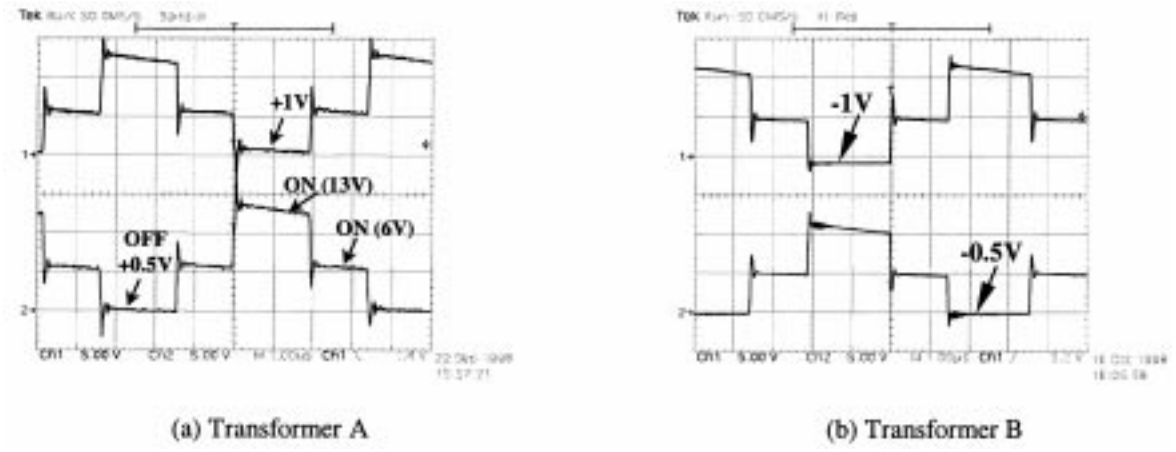

Fig. 5. Measured V_{GS} waveforms when the auxiliary winding is bad coupled (Transformer A) and well coupled (Transformer B) (5 V/div, 1 μs/div).

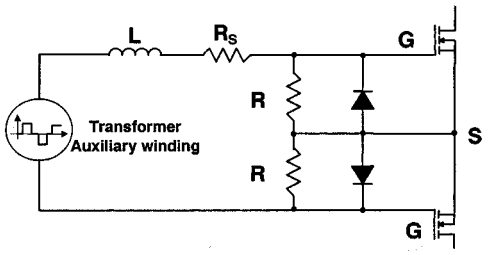

Fig. 6. Simplified circuit for the analysis.

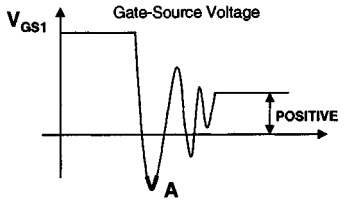

Fig. 7. Resonant transition of V_{GS} due to a bad coupling.

Circuit of Fig. 8 is a standard second-order system, which is analyzed in [14]. Oscillation of the capacitance voltage is given by

$$u_c(t) = V_B \cdot k \cdot \left[1 - \frac{e^{-\zeta \cdot \varpi_n t}}{\sqrt{1-\zeta^2}} \sin(\omega_d t)\right] \tag{1}$$

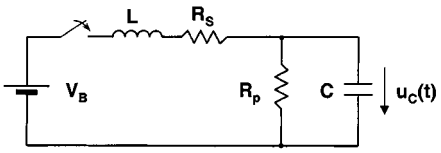

Fig. 8. Equivalent circuit for the analysis of the resonant transition.

when $0 < \zeta < 1$. Being

$$k = \frac{R_p}{R_S + R_p} \tag{2}$$

$$\omega_n^2 = \frac{R_S + R_p}{L \cdot C \cdot R_p} \tag{3}$$

$$\zeta = \frac{1}{2}\left(\frac{1}{C \cdot R_p} + \frac{R_S}{L}\right)\sqrt{\frac{L \cdot C \cdot R_p}{R_S + R_p}} \tag{4}$$

$$\omega_d = \omega_n \sqrt{1-\zeta^2}. \tag{5}$$

Typical values for L, R_S, R_P, and C in switching dc/dc power supplies make the system underdamped ($0 < \zeta < 1$) and there is a risk of wrong operation because gate voltage oscillates. If the system is overdamped ($\zeta > 1$), there will not be oscillations and the diode will clamp the gate voltage.

Theoretically, the system can be easily overdamped by means of increasing the series resistor R_S. However, it can not be done

because charge and discharge of input capacitances is slower, shifting gate pulses, and switching (on and off) *SRs* later than they should. For example, using Transformer A the system is underdamped but it becomes overdamped ($\zeta = 1.14$) if the series resistor is increased ($\mathrm{R_S} = 15\ \Omega$). Although driving waveforms are good because they do not oscillate and diode clamps the voltage to -1 V (Fig. 9), circuit can not be overdamped because gate pulses are delayed, causing a malfunctioning of the power topology.

The system will be underdamped in the majority of converters, however *SRs* can be driven correctly, if oscillations are quickly damped. Hence, the damping constant ($\zeta \cdot \omega_n$) should be as high as possible:

$$\zeta \cdot \omega_n = \frac{1}{2}\left(\frac{1}{C \cdot R_p} + \frac{R_S}{L}\right) \tag{6}$$

The value of the damping constant depends mainly on the value of the leakage inductance (L). Reducing the parameters C and $\mathrm{R_P}$ improve the behavior of the circuit, however it has less influence on the damping constant as well as on the operation of the circuit than the leakage inductance, L, does.

Besides, the number of MOSFETs in parallel required to handle the output current limits the reduction of C. The reduction of $\mathrm{R_P}$ increases the losses in this resistance, this resistor helps to improve the circuit but it is not the key parameter.

Since the most important parameter is the leakage inductance (L), a good coupling between the auxiliary and the primary windings is mandatory for a proper operation of the circuit. Influence of this coupling is clearly shown with the different behavior of the circuit with Transformer A and Transformer B. The circuit behaves properly with Transformer B since the auxiliary winding is well coupled; damping constant is around $2 \cdot 10^6\ \mathrm{s}^{-1}$. However, when it is worse coupled (Transformer A), oscillations are slower damped since the damping constant is smaller (around $0.6 \cdot 10^6\ \mathrm{s}^{-1}$) and the circuit miss-operates under some conditions (Fig. 5).

Other parameter that affects performance of the driving circuit is the step voltage, $\mathrm{V_B}$, imposed by the transformer. It depends on the selected voltage to drive the *SRs*. As seen in (1), the higher the $\mathrm{V_B}$, the higher the amplitude of the oscillations and hence, the risk of malfunctioning of the circuit is greater. Therefore, when oscillations are not quickly damped (bad coupling), there is more risk of malfunctioning for the higher $\mathrm{V_B}$.

The main conclusion of this analysis is that the coupling between auxiliary and primary windings is critical to achieve good performance with this new driving scheme. Other parameters as parallel resistors or gate capacitances can help only if the auxiliary–primary coupling is good enough.

VI. Influence of Different Couplings

As seen above, the goodness of *SWSDSR* technique is highly dependent on the auxiliary–primary coupling. Besides, it is known that keeping a high coupling between primary and secondary windings is critical to reduce voltage spikes, switching losses in the converter, etc. The magnetic coupling between the secondary and auxiliary windings also affects drastically the performance of the converter, to such an extent that the converter may even miss-operate if the synchronous rectifiers are not turned on and off at the right times.

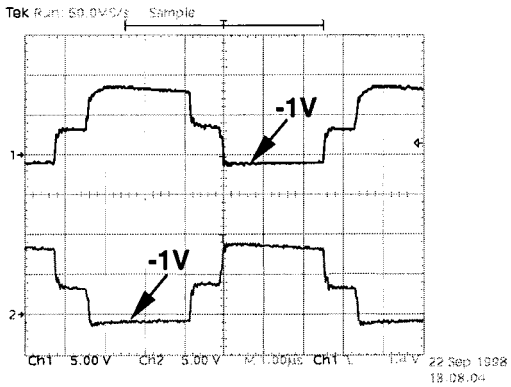

Fig. 9. Measured $\mathrm{V_{GS}}$ at both SRs with Transformer A and $\mathrm{R_S} = 15\ \Omega$ (5 V/div, 1 μs/div).

The three couplings auxiliary–primary, primary–secondary and secondary–auxiliary are very critical but some questions come out when a transformer for a SWSDSR application is designed: Is there any coupling that can be worsened to improve others? Should one of the couplings be prior? if one should, which one? These are the questions that we try to answer in this section.

Four transformers (Transformer B, C, D, and E) with different interleaving are compared to analyze the influence of the couplings. They are designed to be used in the testbench converter. Hence, the magnetic core (EE18) and the PCB technology is the same for all of them, being the interleaving the only difference. The interleaving of the considered transformers is shown in Fig. 4 (Transformer B) and Fig. 10 (Transformer C, D and E).

All the transformers are modeled to characterize and quantify their behavior. Models are based on a frequency dependent fully distributed model [12], being generated with a FEA tool [13].

In Transformer B neither coupling is prior, this interleaving tries to optimize the coupling among all the windings. This transformer is actually tested in the prototype.

In Transformer C the coupling between auxiliary and primary windings is worse than in Transformer B but there is still a good coupling between secondary and auxiliary windings. Interleaving of Transformer C is the same than Transformer A (Fig. 4) but Transformer C does not have the additional winding on the right part.

In Transformer D the auxiliary–primary coupling is optimized while coupling of secondary windings with primary and auxiliary windings is worse than in the previous designs. Secondary windings are in the bottom part without any interleaving.

Finally, Transformer E optimizes primary–secondary coupling and gives less importance to the couplings of the auxiliary winding with primary and secondary. Auxiliary winding is in the bottom part without any interleaving.

Once transformer models are generated, several small signal tests are done to quantify how are the couplings between the different windings. Table II summarizes the simulation results obtained with different short-circuited tests. Short-circuit inductance and resistance were taken at 100 kHz. Short-circuit induc-

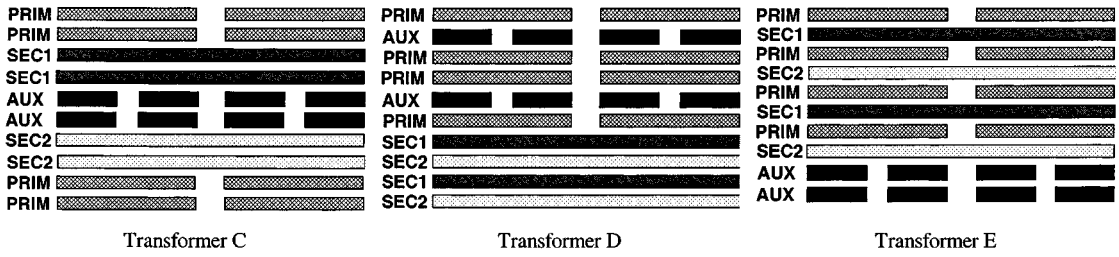

Fig. 10. Interleaved structure of Transformer C, Transformer D and Transformer E.

TABLE II
SIMULATION RESULTS OF SHORT-CIRCUIT TEST (100 KHZ)

	From Primary with Secondary short-circuited		From Auxiliary with Primary short-circuited		From Auxiliary with Secondary-short circuited	
	R (mΩ)	L (nH)	R (mΩ)	L (nH)	R (mΩ)	L (nH)
Transformer A	230	210	110	130	100	60
Transformer B	105	50	50	30	65	35
Transformer C	115	140	50	80	45	35
Transformer D	115	565	55	15	50	155
Transformer E	110	45	50	180	50	130

tance between each pair of windings gives us a good idea about how is their coupling.

From Table II the following conclusions are drawn.

- Primary–Secondary coupling: It is good in Transformer B and E, however these windings are bad coupled in Transformer C and D.
- Auxiliary–Primary coupling: It is good in Transformer B and D and bad in Transformer C and E.
- Auxiliary–Secondary coupling: It is good in Transformer B and C and bad in Transformer D and E.

All the transformers were simulated with the power topology to analyze the influence of the windings coupling on the performance of the SWSDSR scheme. Fig. 11 shows the gate-source and drain-source voltage waveforms obtained in one of the synchronous rectifiers when the power topology is simulated with the models of different transformers. The circuit has been simulated under the same conditions ($V_{IN} = 36$ V, $I_{LOAD} = 10$ A) with each transformer.

- Voltage waveforms with Transformer B are very good because all the windings are very well coupled, gate-source voltage is -0.6 V (clamped by the diode) when the SR has to be off.
- However, in Transformer C, windings coupling is not so good and SWSDSR scheme does not work. As explained, if the auxiliary winding is not well coupled with the primary, the SWSDSR scheme can not work properly and SRs could conduct when they should be off. In this case, gate-source voltage is $+0.6$ V when the SR has to be off, but if input voltage is increased up to 48 V (instead of 36 V) this positive level is higher and SRs are on when they should be off.
- Transformer D is a very interesting case. Although secondary is bad coupled with the rest of the windings, SWSDSR scheme works properly (gate-source voltage is -0.6 V) because auxiliary winding is well coupled with primary. Of course, a bad coupling of the secondary winding with the primary increases the losses in the converter; a higher spike in drain-source voltage is seen in Fig. 11. Besides, a bad coupling of the secondary winding with the auxiliary affects the timings in that SRs are turned on and off, which means again higher losses in the converter. This design points out the importance of the auxiliary–primary coupling.
- Transformer E is just the opposite case than Transformer D, the secondary is well coupled with the primary and the auxiliary is bad coupled with primary and secondary. SWSDSR scheme does not work since auxiliary is bad coupled with primary. In this case, gate-source voltage is $+1.5$ V when input voltage is 36 V but the converter does not work for higher input voltages.

Main conclusion of this analysis is that the auxiliary–primary coupling is the most important to get good performance with the SWSDSR scheme. Of course, primary–secondary and auxiliary–secondary couplings are very important to optimize the power converter but auxiliary–primary coupling is critical to keep the SRs off when they should.

VII. EXPERIMENTAL VALIDATION

Two prototypes have been fully tested in order to validate the SWSDSR scheme. The selected topologies drive the transformer in a different way. One is the standard half bridge

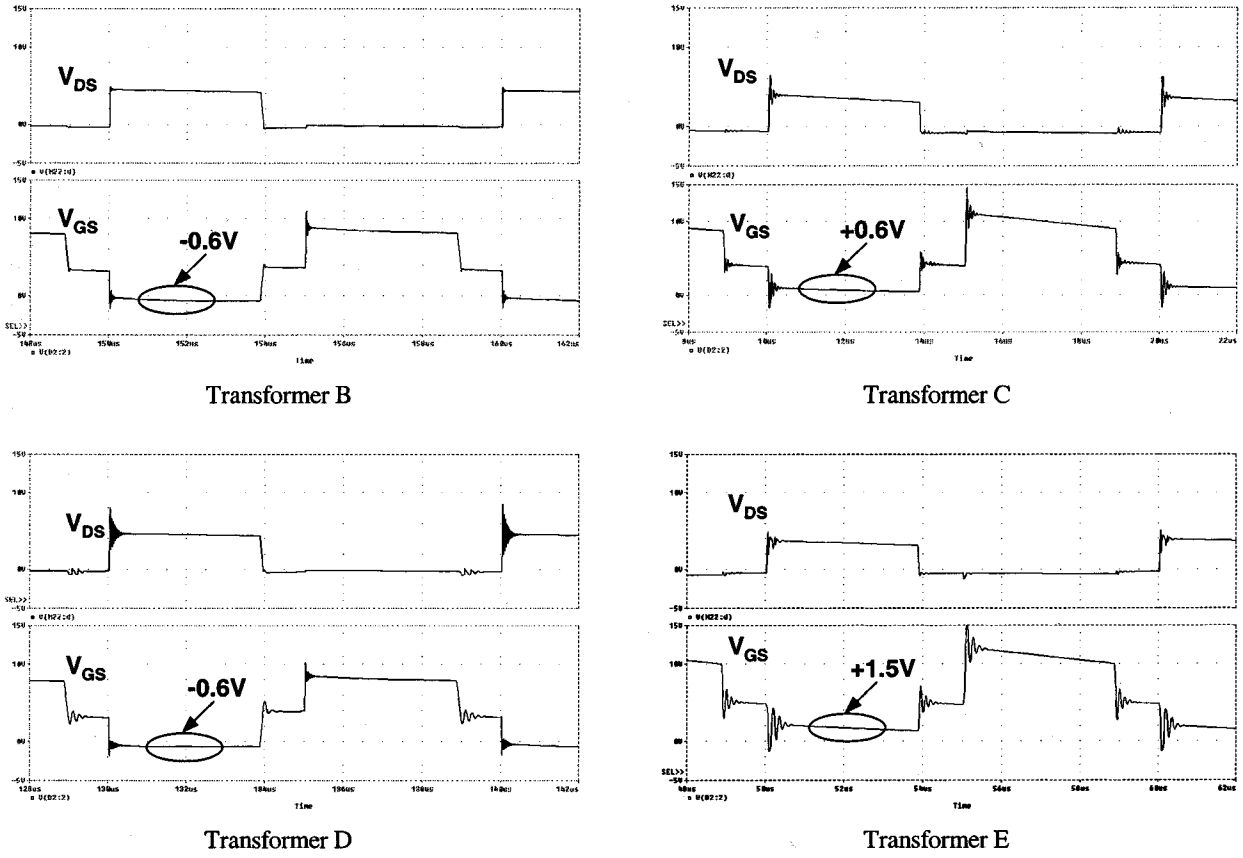

Fig. 11. Simulation results with the four transformers: gate–source ($\mathrm{V_{GS}}$) and drain–source ($\mathrm{V_{DS}}$) voltage waveforms of one synchronous rectifier.

topology, which drives symmetrically the transformer with dead times. The other is the half bridge with complementary control operating at 50% duty cycle, which also drives the transformer symmetrically but without dead times.

A. Experimental Results With the Prototype A

Prototype A, standard half bridge topology, works with a wide input voltage range (36 V–72 V), it is the testbench converter (Section IV) used to analyze the influence of the main parameters on the SWSDSR scheme. Measurements on this converter show that the new self-driven technique works if transformer windings are properly coupled (Transformer B). Fig. 5 shows how SRs are on even during the dead times of the transformer. More information of this prototype is available in [10].

This prototype has also been used to validate the simulation conclusions of Section VI. Simulation results match very well with experimental results. When Transformer A is used, the $\mathrm{V_{GS}}$ is slightly positive at low input voltage (36 V), but this unbalance increases at higher input voltages and SWSDSR does not work in the simulations as well as in the prototype. However with Transformer B, the SWSDSR scheme works properly in the simulations as well as in the actual converter.

B. Experimental Results With the Prototype B

Prototype B is a half bridge topology and has been tested in two modes: with and without dead times. Specifications of this prototype are shown as follows:

- Output voltage: 1.5 V.
- Input Voltage is around 24 V.
- Maximum output current: 15 A.
- Switching frequency: 100 kHz.

Transformer is made with a low profile RM10 core using PCB layers for the windings. Synchronous rectifiers are three Si4410 (13 mΩ) in each branch. Power MOSFETs are packaged in SO8, without heat sink and directly mounted on a standard PCB.

Fig. 12 shows $\mathrm{V_{GS}}$ waveforms for different output currents when the transformer is driven without dead times (half bridge with complementary control operating at 50%). There is a small unbalance in $\mathrm{V_{GS}}$ (due to the coupling of the auxiliary winding) which is dependent on the commutation (zero voltage switching or not) in the primary side. At light load (1 A) there is almost no ZVS, then parasitic capacitances are not discharged when the primary MOSFET is switched on and therefore, the step voltage $\mathrm{V_B}$ imposed by the transformer is high, increasing the amplitude of the oscillation (1) and worsening the behavior of the circuit. At light load, gate voltage is $+1$ V (Fig. 12) during off times. However, at higher load (5 A), there is ZVS and parasitic capacitances are almost discharged when primary MOSFET is switched on, then step voltage $\mathrm{V_B}$ is very small and gate voltage is 0 V during off times.

Fig. 13 shows the efficiency of prototype B when the transformer is driven without dead times (half bridge with complementary control operating at 50%) and SWSDSR scheme is used. The converter is working at constant duty cycle $\mathrm{d} = 50\%$ and the input voltage is slightly modified to regulate the output

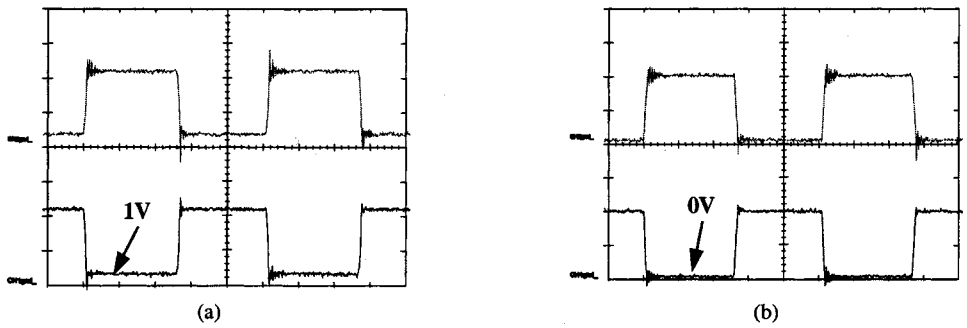

Fig. 12. HBCC prototype with SWSDSR (d = 50%): V_{GS} in SRs (5 V/div, 2 μs/div) when output current is (a) 1 A and (b) 5 A.

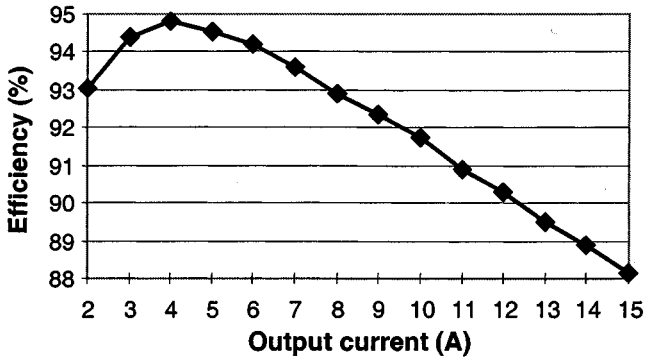

Fig. 13. Prototype B without dead times (HBCC with d = 50%) and with SWSDSR: Efficiency of the power stage.

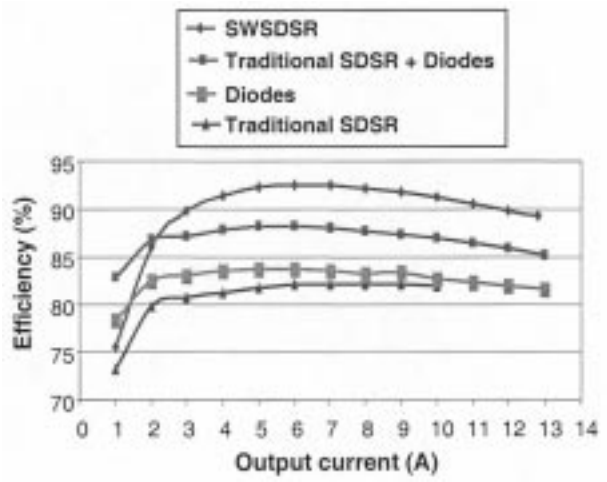

Fig. 14. Efficiency measured in prototype B with dead times (d = 25%) and with different rectification strategies: Diodes, traditional SDSR, traditional SDSR with diodes and the new SWSDSR.

voltage. The maximum efficiency obtained is very high (almost 95% in the power stage, 92.8% for the overall converter) at relatively light loads (5 A). The decrease of the efficiency (88% at 15 A) when load is increased, is due to the temperature rise of the MOSFETs as well as the increase of conduction losses in the layers of the standard PCB (copper thickness is 35 μm). It should be noted that MOSFETs are SMD devices and they do not have heat sink and are mounted on a standard PCB.

Prototype B has been also tested with dead times in the transformer (standard half bridge topology operating around 25% duty cycle) in order to show the benefits of using SWSDSR. Different rectification techniques have been tested to compare them; measured efficiency with each one is shown in Fig. 14. For loads higher than 2 A, SWSDSR technique reduces the losses in prototype B much more than the rest of techniques.

1) Losses of prototype B with the SWSDSR are very low (1.4 W at 10 A, 91% efficiency) since MOSFETs are on during the dead times.
2) Traditional SDSR have been implemented with auxiliary windings since voltage in secondary is very low (1.5 V). Interleaving of the auxiliary windings is the same than the one used with the SWSDSR technique. Body diodes conduct during the dead times increasing the losses drastically (3.3 W at 10 A, 81.8% efficiency) and limiting the maximum power capability of the converter.
3) Prototype B has been also tested using only Shottky diodes as rectifiers (85CNQ015). Measured losses are similar than in the previous case (3.1 W at 10 A, 82.7% efficiency). Forward voltage is around 0.3 V.
4) Finally, the same shottky diodes have been paralleled with the traditional SDSR with auxiliary windings. Although losses are reduced since shottky diodes conduct during the dead times instead of body diodes (2.2 W at 10 A, 87% efficiency), better results are achieved with the SWSDSR technique saving the room and the cost of the Shottky diodes.

VIII. Conclusions

A new circuit to drive the synchronous rectifiers of a very low voltage dc/dc converter is proposed, analyzed and validated. It is called single winding self-driven synchronous rectification (SWSDSR) scheme. The main characteristics of the new driving circuit are:

1) free selection of the driving voltage;
2) low driving energy involved in the process;
3) capability to maintain both *SRs* on even when the voltage in the transformer is zero, which is impossible to do in traditional self-driven approaches.

This new self-driven scheme is applicable to any topology that drives symmetrically the transformer (push–pull, half bridge, etc.) even for a wide input voltage range. It is also applicable to forward with active clamp and half bridge with complementary control only if the duty cycle is 50%.

The main disadvantage of this scheme is that its performance is highly dependent on windings coupling. All the couplings are very important to optimize the power converter but auxiliary–primary coupling is critical to make possible the use of SWSDSR technique. Design of the power transformer is especially complex and modeling techniques are recommended.

This new technique has been fully validated in two very low voltage (1.5 V) converters: Half bridge and half bridge with complementary control (d=50%). A 1.5 V Half Bridge prototype shows much higher efficiency with the new SWSDSR (91% @ 10 A) than with other rectification techniques: schottky diodes (82.7% @ 10 A), traditional SDSR with auxiliary windings (81.8% @ 10 A), or even traditional SDSR with auxiliary windings and schottky diodes in parallel (87% @ 10 A).

SWSDSR approach allows the use of fast dynamic topologies (half bridge or push pull) to supply the new low-voltage fast-transient loads, which is an interesting alternative because input voltage can be high (24 V, 48 V).

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