Analysis and Design of SEPIC Converter in Boundary Conduction Mode for Universal-line Power Factor Correction Applications

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Abstract **- In this paper, the SEPIC converter operated in boundary conduction mode for power factor correction applications with arbitrary output voltage is proposed, analyzed and designed. By developing an equivalent circuit model for the coupled inductor structure, the SEPIC converter with or without coupled inductors (and ripple current steering) can be analyzed and designed in a unified framework. Power factor correction under boundary conduction operation mode can be achieved conveniently using a simple commercially available control IC. Experimental results are provided to validate the circuit design.**

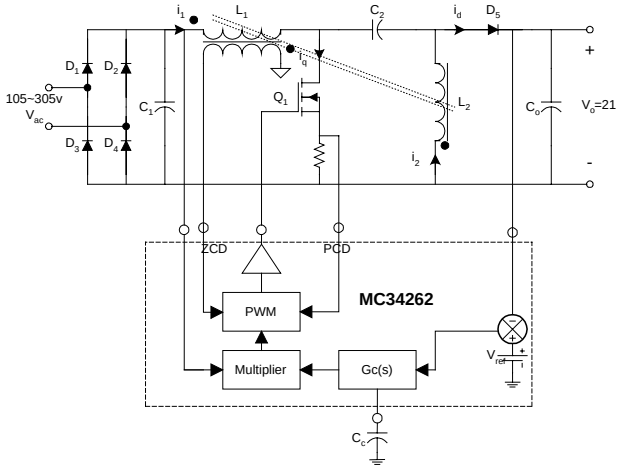
I. INTRODUCTION

In universal line input ($85V_{rms}$~$264V_{rms}$) power factor correction (PFC) applications, the Boost converter is commonly used. However the output DC voltage of the Boost converter has to be set to be greater than the input line peak voltage (normal greater than *400V*). In some applications where an intermediate output voltage level (say *48V*, *210V* or so) is required, converters with step-up and step-down conversion ratio, for examples SEPIC, Flyback and Cuk, are potential candidates.

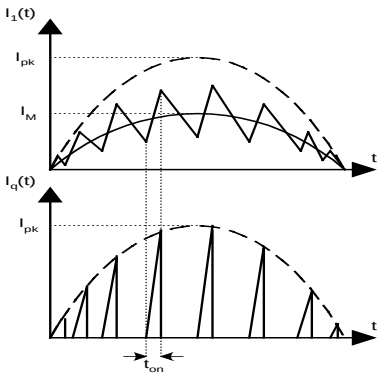
Boost [1,2] and Flyback [3,4] converters at boundary conduction mode (BCM) are generally accepted for low-power PFC applications. At BCM, a turn-on switching process is initiated when the output diode current falls to zero, while a turn-off switching process is established when the peak transistor current reaches the threshold level set by the controller output. This ensures the converter operating at the boundary of Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM) at the expense of variable switching frequency over the AC line period. As a result, there is no diode recovery current problem in a BCM converter. At same power level and design consideration, the peak inductor current is smaller in a BCM converter than in a DCM converter.

SEPIC converter at BCM is found to be suitable as a low harmonics rectifier in this paper. Fig.1 shows that a single controller chip can realize the BCM operation in a SEPIC single-phase rectifier. Compared to a flyback converter, the input current in SEPIC converter is continuous and thus the SEPIC rectifier needs smaller volume of input filter.

It is well known that inductors could be realized in same magnetic core, provided they are fed by similar voltage waveform [5,6,7]. The impedance characteristic of coupled inductors is found to be independent of the feeding voltages of both primary and secondary sides. This leads to a simplified model of coupled-inductors, such that the analysis process of the coupled-inductor and uncoupled-inductor SEPIC can be unified. The ripple steering phenomenon of coupled inductors can also be explained in the same framework.



(a)



(b)

Fig. 1 (a) Experimental BCM SEPIC converter, (b) ideal input inductor current and transistor current waveforms

From the analysis, design and experimental results, it is shown that the SEPIC converter under BCM results in nearly sinusoidal and in-phase input current with small ripple due to current steering effect of coupled inductor. It features adjustable output voltage and no inrush current. Unlike the Flyback converter, the SEPIC converter does not need a lossy snubber circuit or extra active clamping circuit. Therefore, higher efficiency and simpler implementation are expected.

II. ANALYSIS OF UNCOUPLED-INDUCTOR SEPIC CONVERTER AT BCM

During the analysis of converter operation, only the governing factors are being considered. Thus, the following assumptions are made.

A. The input line voltage $V_{in}(t)$ is ideally sinusoidal. No voltage drop or losses will be considered in the bridge rectifier. The input voltage is

$$v_{in}(t) = V_M \sin(\omega t) \tag{1}$$

Then, the rectified voltage becomes

$$v_1(t) = V_M \left|\sin(\omega t)\right| \tag{2}$$

B. The twice frequency ripple on DC bus is neglected. The output voltage is assumed as a constant DC value V_o in quasi-steady state operation.

C. The bandwidth of output voltage feedback loop is selected to be relatively low, compared to the line frequency, such that the compensator output can be considered constant for a half line cycle. As a result, the peak transistor current is enveloped by a rectified sinusoid:

$$i_{pk}(t) = I_{pk} \left|\sin(\omega t)\right| \tag{3}$$

The value of I_{pk} is determined by the compensator output and considered constant during the line half cycle.

Fig. 2 portrays the typical current waveforms in SEPIC converter at the boundary conduction mode. The peak to peak ripple on uncoupled inductors are described in (4) and (5).

$$\Delta i_1(t) = v_1(t) t_{on}(t) / L_1 \tag{4}$$

$$\Delta i_2(t) = v_1(t) t_{on}(t) / L_2 \tag{5}$$

When the transistor is conducting, the peak transistor current is the sum of two inductor current and expressed as:

$$i_{pk}(t) = (\frac{1}{L_1} + \frac{1}{L_2}) t_{on}(t) V_M \left|\sin(\omega t)\right| \tag{6}$$

The transistor "on" time can be obtained by substituting (3) into (6).

$$t_{on}(t) = L_e I_{pk} / V_M = T_{on} \tag{7}$$

where $L_e = L_1 // L_2$. This equation shows that the transistor "on" time of BCM SEPIC is constant under stable load and input voltage conditions. To further evaluate the switching frequency, we apply volt-seconds balance on L_1 and L_2, and find out the transistor "off" time as:

$$t_{off}(t) = T_{on} v_1(t) / V_o \tag{8}$$

The instantaneous switching frequency is then described as:

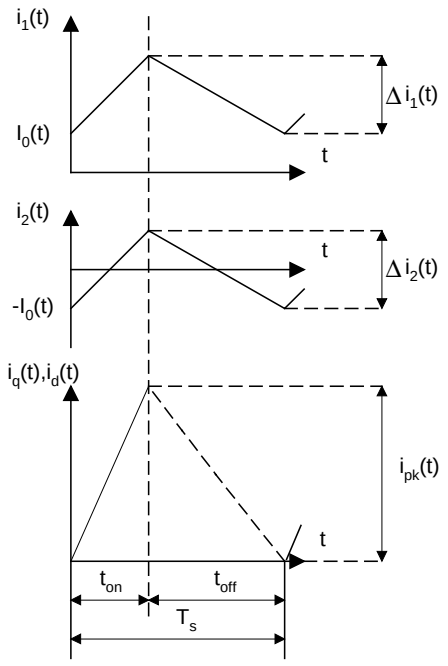


Fig. 2 Waveforms of uncoupled-inductor SEPIC at BCM

$$f_s(t) = \frac{1}{T_{on}(1 + v_1(t)/V_o)} \tag{9}$$

It is seen that the switching frequency changes along with line input voltage in the BCM SEPIC converter.

Due to the operation of BCM, the transistor will conduct zero current after being turned on. To satisfy the charge balance on C_2 in a switching cycle, the inductors current will not be zero at the point of turning on transistor, instead there is a shift $I_o(t)$ with different signs applied. The charge balance on C_2 in a switching cycle can be written as:

$$\left[\frac{1}{2}\Delta i_2(t) - I_o(t)\right] T_{on} = \left[\frac{1}{2}\Delta i_1(t) + I_o(t)\right] t_{off}(t) \tag{10}$$

The inductor current shift can be obtained by solving (10).

$$I_o(t) = \frac{1}{2} T_{on} v_1(t) \left(\frac{1}{L_2}\frac{V_o}{v_1(t) + V_o} - \frac{1}{L_1}\frac{v_1(t)}{v_1(t) + V_o}\right) \tag{11}$$

The average value of rectified input current is then found as

$$i_{1,avg}(t) = \frac{1}{2}\Delta i_1(t) + I_o(t) = \frac{T_{on}}{2L_e}\frac{V_o}{v_1(t) + V_o} v_1(t) \tag{12}$$

By further simplification, it becomes

$$i_{1,avg}(t) = \frac{1}{2} I_{pk} \frac{\left|\sin(\omega t)\right|}{1 + K_v \left|\sin(\omega t)\right|} \tag{13}$$

where the input-output ratio is defined as: $K_v = V_M / V_o$.

The filtered input line current is then:

$$i_{in}(t) = \frac{1}{2} I_{pk} \frac{\sin(\omega t)}{1 + K_v \left|\sin(\omega t)\right|} \tag{14}$$

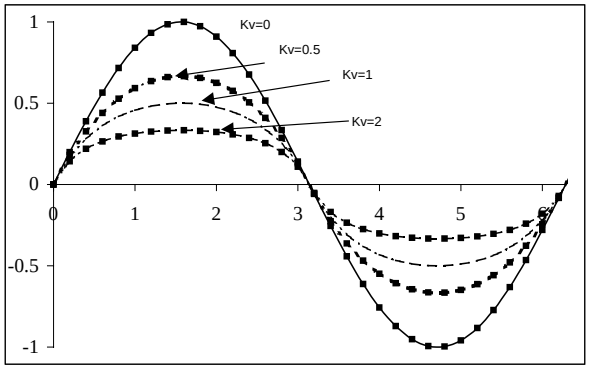


Fig. 3 Input current waveform with different K_v

The input current waveforms of different values of K_v are plotted in Fig. 3. It is shown that the current is sinusoidal for $K_v=0$ but will be distorted as K_v increases. This means that the SEPIC at BCM can not achieve unity power factor performance except at extreme condition.

Next step is to find out the input current as a function of averaged input power, which is:

$$P_{in} = \frac{1}{T_{ac}} \int_0^{T_{ac}} \left[\frac{I_{pk}}{2} \frac{\sin(\omega t)}{1 + K_v \left| \sin(\omega t) \right|} \cdot V_M \sin(\omega t) \right] dt \qquad (15)$$

We can define

$$F(x) = \frac{1}{T_{ac}} \int_0^{T_{ac}} \left[\frac{\sin^2(\omega t)}{1 + x \left| \sin(\omega t) \right|} \right] dt \qquad (16)$$

then, the average input power is then expressed in a compact form as

$$P_{in} = \frac{1}{2} V_M I_{pk} F(K_v) \qquad (17)$$

A closed form solution and approximate express for $F(x)$ can be found in [8]. It is now possible to find the enveloped peak current I_{pk} from the specified input voltage, output power and expected efficiency.

$$I_{pk} = \frac{2P_o}{\eta V_M F(K_v)} \qquad (18)$$

For the switch loss estimation, it is found out that the RMS value of transistor current and average diode current are

$$I_{q,rms} = I_{pk} \sqrt{\frac{F(K_v)}{3}} \qquad (19)$$

$$I_{d,avg} = I_o \qquad (20)$$

By substituting expression for I_{pk} into (10), the switching frequency can be expressed as a function of input voltage, regulated output voltage, output power and equivalent inductance.

$$f_s(t) = \frac{\eta V_M^2 F(K_v)}{2P_o L_e (1 + K_v \left| \sin(\omega t) \right|)} \qquad (21)$$

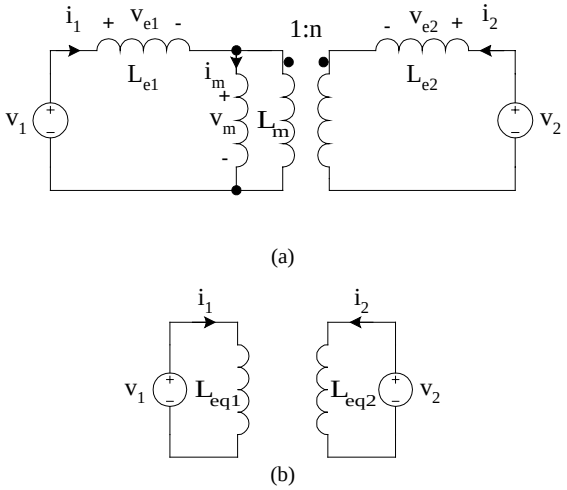


Fig. 4 Equivalent circuit model of coupled-inductor structure: (a) T-model, (b) simplified model

III. COUPLED-INDUCTOR MODELING

The ripple-steering phenomenon was originally investigated in Cuk converter [6]. It is well known that two or more inductors fed by same or scaled voltage waveforms can be coupled on same magnetic core. In the following analysis, it is found that the impedance characteristic of coupled-inductor is independent of the feeding voltage in SEPIC converter, as a result the parameters in the simplified model are only related to the physical structure of coupled-inductors.

Fig. 4 is the general T-model of a two-winding coupled-inductor, in which the leakage inductors of primary and secondary sides are modeled as L_{e1} and L_{e2} respectively. The basic voltage and current relation sare shown in (22).

$$\begin{cases} v_1(t) = L_{e1} \dfrac{di_1(t)}{dt} + L_m \dfrac{di_m(t)}{dt} \\ v_2(t) = L_{e2} \dfrac{di_2(t)}{dt} + nL_m \dfrac{di_m(t)}{dt} \\ \dfrac{di_m(t)}{dt} = \dfrac{di_1(t)}{dt} + n \cdot \dfrac{di_2(t)}{dt} \end{cases} \qquad (22)$$

In the coupled inductors in SEPIC converter, both windings are fed by equal voltage which is $v_1(t) = v_2(t)$. Under this condition, primary and secondary current condition can be wirtten as:

$$\left[L_{e1} - (n-1)L_m \right] \frac{di_1(t)}{dt} = \left[L_{e2} + (n-1)nL_m \right] \frac{di_2(t)}{dt} \qquad (23)$$

The zero ripple condition for both terminals can be directly derived and described in the phisical relations between leakage inductance, magnitizing inductance and winding turns ratio as followings:

Primary side: $\frac{di_1(t)}{dt} = 0 \Rightarrow L_{e2} = (1-n)nL_m$ (24)

Secondary side: $\frac{di_2(t)}{dt} = 0 \Rightarrow L_{e1} = (n-1)L_m$ (25)

From (22) and (23), a simplified equivalent circuit model, obeying (26) and (27), is obtained and shown in Fig. 4(b).

$$\begin{cases} v_1(t) = L_{eq1}\frac{di_1(t)}{dt} \\ v_2(t) = L_{eq2}\frac{di_2(t)}{dt} \end{cases} \quad (26)$$

$$\text{where, } \begin{cases} L_{eq1} = \frac{L_{e1}L_{e2} + L_mL_{e2} + n^2L_mL_{e1}}{L_{e2} + n(n-1)L_m} \\ L_{eq2} = \frac{L_{e1}L_{e2} + L_mL_{e2} + n^2L_mL_{e1}}{L_{e1} - (n-1)L_m} \end{cases} \quad (27)$$

The simplified model shows that coupled inductors fed by the same voltage waveforms will exhibit as two equivalent inductors, which only depend on the physical inductor structure instead of the feeding voltages. So that, the analysis results from the uncoupled inductor SEPIC converter can be extended to coupled inductor SEPIC converter.

Furthermore, if those two windings were wound symmetrily, the major factor that determines the difference between primary and secondary leakage inductance is turns ratio. The leakage inductors have following relationship:

$$L_{e2} = n^2L_{e1} \quad (28)$$

By defining the coupling coefficient $k_r = L_{e1}/L$ *with* $L=(L_m+L_{e1})$, the equivalent inductance and zero ripple condition can be written in compact forms:

$$\begin{cases} L_{eq1} = \frac{nk_r(2-k_r)}{(n-1)+k_r}L \\ L_{eq2} = \frac{nk_r(2-k_r)}{\frac{(1-n)}{n}+k_r}L \end{cases} \quad (29)$$

Primary side zero ripple condition: $k_r = 1-n$ (30)

Secondary side zero ripple condition: $k_r = \frac{n-1}{n}$ (31)

These equations agree with the results in [6].

IV. SMALL SIGNAL MODELING

The modeling approach for ideal rectifier with pure sinusoidal input current waveform has been proposed in [8] and [9]. Due to the rigid restriction on the input current, the output voltage will have twice line frequency harmonics, which should not be regulated by the voltage feedback loop. Hence the bandwidth of output voltage loop will be much lower than the line frequency and it is unnecessary to model the system behavior of frequency higher than the line frequency. Upon this, the approach in [9] can extend to BCM SEPIC which has a non-sinusoidal but periodic input current waveform at line frequency.

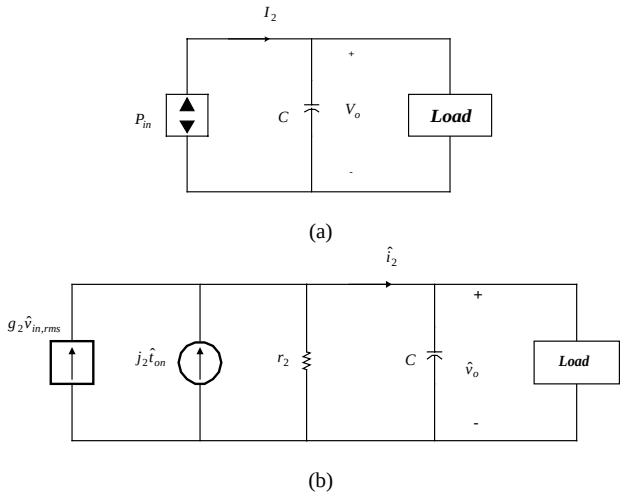


Fig. 5 Modeling SEPIC rectifier: (a) large-signal model, (b) small-signal model

Under quasi-steady state operation, the output port of the rectifier can be modeled as in Fig. 5(a). The second and higher harmonic components are removed by averaging over one-half of the ac line cycle. Average power in (17) can be rewritten in (32) as a function of input RMS voltage, transistor "on" time, which is proportional to control input.

$$P_{in} = \frac{F(K_v)}{L_e}V_{in,rms}^2T_{on} \quad (32)$$

In the averaged model of Fig. 5(a), the averaged output current I_2 is given by:

$$I_2 = \frac{F(K_v)}{L_e}\frac{V_{in,rms}^2T_{on}}{V_o} \quad (33)$$

The small-signal model is obtained by linearizating (33) at the quiescent operating point and eliminating the high-order nonlinear terms.

$$\hat{i}_2 = g_2\hat{v}_{in,rms} + j_2\hat{t}_{on} - \frac{\hat{v}_o}{r_2} \quad (34)$$

where

$$g_2 = \frac{\sqrt{2}K_vF(K_v)T_{on}}{L_e} \quad (35)$$

$$j_2 = \frac{V_{in,rms}^2F(K_v)}{VL_e} \quad (36)$$

$$r_2 = \frac{2L_e}{K_v^2T_{on}F(K_v)} \quad (37)$$

The resulting small-signal model of BCM SEPIC rectifier is given in Fig. 5(b). The input to output and control to output

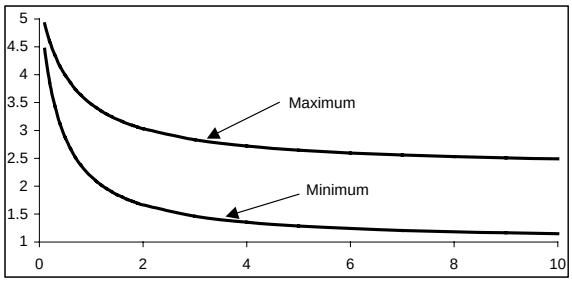


Fig. 6 The ratio of maximum frequency and minimum frequency between high line and low line as a function of turns ratio

transfer functions can then be derived from (34) if the load condition were known.

V. DESIGN CONSIDERATIONS

In this section, we first discuss the voltage stresses and current stresses of switch components. The switching frequency distribution for different line inputs is then discussed. Finally, ripple steering phenomenon is evaluated.

A. Component stresses

It is assumed that the DC output voltage for the SEPIC is V_0. Current stresses are evaluated and normalized in terms of the DC load current I_o. Voltage stresses are expressed in terms of DC output voltage V_o.

The switch voltage stress is $(1+K_v)V_o$, which shows that under maximum line input voltage, switches have the worst voltage stresses. The worst-case current stress for both transistor and diode, shown in (38), happens at low-line input and maximum output power. The peak current of both transistor and diode, RMS transistor current, and average diode current also are given by:

$$\begin{cases} I_{q,pk} = \dfrac{2P_o}{V_{M,low}F(K_v)} = \dfrac{2}{K_{v,low}F(K_{v,low})}I_o \\ I_{q,rms} = \dfrac{2}{K_{v,low}}\sqrt{\dfrac{1}{3F(K_{v,low})}}I_o \\ I_{d,avg} = I_o \end{cases} \tag{38}$$

B. Switching frequency

In order to design an EMI filter to remove most of the harmonics effectively, it is necessary to investigate the switching frequency distribution for the SEPIC at BCM.

For each given input line voltage, the minimum switching frequency happens at peak of AC line voltage, while the maximum switching frequency happens at zero crossing of AC line voltage. The ratio of switching frequency between

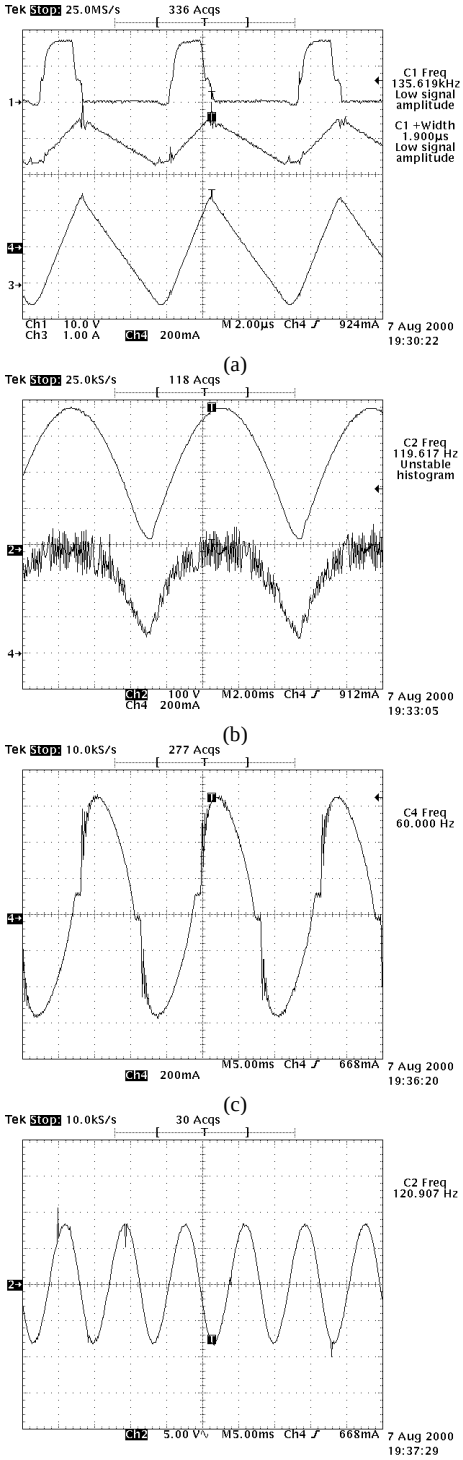


Fig. 8 Experiment results of SEPIC converter. (a)gate drive (ch1), primary (ch4, 0.2A/DIV) and secondary inductor current (ch4, 1A/DIV), (b) rectifier input voltage (ch2, 100V/DIV) and current (ch4, 0.2A/DIV), (c)line current at high-line input (0.2A/DIV, PF=0.924, THD=18.1%), (d)output voltage ac ripple at twice line frequency (5V/DIV)

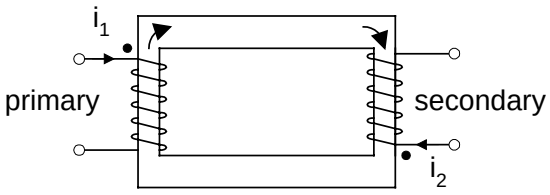


Fig. 7 Coupled inductor structure

Primary: 133 turns of Litz wire, 16/36, N3=18 turns of #26 AWG
Secondary: 80 turns of Litz wire, 20/36
*Air gap: 2*0.03''with L_p =853uH, L_{e1}=662.5uH*

TABLE I
EXPERIMENTAL RESULTS

	Vin(V)	Efficiency	PF	THD	Max(fs) (KHz)	Min(fs) (KHz)
Low line	120	89.8%	0.990	4.9	217.5	112.3
High Line	264	91.5%	0.924	18.1	426.1	142.6

P_o = 100W, V_o = 210V, $V_{in,low}$ = 120Vac, $V_{in,high}$ = 264Vac

high line and low line input at the maximum and the minimum points are given by:

$$(\frac{f_{s,high}}{f_{s,low}})_{\min}=\frac{\eta_{high}}{\eta_{low}}(\frac{V_{M,high}}{V_{M,low}})^2\frac{F_2(K_{v,high})(1+K_{v,low})}{F_2(K_{v,low})(1+K_{v,high})} \quad (39)$$

$$(\frac{f_{s,high}}{f_{s,low}})_{\max}=\frac{\eta_{high}}{\eta_{low}}(\frac{V_{M,high}}{V_{M,low}})^2\frac{F_2(K_{v,high})}{F_2(K_{v,low})} \quad (40)$$

C. Ripple steering

The ripple steering phenomenon can be visually observed from the simple model derived in Section III. In (27) or (29), when primary and secondary sides do not have the same turns, the equivalent inductance of each side will be different. Current ripple steering then happens. When $n>1$, $Leq1<L_{eq2}$, the primary side ripple will be steered from the secondary side. When $n<1$, $L_{eq1}>L_{eq2}$, the opposite phenomenon appears. Steering the ripple to secondary side can lead to reducing the conducted EMI at line input. But steering the entire ripple to the secondary side is not practical. One of the reasons is that this will increase the switching frequency to a level where driving the MOSFET and switching loss could be a problem. Also, when the turns ratio n is reduced, the switching frequency range will increase as shown in Fig. 6. This may lead to difficulties in EMI filter design.

VI. EXPERIMENTS

A prototype for the coupled-inductor BCM SEPIC topology at 100W output was built to verify the simplified coupled-inductor model and evaluate the circuit performance. The output voltage is regulated to 210V. The circuit diagram is given in Fig. 1. The MOSFET IRFPE50, diode BYM26E and PFC Controller MC34262 are used in the prototype.

The coupled-inductor structure used in [4] is adopted in the prototype and shown in Fig. 7. The SEPIC inductors and zero current detection windings are realized in a UU core. Experimental waveforms are shown in Fig. 8. In Fig. 8(a), the inductor current waveforms of both primary and secondary sides are shown. Part of the primary winding current is steered to secondary side at a turns ratio of 133/80. It is shown in Fig. 8(b) that the rectified current waveform is not pure sinusoidal as predicted in Section II. Input current and output voltage are well regulated and shown in Fig. 8(c) and (d) respectively. Experimental results of two different line inputs are concluded in Table I. The BCM SEPIC rectifier can achieve high efficiency, high power factor and acceptable THD at both high and low line inputs.

VII. CONCLUSIONS

In this paper, the SEPIC converter operating in boundary conduction mode for power factor correction application is proposed, analyzed and designed. By developing a simplified equivalent circuit model for the coupled inductor structure, the SEPIC converter with or without coupled inductors (and ripple current steering) can be analyzed and designed in a unified framework. Small signal model is presented for the purpose of designing the output voltage loop. Power factor correction under boundary conduction operation mode could be achieved conveniently using a simple commercially available control IC. Experimental results are provided to validate the circuit design.

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