High-Quality Rectifier Based on Coupled-Inductor Sepic Topology

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Abstract. A high-quality rectifier employing a coupled-inductor SEPIC topology is described, featuring high-frequency insulation and low input current ripple. Moreover, sinusoidal and in-phase input current is obtained even with constant duty-cycle. The magnetic structure is simple and cheap, allowing considerable size and cost reduction.

Converter analysis, design criteria of both power and control sections and experimental results are reported in the paper.

INTRODUCTION

For applications in which the line pollution in terms of harmonic content and displacement factor of the input current is of main concern, ac/dc converters featuring almost unity power factor are required. These high quality rectifiers, also called Power Factor Preregulators (PFP's), replace the usual capacitive-filter rectifiers, which have the disadvantage of absorbing high and narrow peak currents from the utility line. The goal is to emulate a resistive load, so achieving theoretically unity power factor, even in the presence of distorted line voltage. In order to do that, PFP's must be able to shape the input current in such a way that it represents a scaled replica of the line voltage. Between the active methods for input current shaping based on switching dc/dc converters, those employing boost topology are most diffused [1-3]. These solutions are effective and quite simple but have some limitations, like lack of insulation, output voltage higher than peak input voltage, high in-rush current during start-up and no overload protection.

In those applications in which a fast output voltage regulation is not required, like in distributed power systems, single stage solutions based on flyback, Cuk and Sepic topologies are well suited. The first converter is simpler, but it draws a pulsating input current, thus increasing the input filter requirements [4]. Instead, Cuk and Sepic topologies are free of current steps even in DICM (Discontinuous Inductor Current Mode) [5]. In addition, the Sepic topology is well suited for multi-output converters.

DICM operation (which occurs when the freewheeling diode current zeroes during the switching period) is convenient from the control point of view, because sinusoidal and in-phase input current absorption is obtained with constant on-time of the switch, thus avoiding the need of an internal current loop.

Moreover, in order to obtain a low input current ripple, a proper choice of the circuit parameters must be done, which typically leads to high values of the input inductance. This, in turn, causes an increase of input current-to-voltage lag and a decrease of the power factor.

The same property of very low input current ripple can also be achieved by exploiting another feature of Cuk and Sepic structures, i.e. the possibility to magnetically couple inductances and transformer. In this case, a single magnetic core is needed, thus allowing considerable size and cost reduction [6,7].

This paper describes a single-phase high-quality rectifier based on a coupled-inductor Sepic topology. It features: sinusoidal and in-phase input current with low ripple, high-frequency insulation, simple PWM controller and only one magnetic core.

SEPIC CONVERTER IN DICM

Operation as dc/dc converter.

Before going into the details of the proposed high quality rectifier, it is worth while to review the fundamental relations of the dc/dc Sepic converter with separate inductors, whose scheme is shown in Fig.1.

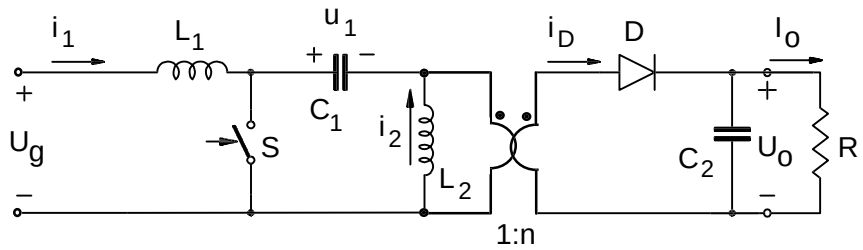


Fig.1 - Dc/dc Sepic converter scheme

The voltage conversion ratio is [5]:

$$M = \frac{U_o}{U_g} = \frac{\eta I_1}{I_o} = n \cdot \frac{D}{1-D} \qquad \text{(CICM)} \qquad (1)$$

$$M = \frac{U_o}{U_g} = \frac{\eta I_1}{I_o} = \frac{D}{\sqrt{K}} \qquad \text{(DICM)} \qquad (2)$$

where η is the converter efficiency, D is the duty-cycle and the parameter K is given by:

$$K = \frac{2L_e}{RT_s}, \text{ with } \qquad L_e = \frac{L_1 L_2}{L_1 + L_2} \qquad (3)$$

In the above equations T_s is the switching period and L_2 is the transformer magnetizing inductance.

Using (1) and (2), the value of parameter K_{crit} at the boundary between continuous and discontinuous inductor current mode results:

$$K_{crit} = \frac{(1-D)^2}{n^2} = \frac{1}{(n+M)^2} \begin{cases} K > K_{crit} \Rightarrow \text{CICM} \\ K < K_{crit} \Rightarrow \text{DICM} \end{cases} \qquad (4)$$

Another quantity of interest is the average inductor current I_2 which is given by:

$$I_2 = n \cdot i_D = n \cdot I_o \qquad (5)$$

The main difference between Sepic (and Cuk) topologies and other converters working in DICM is represented by the continuous inductor currents. In fact, DICM means that, during the switch turn-off interval, the freewheeling diode, which is carrying the sum of the inductor currents, stops to conduct. In this situation, the inductor current waveforms are as shown in Fig.2. During the interval in

which both switch and diode are non conducting, the inductor currents have a non zero value. This explains why the input current can have a low high-frequency ripple even in DICM operation.

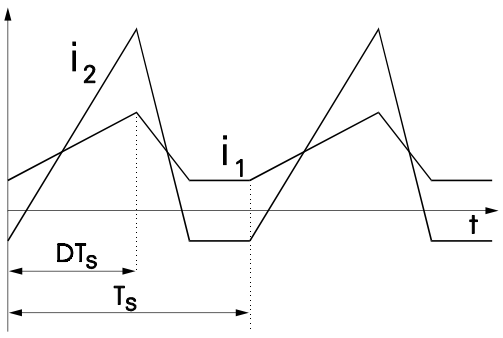


Fig.2 - Inductor current waveforms in DICM

Operation as a rectifier.

When operating as a rectifier, the dc input voltage U_g is substituted by the rectified line voltage:

$$u_g(\theta) = U_g \cdot |\sin(\theta)|$$

where $\theta = \omega_l t$. Consequently, the voltage conversion ratio becomes:

$$m(\theta) = \frac{U_o}{u_g(\theta)} = \frac{M}{|\sin(\theta)|} \qquad (6)$$

where $M=U_o/U_g$. Moreover, when the converter draws a sinusoidal current, the input power is pulsating. Thus, the output capacitor must be designed to absorb energy at twice the line frequency while keeping low the output voltage ripple (voltage-fed approach [8]). In the hypothesis of constant dc voltage, the average (respect to the switching period) inductor current $i_2(\theta)$ is equal to:

$$i_2(\theta) = n \cdot i_D(\theta) = n \cdot 2I_o \sin^2(\theta) \qquad (7)$$

and the apparent load $r(\theta)$ seen at the secondary side of the transformer is given by:

$$r(\theta) = \frac{U_o}{i_D(\theta)} = \frac{R}{2\sin^2(\theta)} \qquad (8)$$

Substituting (6) and (8) into (3) and (4) we obtain:

$$k(\theta) = \frac{2L_e}{r(\theta)T_s} = 2K_a \sin^2(\theta), K_a = \frac{2L_e}{RT_s} \qquad (9)$$

$$k_{crit}(\theta) = \frac{\sin^2(\theta)}{(M + n \cdot |\sin(\theta)|)^2} \qquad (10)$$

For the converter to operate in DICM the following condition must be satisfied:

$$K_a < \frac{1}{2(M + n \cdot |\sin(\theta)|)^2} \qquad (11)$$

The average current drawn by the converter, at constant duty-cycle and switching frequency, is sinusoidal and in phase with the line voltage and is given by [5]:

$$i_1(\theta) = \frac{1}{2}\frac{D^2 T_s}{\eta L_e} \cdot u_g(\theta) = \frac{u_g(\theta)}{R_{em}} \qquad (12)$$

where,

$$R_{em} = \frac{2\eta L_e}{D^2 T_s} \qquad (13)$$

is the emulated resistance, i.e. the converter appears to the line as a "resistor", which is the condition to achieve unity power factor.

Proposed converter.

The scheme of the proposed converter is shown in Fig.3. The mutual inductance L_M reveals the magnetic coupling between inductors L_1 and L_2. As we will explain in the next section, this arrangement allows not only to eliminate one magnetic core, but also to obtain a low high-frequency ripple in the input inductor current by means of an appropriate choice of the magnetic structure parameters.

An output voltage loop controls the converter duty-cycle D, thus varying R_{em}, by using a simple PWM generator.

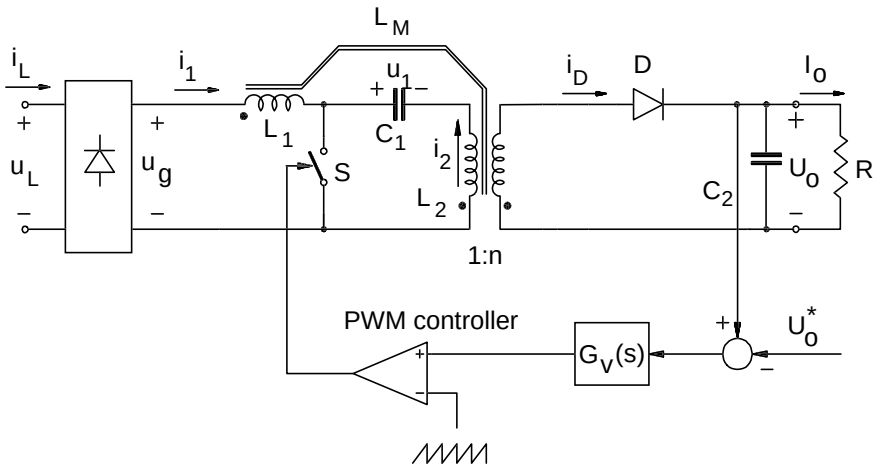
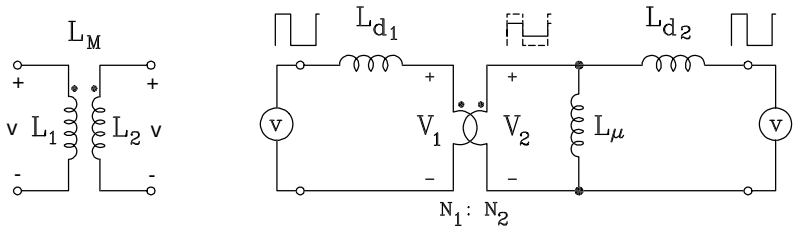


Fig.3 - Proposed converter scheme

RIPPLE-STEERING CONCEPT

The ripple-steering phenomenon was originally investigated in Cuk converters [6], but it can effectively be applied to all converter topologies in which two or more inductors are fed by similar (scaled) voltage waveforms. In a Sepic converter the two inductor voltages are equal, both in CICM and DICM operation, providing that the voltage across capacitor C_1 follows rectified voltage $u_g(\theta)$ with a negligible high-frequency ripple. The equivalent circuit model of a two-winding coupled-inductor structure is shown in Fig.4.



$$L_M = \frac{N_1}{N_2} \cdot L_\mu$$

$$L_1 = L_{d1} + \left(\frac{N_1}{N_2}\right)^2 \cdot L_\mu$$

$$L_2 = L_{d2} + L_\mu$$

Fig.4 - Coupled-inductor equivalent circuit

Due to converter operation, the same voltage v is applied to both windings. Accordingly, zero ripple condition of primary current is easily derived by observing that secondary leakage inductance L_{d2} and magnetizing inductance L_μ form an inductive divider which scales the voltage applied to the secondary winding without altering its shape (voltage V_2 in Fig.4). If turn ratio N_1/N_2 is chosen to step-up the voltage V_2 to the original value v, zero current ripple on the primary side is obtained. Thus, the zero ripple condition is [9,10]:

$$\frac{N_2}{N_1} = \frac{L_\mu}{L_\mu + L_{d2}} = k_r \qquad (14)$$

where k_r is defined as secondary coupling coefficient. The input current ripple does not simply disappear, but it is "steered" into the other winding.

We can obtain the same result starting from the mutual inductor equations: assuming the same voltage applied on both windings, we can derive the rate of change of the currents in the two windings:

$$\frac{di_1}{dt} = \frac{v}{L_{1eq}}, \frac{di_2}{dt} = \frac{v}{L_{2eq}}$$

where,

$$L_{1eq} = L_1 \cdot \frac{1-\frac{L_M^2}{L_1 L_2}}{1-\frac{L_M}{L_2}}, L_{2eq} = L_2 \cdot \frac{1-\frac{L_M^2}{L_1 L_2}}{1-\frac{L_M}{L_1}} \quad (15)$$

From these expressions, it is seen that, to obtain zero ripple current in the input winding, the equivalent input inductance L_{1eq} must be infinity, which is accomplished by selecting $L_2=L_M$. With this choice, we obtain also $L_{2eq}=L_2$. Using the relations reported in Fig.4, it is easily verified that this zero ripple condition is equivalent to the previous one (14).

SENSITIVITY OF ZERO RIPPLE CONDITION

From the previous analysis, we can recognize that the zero ripple condition is independent of leakage inductance L_{d1} on the primary side. In practice, two main causes contribute to a non-zero ripple in the input inductance current [10]:

1) *Zero ripple condition mismatch*. In practical design, zero ripple condition (14) cannot be achieved due to integer number of turns and difficulty to set the gap thickness to the exact value required. This situation comes from nonidealities in the coupled inductors themselves and does not depend on the remaining part of the converter.

2) *Applied voltage mismatch*. This problem arises from the fact that a real converter does not apply the same voltage to both inductor windings. These differences may come from non-zero voltage ripple on capacitors, DC voltage drop on inductors, switching noise and so on. The consequent current ripple depends only on the converter design and is independent of coupled-inductor parameters. For example, in usual dc/dc applications, the capacitor voltage ripples can be reduced by increasing capacitor values. However, in the case of high-quality ac/dc rectification, there are limitations on capacitor sizes due to possible distortion of the input current.

In order to quantify the residual current ripple, the equivalent circuit shown in Fig.4 can be simplified as shown in Fig.5, in which different voltages applied to the two windings are considered. The rate of change of current i_1 is given by:

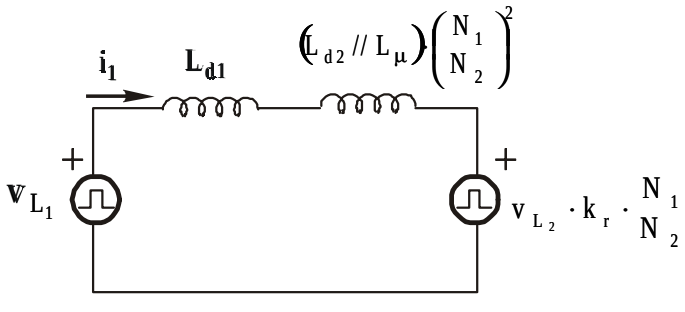


Fig.5 - Coupled-inductor equivalent circuit reported to primary side

$$\frac{di_1}{dt} = \frac{\left(v_{L_1} - k_r \frac{N_1}{N_2} v_{L_2}\right)}{L'} = \left(\underbrace{\left(v_{L_1} - v_{L_2}\right)}_{\text{Applied voltage mismatch}} + \underbrace{v_{L_2} \cdot \left(1 - k_r \frac{N_1}{N_2}\right)}_{\text{Zero ripple condition mismatch}} \right) \cdot \frac{1}{L'} \quad (16)$$

where

$$L' = L_{d1} + \frac{L_{d2} \cdot L_\mu}{L_{d2} + L_\mu} \cdot \left(\frac{N_1}{N_2}\right)^2 \cong L_{d1} + L_{d2} \cdot \frac{N_1}{N_2} \quad (17)$$

In the last term of (17), zero ripple condition (14) has been used. Equations (16) and (17) highlight the need of a high-leakage structure in order to have high values of L_{d1} and L_{d2}. Moreover, high leakage means low coupling coefficient k_r and, consequently, high turns ratio to meet condition (14), thus further increasing the value of L'.

POWER STAGE DESIGN

The power stage design criteria are similar to those of a normal Sepic converter used as a power factor preregulator without magnetic coupling and working in DICM, the only difference being the value of inductances L_1 and L_2 which are equal to L_{1eq} and L_{2eq} respectively. Input data are:

- minimum and maximum input voltage peak value U_{gmin}, U_{gmax};
- output voltage U_o;
- output power P_o;
- switching frequency f_s;
- expected converter efficiency η;
- initial value for transformer turns ratio n.

The design procedure is as follows:

1) calculate minimum and maximum voltage conversion ratio M_{min}, M_{max} from (6);
2) evaluate the second term of (11) for $\theta=\pi/2$ and M_{max};
3) choose the value of parameter K_a suitably lower than the value found in step 2 (for instance 10-20% lower);
4) find the value of inductance L_e, which coincides with L_2 if zero ripple condition is satisfied;
5) calculate device current and voltage stresses as well as peak inductor currents;
6) repeat the procedure for different values of transformer turns ratio;
7) choose the solution which best meets device ratings.

Particular attention must be given to the selection of capacitor C_1. Three constrains must be taken into account: first, voltage u_1 must follow the input voltage shape without distorsion; second, its voltage ripple must be as low as possible; third C_1 should not cause low-frequency oscillations with inductors L_1 and L_2. The former constrains arise from the need to have the same voltage waveform applied to L_1 and L_2, to reduce the *applied voltage mismatch* problem, while the latter avoids input current distortion. Clearly the requirement of low voltage ripple, which calls for a big capacitor, is in contrast with the others, and a trade-off must be done. In practice, the higher capacitor value which causes limited input current distortion or oscillations must be chosen. Simulation can be employed for the best choice.

Lastly, the output capacitor value is selected to achieve the desired 100 Hz voltage ripple.

MAGNETIC STRUCTURE DESIGN CONSIDERATIONS

As reported in [9-10], the magnetic structure could be a simple U-I or U-U core with a winding on each leg, as shown in Fig.6. In this case, we rely on the inherent leakage reluctance of the core, which has been demonstrated to be relatively independent of air-gap size and number of turns. Thus, for a given core, a "leakage parameter ℓ" can be introduced which greatly simplify the design. This parameter is defined as:

$$\ell = \mu_0 S R_\ell$$

where R_ℓ is the core leakage reluctance and S is the core section. But, from the considerations done with regard to the sensitivity of

zero ripple condition and in particular for the *applied voltage mismatch* problem related to the value of capacitor C_1, it seems more convenient to use an E-I or E-E core to increase the leakage inductances. The corresponding magnetic structure, is shown in Fig.7, together with its reluctance model. In the following we will assume that the magnetic core has already been chosen and its leakage parameter measured. Moreover, from the power stage design, the maximum current I_1 and I_2 in the two windings are known.

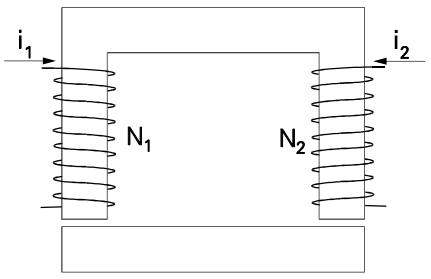


Fig.6 - Coupled-inductor on U-I core

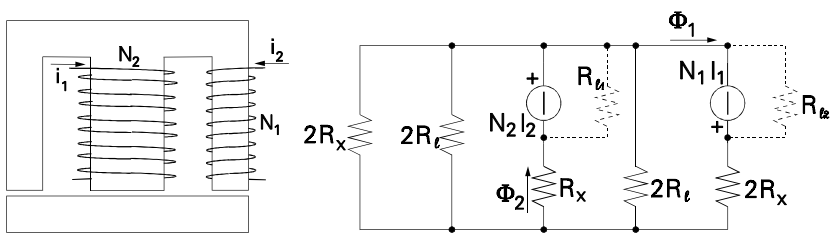


Fig.7 - Coupled-inductor on E-I core

Design specifications are as follows:

1) zero current ripple condition (14) must be satisfied;
2) inductance L_2 must have the desired value imposed by the power stage design (i.e. DICM operation);
3) core saturation must be avoided.

From the core reluctance model, the above constrains are easily expressed in terms of number of turns N_1 and N_2 and gap size x. In particular, from Fig.7b we derive:

$$\frac{N_2}{N_1}=\frac{R_\ell \,//\, 2R_x}{2R_x + R_\ell \,//\, 2R_x}=\frac{1}{2}\cdot\frac{\ell}{\ell+x}, \qquad R_x=\frac{x}{\mu_0 S} \tag{18}$$

$$L_2=\frac{N_2^2}{R_x + R_x \,//\, R_\ell}=\frac{N_2^2}{R_x}\cdot\frac{\ell+x}{2\ell+x} \tag{19}$$

$$\begin{cases}\Phi_2=\dfrac{N_2 I_2}{R_x + R_\ell \,//\, R_x}+\dfrac{N_1 I_1}{2R_x + R_\ell \,//\, \frac{2}{3}R_x}\cdot\dfrac{R_\ell \,//\, 2R_x}{R_x + R_\ell \,//\, 2R_x}\\ \Phi_1=\dfrac{N_2 I_2}{R_x + R_\ell \,//\, R_x}\cdot\dfrac{R_\ell \,//\, 2R_x}{2R_x + R_\ell \,//\, 2R_x}+\dfrac{N_1 I_1}{2R_x + R_\ell \,//\, \frac{2}{3}R_x}\end{cases} \tag{20.a}$$

$$\begin{cases}\Phi_2=\dfrac{L_2}{N_2}\cdot(I_1+I_2)\le S\cdot B_M\\ \Phi_1=\dfrac{L_2}{2N_2}\cdot\left(I_1\cdot\dfrac{3\ell+2x}{\ell}+I_2\cdot\dfrac{\ell}{\ell+x}\right)\le\dfrac{S\cdot B_M}{2}\end{cases} \tag{20.b}$$

where B_M is the maximum induction allowed in the core. Only one of (20.b) can be taken as equality; in particular, a simple solution in closed form can be obtained if:

$$\frac{I_2}{I_1}>2\frac{(\ell+x)^2}{x\ell} \tag{21}$$

which means that $\Phi_2>2\Phi_1$ and the central leg saturates first. In this case the solution is:

$$N_2=\frac{L_2}{B_M S}\cdot(I_1+I_2) \tag{22}$$

$$x=-\left(\ell-\frac{\mu_0 S N_2^2}{2L_2}\right)+\sqrt{\ell^2+\left(\frac{\mu_0 S N_2^2}{2L_2}\right)^2} \tag{23}$$

$$N_1=2\frac{\ell+x}{\ell}\cdot N_2 \tag{24}$$

If condition (21) is not satisfied no closed form solution can be obtained. For the design procedure in this case and for an estimation of the core cross section refer to [10].

CONTROL SECTION DESIGN

Due to the input power fluctuation, which causes an output voltage ripple at a frequency double than the line frequency, the bandwidth of the voltage loop must be limited to a value properly lower than the line frequency, in order to avoid input current distorsion. Thus the simple small-signal model derived in [11] can be used, which shows that a PI controller is sufficient.

EXPERIMENTAL RESULTS

In order to test the actual converter performances, two prototypes were built with different magnetic cores: one U-U and the other E-E core type. The converter parameters are listed in Table I. A capacitor C_f was used at the bridge rectifier output in order to filter the high frequency content of the input inductor current. The high frequency switch current and voltage waveforms, taken at nominal input voltage and rated power, are shown in Fig.8. The DICM operation is evident from both the ramp current waveform (which means zero-current turn on), and the oscillations at the end of the turn-off interval. These latter are caused by the resonance between inductance L_2 and switch parasitic capacitance C_{DS} when the freewheeling diode stops to conduct. Instead, the high frequency oscillations present at switch turn off, are caused by the transformer leakage inductance and the switch parasitic capacitance. Dispite the conservative design intended to limit the switch voltage stress in order to use 500V low resistance mosfets, these oscillations imposed the use of a 800V mosfet in order to avoid a too heavy snubber, with consequent decrease of converter efficiency. This choice, of course, implies a trade-off between switch and snubber losses.

The rectified input voltage and filtered input current for the prototype with E-E core at nominal conditions are shown in Fig.9. As we can see, the input current follows quite well the input voltage shape with low-frequency oscillations superimposed on it. These latter, and the phase shift of the current with respect to the voltage, are strongly influenced by the value of capacitor C_1. For the sake of comparison, the filtered input current waveform in correspondence of different values of capacitor C_1 are reported in Fig.10: the worsening at higher values is evident. This fact represents a big difference as compared to dc/dc applications, in which C_1 can be chosen from ripple consideration only, and limits the effectiveness of magnetic coupling. In fact, with these values of capacitance, the voltage ripple across C_1 is not negligible, so increasing the residual input current high-frequency ripple (*applied voltage mismatch* problem) (16). From this point of view, E-E core showed better performance then U-U type, as expected, due to the higher leakage. Table II reports the variation of the residual input current ripple for different C_1 values for both prototypes.

Although the input current waveform looks not good, the power factor, at rated load, is close to unity (0.99), as revealed by the plots in Figs.11 and 12. It becomes worse at low output power and maximum line voltage.

As far as converter efficiency is concerned, Figs.13 and 14 report this parameter as a function of the output power for different

input line voltages: E-E core has an efficiency of 86% in rated conditions, showing an improvement of 4% respect to U-U core in the same conditions (82%).

Table I: Prototype parameters

U_g = 220 V_{rms} ± 20%	U_o = 36 V	P_o = 100W	f_s = 100 KHz
L_2 = 74 μH	C_1 = 0.68 μF	C_f=0.1 μF	C_2 = 10 mF
D=BYT30P400	S=IRFPE50	n = 0.5	

Table II: Residual input current ripple for different C_1 values

C_1 [μF]	Δ_{i1} [A] (U-U core)	Δ_{i1} [A] (E-E core)
0.22	0.4	0.14
0.68	0.13	0.045
2	0.1	0.03

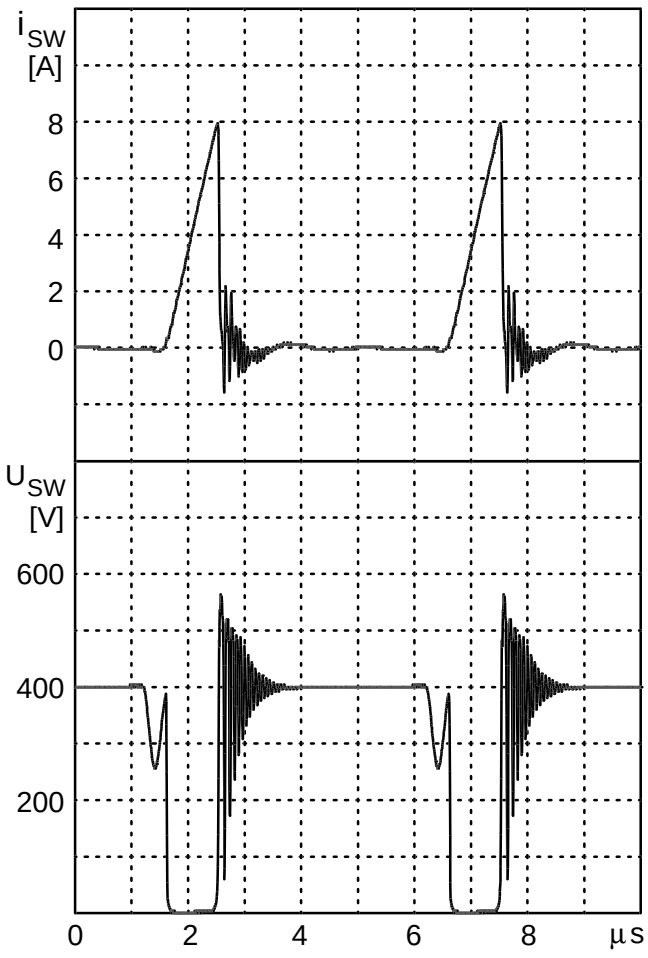


Fig.8 - High-frequency switch current and voltage waveforms (nominal conditions)

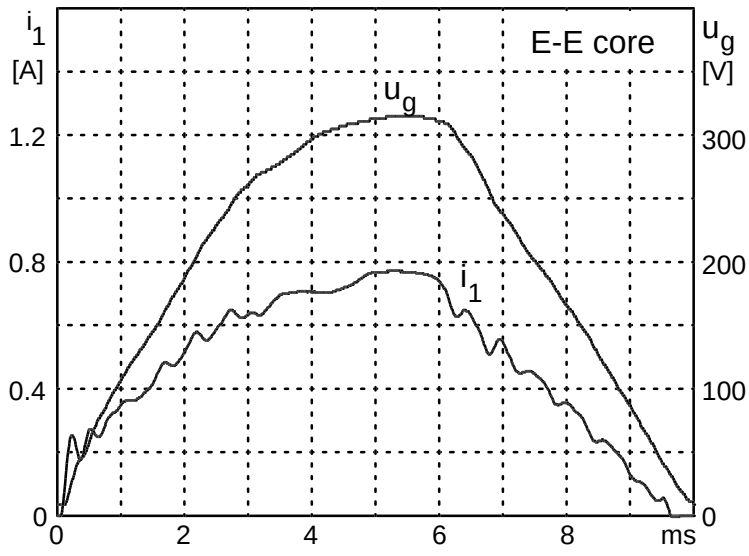


Fig.9 - Rectified input voltage and filtered input current (nominal conditions)

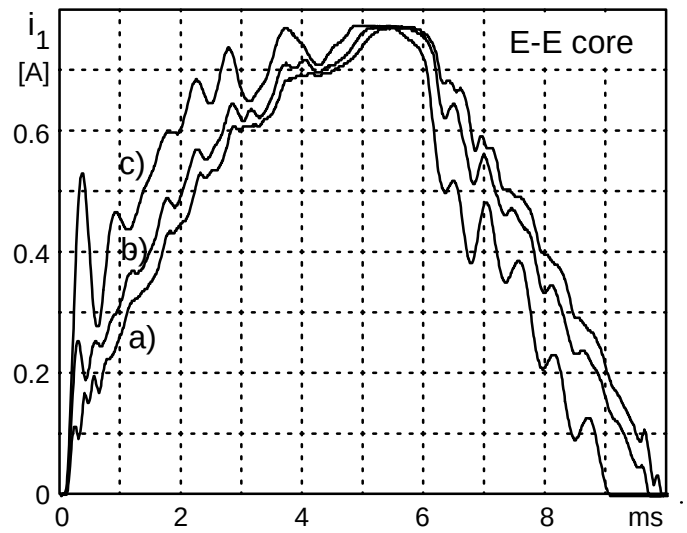


Fig.10 - Input current waveforms for different C_1 values (nominal conditions): a) 220nF, b) 680nF, c) 2uF

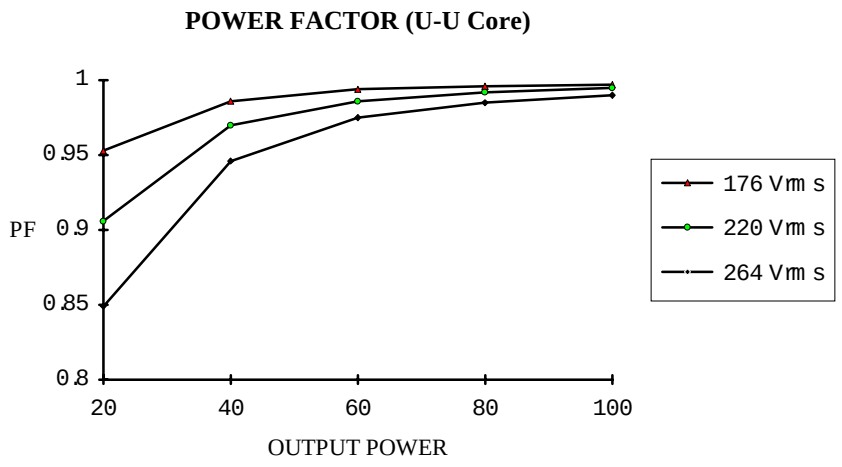


Fig.11 - Power factor vs. output power for different input voltages

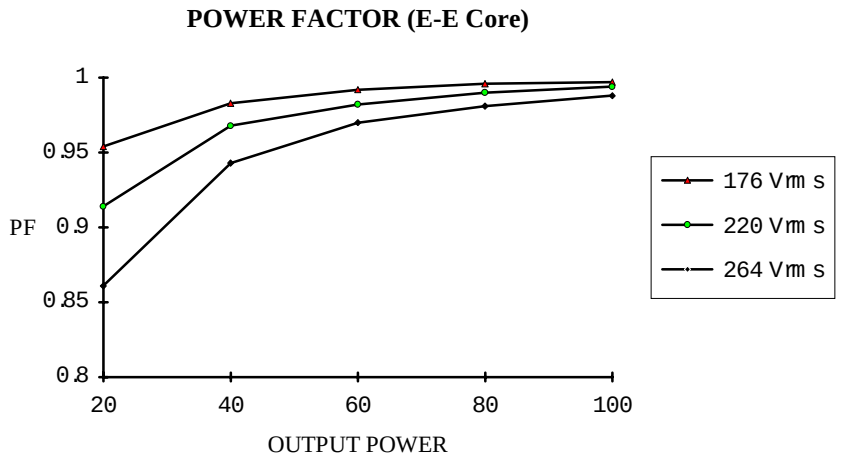


Fig.12 - Power factor vs. output power for different input voltages

Fig.13 - Converter efficiency vs. output power for different input voltages

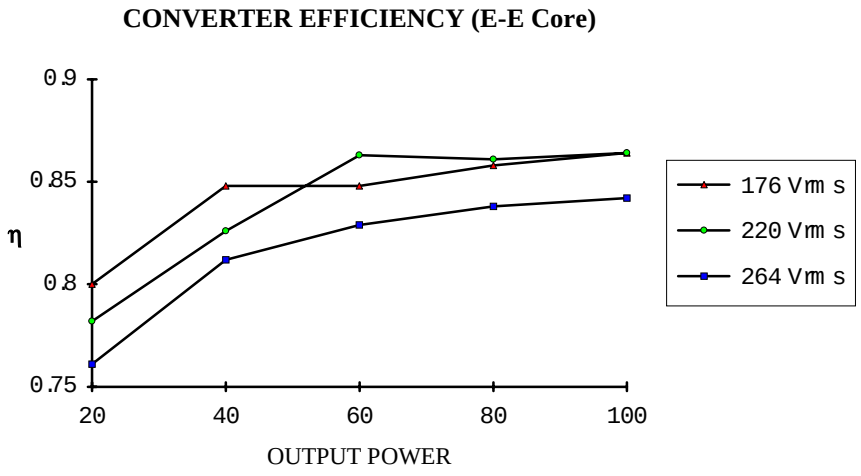


Fig.14 - Converter efficiency vs. output power for different input voltages

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CONCLUSIONS

In the paper, a high-quality rectifier employing a coupled-inductor Sepic stage is presented, featuring almost unity power factor with low input current ripple, high-frequency insulation, and simple PWM control. It is demonstrated that the coupled-inductor technique, when applied to ac/dc Sepic converters, allows low input current ripple with considerable size and cost reduction of the magnetic structure. Experimental tests on prototypes employing different magnetic cores are reported, which show the actual converter performances.

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