Appendix 1

A.1 Control Design of a Boost PFC Circuit

A.1.1 Controller Design

The controller design is based upon the procedures described in [25] [26]. The following sections give a brief description of the operation of each control loop.

A.1.1.1 Current Loop

The purpose of the current loop is to force the input current to follow a sinusoidal reference. Therefore the current loop bandwidth must be high enough to easily track the current reference signal and low enough to provide adequate phase and gain margin.

A.1.1.2 Voltage Loop

The voltage loop regulates the output voltage. If the voltage loop bandwidth were very high, then the output voltage would be constant but the input current would be distorted. Therefore the voltage loop bandwidth must be less than the line frequency. A larger 2nd harmonic voltage ripple is tolerated on the output thus allowing the current loop to regulate the input current more precisely.

A.1.1.3 Feedforward Network

The feedforward network is used to adjust the duty cycle to compensate for changes in the input line voltage. This is accomplished by supplying a DC signal proportional to the rms value of the line voltage. For this application, the feedforward network is not necessary.

A.1.2 Controller Design Example

The following equations and comments are used to provide an example controller design for a particular PFC boost circuit.

Control Design of PFC Converters

Design Specifications

Input AC Voltage	$Vi\_min := 180$ Vrms		$Vi\_max := 240$ Vrms
Output DC Voltage	$Vo := 354$ Vdc		
Output Power	$Po := 1150$ W		
Input Power	$Pin := \dfrac{Po}{0.9} \rightarrow 1277.7777777777777778$		
Switching Frequency	$fs := 40 \cdot 10^3$ Hz		
Line Frequency	$fl := 50$ Hz		

Given Power Stage Parameters

Capacitance of the drive	$Cdc := 920 \cdot 10^{-6}$
Boost Output Capacitance	$Cb := 68 \cdot 10^{-6}$
PFC Input Inductor	$L := 0.532 \cdot 10^{-3}$
Total Output Capacitor	$C := Cdc + Cb$
Minimum Output Capacitance	$C\_min := 680 \cdot 10^{-6} + 0.8 \cdot Cb$
Voltage Feedback Resistor	$R1 := 420 \cdot 10^3$
Current Sense Resistor	$Rs := 0.03$
External Ramp	$Vs := 5$
Control IC	$4981 A$

Magnitude and Phase Definitions

$$\text{gain}(X, s) := 20 \cdot \log(|X(s)|)$$

$$P(X, s) := \frac{180}{\pi} \cdot \text{angle}(\text{Re}(X(s)), \text{Im}(X(s)))$$

$$\text{phase}(X, s) := \text{if}(P(X, s) \geq 90, P(X, s) - 360, P(X, s))$$

$$\text{phase1}(X, s) := P(X, s) - 360$$

$$\text{ga}(X, y, s) := 20 \cdot \log(|X(y, s)|)$$

$$P(X, y, s) := \frac{180}{\pi} \cdot \text{angle}(\text{Re}(X(y, s)), \text{Im}(X(y, s)))$$

$$\text{ph}(X, y, s) := \text{if}(P(X, y, s) \geq 90, P(X, y, s) - 360, P(X, y, s))$$

$$\text{ph1}(X, y, s) := P(X, y, s) - 360$$

$$n := 0, 1 .. 600 \qquad f_n := 1 \cdot 10^{\frac{n}{100}} \qquad ff_n := 0.1 \cdot 10^{\frac{n}{100}}$$

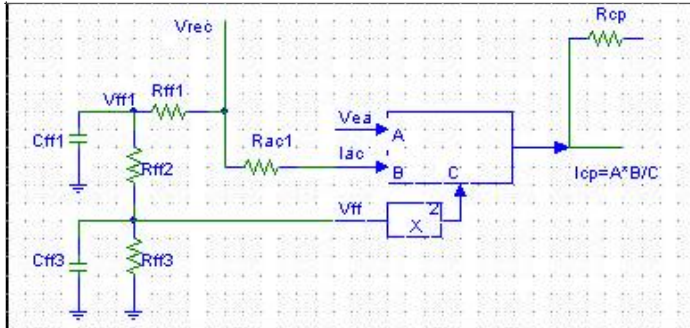***Step 1 Multiplier Setup and the Feedforward Loop Design***

Fig 1 the Multiplier circuit in 4981

(1) Rac1 design

From the Date sheet of 4981, the port of Iac is to sense the rectified voltage and force the inductor current to follow the voltage.

$Iac\_max := 600 \cdot 10^{-6}$ A

the best working condition is $\quad Iac := 300 \cdot 10^{-6}$ A

So

$$Rac1\_min := \frac{Vi\_max\sqrt{2}}{Iac\_max} \qquad Rac1\_min = 5.657 \cdot 10^{5}$$

SELECT $\qquad Rac1 := 10 \cdot 10^{5}$

(2) Feedforward voltage set

From the Data sheet of 4981, there is a relationship of the multipler input and output:

$$Icp = \frac{Iac \cdot (Vea - 1.28)}{Vff^{2}}$$

$Icp \leq 2 \cdot Iac$

$1.4 \text{ V} \leq Vff \leq 4.5 \text{ V}$

$Vea \leq 8.5 \text{ V}$

Normally set Vea=5.1V as the full-load voltage EA output, which means that we still have about 60% overload power limit.

When input voltage is the lowest, Iac is the lowest and Im will reach twice Iac, the EA output will be the maximum. So, we can get the minumun feedforward voltage requirement:

$Vea\_max := 8.5$

$Vea\_min := 0 \qquad Vff\_min := \sqrt{\dfrac{|Vea\_max - 1.28|}{2}}$

$\qquad Vff\_min = 1.9$

In this condition $\quad Vff\_max := Vff\_min \dfrac{Vi\_max}{Vi\_min} \qquad Vff\_max = 2.533$

Thus the design is in the range of 4981 working specifications.

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(3) Feedforward loop design

(a) design resistors to get the desired feedforward DC voltage

From Fig 1, we have following relationship:

$$Vff1 = 0.9 \cdot Vi \cdot \frac{Rff2 + Rff3}{Rff1 + Rff2 + Rff3}$$

$$Vff2 = 0.9 \cdot Vi \cdot \frac{Rff3}{Rff1 + Rff2 + Rff3} = Vff1 \cdot \frac{Rff3}{Rff2 + Rff3}$$

There are two voltage dividers. Define:

$$K1 = \frac{Vff1}{0.9 \cdot Vi} \qquad\qquad K2 = \frac{Vff}{Vff1}$$

Set K1=K2, we know:

$$Vff1 := \sqrt{\frac{0.9 \cdot Vi\_min}{Vff\_min}} \qquad\qquad Vff1 = 9.234$$

SELECT $\qquad Rff3 := 47 \cdot 10^3$

Given $\qquad Vff1 = 0.9 \cdot Vi\_min \cdot \dfrac{Rff2 + Rff3}{Rff1 + Rff2 + Rff3} \qquad\qquad Vff\_min = Vff1 \cdot \dfrac{Rff3}{Rff2 + Rff3}$

$$\text{Find}(Rff1, Rff2) \rightarrow \begin{bmatrix} 3778953.2405620946409 \\ 181415.18049053693809 \end{bmatrix}$$

SELECT $\qquad Rff1 := 3.9 \cdot 10^6 \qquad Rff2 := 180 \cdot 10^3$

(b) design capacitors to attenuate the 2rd harmonic

Normally, the second harmonic ripple of the rectified voltage is 66.2% of the input AC line voltage, which is the input of the devider.

DESIGN the total harmonic distoration of Vff is less than 1%

So, the required attenuation is:

$$Gff := \frac{1}{66.2} \qquad\qquad Gff = 0.015$$

the filter is a second order filter. To get the widest bandwith, set the two poles at the same place and set the gain of each order filter as the same. So the cutoff frequency of each filter is:

$$fc := \sqrt{Gff \cdot 100} \qquad\qquad fc = 12.291$$

So, we can get Cff1 and Cff3 as follows:

$$Cff1 := \frac{1}{2 \cdot \pi \cdot fc \cdot Rff2} \qquad Cff1 = 7.194 \cdot 10^{-8} \qquad Cff3 := \frac{1}{2 \cdot \pi \cdot fc \cdot Rff3} \qquad Cff3 = 2.755 \cdot 10^{-7}$$

SELECT $\qquad Cff1 := 82 \cdot 10^{-9} \qquad\qquad Cff3 := 0.33 \cdot 10^{-6}$

(c) Get the transfer function and bode plot of the feedforward loop $\quad Gff = \dfrac{vff}{vrec}$

From Fig 1, we konw

$$Kff := \frac{Rff3}{Rff1 + Rff2 + Rff3}$$

$$Wff := \sqrt{\frac{1}{Rff2 \cdot Cff1 \cdot Rff3 \cdot Cff3}} \qquad Fff := \frac{Wff}{2 \cdot \pi} \qquad Fff = 10.519$$

$$Qff := \frac{1}{Wff \cdot ((Rff2 + Rff3) \cdot Cff1 + Rff3 \cdot Cff3)} \qquad Qff = 0.443$$

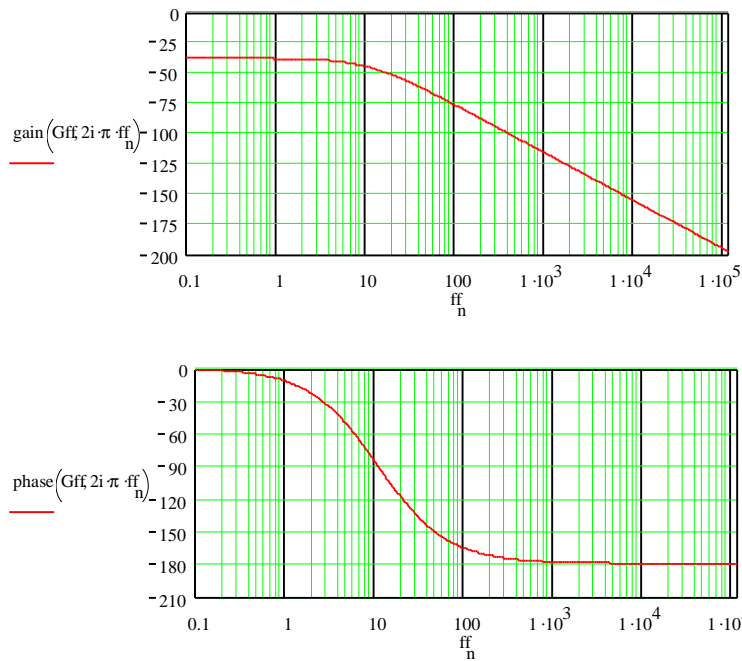$$Gff(s) := \frac{Kff}{1 + \dfrac{s}{Qff \cdot Wff} + \dfrac{s^2}{Wff^2}}$$

Fig 2 the Bode Plot of feedforward loop

$gain\_100 := gain(Gff, 2i \cdot \pi \cdot 100) \qquad\qquad gain\_0 := gain(Gff, 2i \cdot \pi \cdot 0)$

$gain\_0 = -38.871$

$Vff\_100 := 66.2 \cdot 10^{\frac{gain\_100 - gain\_0}{20}} \qquad Vff\_100 = 0.72$

We can see, the designed filter can attenuate the 2nd ripple to 1% requirement. It satisfies the design requirement.

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(4) Rcp design

Since Icp is the current reference, and the voltage across Rs is the sensed inductor current information, so it is required:

$$Rcp \cdot Icp = IL \cdot Rs$$

In the condition when Vi is lowest, and assume the PFC efficiency is 90%

$$IL := \frac{Pin}{Vi\_min}$$

$$Iac := \frac{Vi\_min\sqrt{2}}{Rac1}$$

$$Icp := 2 \cdot Iac$$

$$Rcp := \frac{IL \cdot Rs}{Icp} \qquad Rcp = 418.299$$

SELECT $\qquad Rcp := 420$

Current Loop Compensator Design Procedure

The current loop must be compensated for stable operation. The boost converter control to input current transfer function has a single pole response at high frequencies which is due to the impedance of the boost inductor and the sensing resistor (Rs). The equation is:

$$Gc = \frac{vrs}{vcea} = Vo \cdot \frac{Rs}{Vs \cdot (sL)}$$

where Vo is the boost output voltage
Rs is the sensing resistance
Vs is the peak to peak voltage of the oscillator ramp
L is boost inductance

This equation is only valid for frequencies above the resonant frequency of the boost inductor and capacitor and below the switching frequency. For frequencies below the LC resonance the equation is different.

A zero at low frequency in the current amp response is used to give high gain which makes current mode control work. The gain of the current amp near the switching frequency is determined by matching the down slope of the inductor current when the switch is off with the slope of the oscillator ramp. These two signals are the inputs to the comparator in the L4981A.

The down slope of the inductor current current is maximum when the input voltage is zero. At this point (Vin=0) the inductor current is given by the ratio of the output voltage and the inductance (Vo/L). The current flows through the sensing resistor and produces a voltage with slope = VoRs/L. This slope multiplied by the gain of the current error amplifier must be equal to the slope of the oscillator ramp. If the gain is too high, then the slope of the inductor current would be greater than the ramp and the loop could go unstable. This instability would be greatest at the zero crossing of the input voltage.

The gain of the current amp near the cross-over frequency is simply :

$$Gcea = 1 + \frac{Rz}{Ri}$$ current amp gain

The current loop gain is simply Gcea*Gc

$$Gloop = \frac{Vo \cdot Rs \cdot Rz}{Vs \cdot 2 \cdot \pi \cdot f \cdot L \cdot Ri} + \frac{Vo \cdot Rs}{Vs \cdot 2 \cdot \pi \cdot f \cdot L}$$

The slope of the voltage across the sensing resistor is given by:

$$Cslope := Vo \cdot \frac{Rs}{L \cdot 10^6}$$

$$Cslope = 0.02$$ volts per microsecond

The slope of the oscilllator in the L4981A at 40kHz is given by

$$\text{Oslope} := \text{Vs} \cdot \frac{\text{fs}}{10^6}$$

$$\text{Oslope} = 0.2 \qquad \text{volts per microsecond}$$

Therefore the current amp must have a gain of: $\dfrac{\text{Oslope}}{\text{Cslope}} = 10.019$ at the switching frequency.

thus $\qquad \text{Gcea} := \dfrac{\text{Oslope}}{\text{Cslope}}$

Let $\qquad \text{Ri} := 10 \cdot 10^3$

therefore $\qquad \text{Rz} := \text{Gcea} \cdot \text{Ri} - 1 \qquad \text{Rz} = 1.002 \cdot 10^5$

SELECT $\qquad \text{Rz} := 0.91 \cdot 10^5$

Now the loop gain (Gloop) is set to one and thus the cross-over frequency can be found.

$$\text{fic} := \frac{\text{Vo} \cdot \text{Rs} \cdot \left(1 + \dfrac{\text{Rz}}{\text{Ri}}\right)}{\text{Vs} \cdot 2 \cdot \pi \cdot \text{L}}$$

$$\text{fic} = 6.418 \cdot 10^3$$

The placement of the zero in the current loop response must be at or below the cross-over frequency. If the zero is at fic then the phase margin would be 45 degrees. If the zero is below fic then the phase margin would be slightly more than 45 degrees. To place the zero directly at the cross-over frequency the impedance of Ccz at that frequency must be equal to Rcz. Thus the equation is:

$$\text{Cz} := \frac{1}{2 \cdot \pi \cdot \text{fic} \cdot \text{Rz}}$$

$$\text{Cz} = 2.725 \cdot 10^{-10}$$

SELECT $\qquad \text{Cz} := 220 \cdot 10^{-12}$

The selected value is clearly too low. This places the zero after the cross-over frequency thus our phase margin is less than 45 degrees. This is probably due to the fact that the value for Cz was chosen for the 100kHz prototype which had a different boost inductance.

A pole is normally added to the current error amplifier response near the switching frequency to reduce noise sensitivity. The best place for the pole is at half the switching frequency. In this way the pole does not affect the current loop response and it provides good attenuation at the switching frequency. However the pole should be at least one decade after the zero otherwise the phase margin would be greatly reduced.

$$fz := \frac{1}{2 \cdot \pi \cdot Rz \cdot Cz}$$

$$fz = 7.95 \cdot 10^3 \qquad \text{frequency of the zero}$$

$$fp = \frac{(Ccp + Cz)}{Ccp \cdot Cz \cdot Rz \cdot 2 \cdot \pi} \qquad \text{frequency of the pole}$$

sloving for Ccp

$$Ccp(fp) := \frac{Cz}{2 \cdot \frac{\pi \cdot fp}{2} \cdot Rz \cdot Cz - 1}$$

$$Ccp(10 \cdot fz) = 5.5 \cdot 10^{-11}$$

$$fp := \frac{(Ccp(10 \cdot fz) + Cz)}{Ccp(10 \cdot fz) \cdot Cz \cdot Rz \cdot 2 \cdot \pi}$$

$$fp = 3.975 \cdot 10^4 \qquad$$ In our case the switching frequency is too low for this technique to be effective.
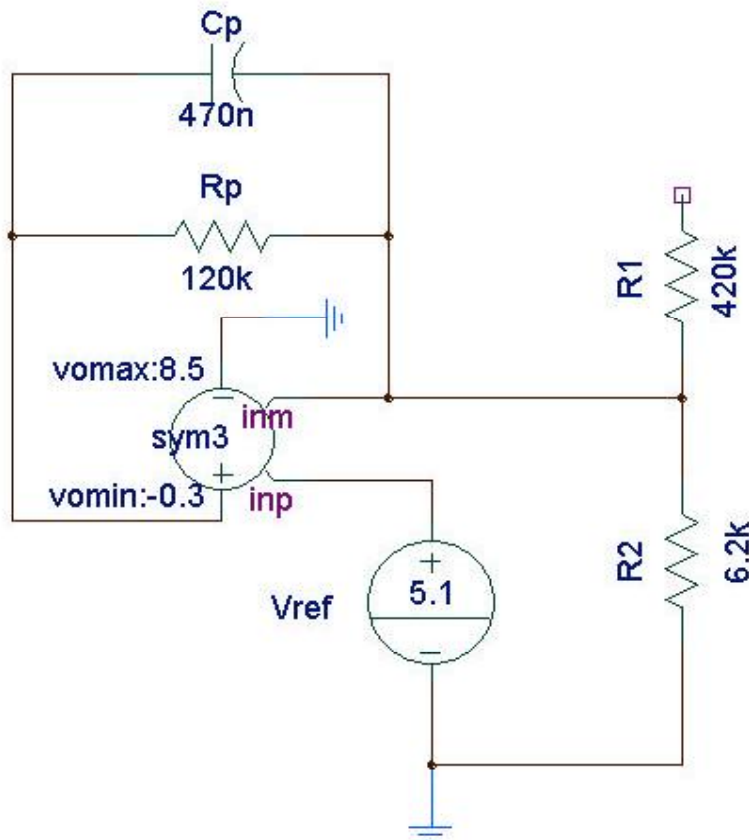
SELECT $\qquad CCp := 0$

Figure 11: Voltage compensation network

Voltage Loop Compensator Design:

The voltage loop must be compensated for stability but because the bandwidth of the voltage loop is so much lower than the switching frequency the requirements for the voltage compensation are mainly driven by the need to reduce the input distortion.

A pole in the amplifier is needed to reduce the amplitude of the second harmonic and to shift the phase by 90 degrees.

The choice of R1 is somewhat vague. It is selected to be small enough so that the amplifier bias current does not affect the output but R1 must be large enough to avoid too much power dissipation. In our case:

$$R1 = 4.2 \cdot 10^5$$

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Control Design of a Boost PFC Circuit

Note that R2 has no effect on the small signal gain because the potential across R2 is fixed to Vref. The error amp small signal gain can be seen as the ratio between the error amp output ripple and the imposed output voltage ripple of the boost. The error amp output voltage can swing between 1.28 and 5.1V. A value less than 2.5% of the error amp swing voltage can be chosen to fix the value of Cp. So the desired gain at the output voltage ripple frequency determines the value of Cp. This will ensure proper attenuation at 100Hz (2*fl).

$$\text{Gea}(s) = \frac{1}{s \cdot R1 \cdot Cp} = \frac{vea}{vo}$$ error amp small signal gain

$$\Delta Vvea := 5.1 - 1.28$$ The error amp voltage swing

$$\text{ripple} := 0.025 \cdot \Delta Vvea$$ The amount of output ripple we will tolerate

$$Vopk := \frac{Pin}{2 \cdot fl \cdot \pi \cdot C\_min \cdot Vo}$$ the output voltage ripple

$$Vopk = 15.645$$ The peak to peak ripple would be twice this value.

$$\text{Gea} := \frac{\text{ripple}}{Vopk}$$ desired gain at 2*fl based on 2.5% distortion.

$$Cp := \frac{1}{2 \cdot \pi \cdot 2 \cdot fl \cdot R1 \cdot Gea}$$ Cp is selected to acheive the desired gain at 2*fl

$$Cp = 6.208 \cdot 10^{-7}$$

SELECT $$Cp := 470 \cdot 10^{-9}$$

$$Xcp(fvc) := \frac{1}{2 \cdot fvc \cdot Cp}$$ impedance of Cp

$$Xc(fvc) := \frac{1}{2 \cdot fvc \cdot C}$$ impedance of output capacitor

This is slightly smaller than the theoretical value however there is no noticable 100Hz ripple in the control signals on the prototype.

The system must be able to compensate the total external load variation through the error amp output response ($\Delta Vvea$). The power gain transfer function (Gpw) can be written as:

$$Gpw = Io \cdot \frac{Xc}{\Delta Vvea}$$ where Io is the load current and Xc is the output capacitor impedance.

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The total load variation can be considered as:

$$Gpw(fvc) := \frac{(Po \cdot Xc(fvc))}{Vo \cdot \Delta Vvea}$$

The gain of the voltage loop is the product of Gpw and Gea

$$Gloop(fvc) := \frac{(Pin \cdot Xc(fvc) \cdot Xcp(fvc))}{\Delta Vvea \cdot Vo \cdot R1}$$

Note that this transfer function contains two poles at the origin 1/sC and 1/sCp. This could cause a stability problem. To avoid this a resistor (Rp) is added in parallel with Cp to move the voltage compensator pole to 1/(sCpRp).

The cross-over frequency (fvc) can be calculated by setting Gloop =1 and solving for fvc.

$$fvc := \sqrt{\frac{Po}{Vo \cdot \Delta Vvea \cdot R1 \cdot C \cdot Cp \cdot (2 \cdot \pi)^2}}$$

$fvc = 10.51$ cross-over frequeuncy

to allow the highest DC gain while maintaining a phase margin of at least 22 degrees Rp is chosen as:

$$Rp := \frac{2.75}{2 \cdot \pi \cdot fvc \cdot Cp}$$

$Rp = 8.861 \cdot 10^4$

SELECT $Rp := 12 \cdot 10^4$

The output voltage is set by the voltage divider circuit created by R1 and R2. Since the value of R1 is already selected R2 is chosen to give the desired output voltage.

Guess $R2 := 10 \cdot 10^3$

Given $\frac{R2}{R1 + R2} = \frac{5.1}{Vo}$ $Find(R2) = 6.139 \cdot 10^3$

SELECT $R2 := 5.7 \cdot 10^3$

In practice it is best to determine R2 by adjusting the value manually until the desired bus voltage is obtained. The value of R2 has no effect on the ac characteristics of the voltage compensation network. R2 is only used to set the DC bus voltage.

Discussion of the design consideration and results

(1) about the feedforward loop design

The feedforward loop design is a trade-off between quick converter responsce and low current distortation. The crossover frequency can only designed high below 120Hz so the 2nd harmonic will have little influence to the current reference and the input current distortation will be small. We select a two stage filter to increase the respense time and achieve a high attenuation of 2nd harmonic.

Fig 2 shows the designed feedforward filter has about 18Hz crossover frequency, and the attenuation of 2nd harmonic is below 1.5%. It can satisfy the requiment.

(2) about the current loop design

The design is based upon an intuitive time domain analysis given in the Unitrode application note for the UC3854 PFC controller and the ST application not for the L4981A PFC controller.

(3) about the voltage loop design

The voltage loop design procedure is based upon an intuitive time domain analysis given in the Unitrode appication note for the UC3854 PFC controller and the ST application note for the L4981A PFC controller. This analysis is mainly based on suppression of the 100Hz ripple in the boost output voltage.

In the previous file a low frequency model of the boost stage is used to perform classical voltage loop compensation. However this low frequency model is not so clear because the output voltage, input voltage and current cannot be considered constants. Therefore it is theoretically impossible to linearize the system and have an accurate power stage model. This is always a difficulty when modelling any single phase PFC circuit.