SMALL-SIGNAL MODELING OF THE SINGLE-PHASE BOOST HIGH POWER FACTOR CONVERTER WITH CONSTANT FREQUENCY CONTROL

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Abstract: *A simple and accurate small-signal model, for the high power factor converter with constant switching frequency, is developed and verified. The model is applicable for all frequencies below half of the switching frequency. The model is useful in the design and analysis of the voltage and current loops, and of the input and the output impedances of the converter. The model use is demonstrated in the analysis and design of the power factor boost converter with average current control.*

INTRODUCTION

Recently there have been increasing demands for high power factor and low harmonic distortion in the current drawn from the utility. Among the commonly used are the boost derived topologies. Constant switching frequency average current control has the advantage of easier design of the EMI filters and better control of the average input current of the converter than the peak current control schemes. One of the commercially available average current controllers is the one shown in Fig.1 (UC3854). To design the average current control, the frequency response of the converter has to be modeled up to half of the switching frequency to achieve the maximum possible gain and bandwidth.

To derive the small-signal model for the HPF (high power factor) boost converter, two main problems have to be addressed : (1) the input of the converter is the rectified line voltage that varies in a wide range at twice the line frequency, (2) the controller is nonlinear because of the multiplier/divider function.

Several methods for modeling the HPF converters were introduced [1-11], mainly for peak current control schemes, and all of these works have the following limitations :

1) Models were derived for frequency range much lower than the line frequency, with the assumption of unity power factor. Under this assumption, the system was reduced to first order.
2) Models were derived for frequency range much higher than the line frequency, with the assumption of a constant voltage source at the output. Under this assumption, the system was reduced to first order.
3) Lack of a single small-signal model that is applicable to frequencies both lower and higher than the line frequency.
4) In [7-10] the quasi-static analysis approach was introduced. But the quasi-static approach is applicable if the dynamics of all the system variables are much faster than the line frequency. In most of the practical single-phase HPF boost converters the output voltage dynamics are much slower than the line frequency.

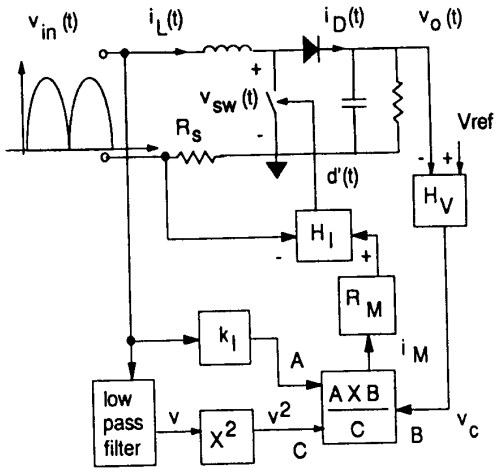

Fig.1: Boost HPF converter with average current control, H_v and H_i are the voltage and current compensators respectively.

In this paper, it is shown that the rectified input voltage can be replaced by its RMS value (DC voltage), and the small-signal dynamics of the obtained model is a good approximation of the small-signal dynamics of the HPF converter. Therefore the power stage can be treated as a DC-DC converter and modeled with the use of the PWM-Switch small-signal model [12] that is applicable to all the frequencies below half of the switching frequency. The average current controller shown in Fig.1 is analyzed, but the modeling approach, presented in this paper, can be applied to other HPF controllers. Moreover, the analysis and design of DC-DC converters with average current control, presented in [13], can be used to design the HPF boost current loop. The main assumption is that there is a large hold-up capacitor at the output of the converter, so that the line frequency ripple is very small compared to the DC level of the output (usually less than 5%). Unity power factor is not assumed, but HPF is, and the operation of the converter is restricted to CCM (continuous conduction mode) only. The model is derived for the HPF boost converter in CCM, but in a similar way the modeling approach can be extended to DCM (discontinuous conduction mode) boost, buck, or buck-boost converters.

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MODEL DERIVATION

The small-signal model is derived for the HPF boost described in Fig.1. The model is derived in two steps: (1) modeling of the power stage, (2) modeling of the controller.

Power Stage Modeling:

The boost converter switch is replaced by its average, over the switching frequency, large-signal model as shown in Fig.2. For CCM operation, we have:

$$v_{sw}(t) = d'(t)v_o(t), \tag{1}$$

$$i_D(t) = d'(t)i_L(t), \tag{2}$$

where $v_{sw}(t)$, $i_D(t)$, $d'(t)$, $i_L(t)$, and $v_o(t)$ are the large-signal averages of the switch voltage, diode current, the complementary duty-cycle, the inductor current, and the output voltage, respectively.

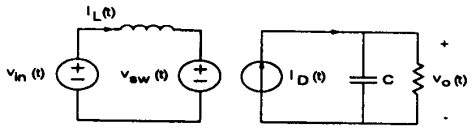

Fig.2: Large-signal average model of the boost power stage.

The power stage is modeled in two steps : (1) steady-state modeling, (2) perturbation analysis.

Step(1): Steady-state modeling: In the steady-state the output average power is equal to the input average power (over the line period, and ignoring the losses), so that, the DC operating point (Fig.3) is chosen to be as follows: V_o is the steady-state DC output voltage, V_{rms} and I_L are the RMS values of the input voltage and current, respectively, and D' = 1-D = V_{rms}/V_o, where D is the duty-cycle.

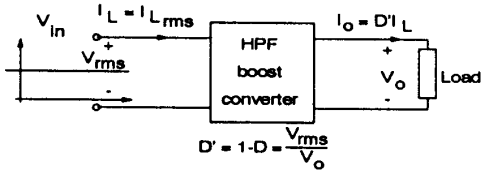

Fig.3: The operating point of the boost power stage.

The large-signal averaged variables of the system can be described as follows:

$$v_{sw}(t) = V_o + v_{or}(t), \tag{3.a}$$

$$i_{Ls}(t) = I_L + i_{Lr}(t), \tag{3.b}$$

$$d'_{ss}(t) = D' + d'_r(t), \tag{3.c}$$

$$v_{ins}(t) = V_{rms} + v_{inr}(t), \tag{3.d}$$

where the subscripts 'ss' and "r" denote the steady-state waveforms, and the AC quantities caused by the line ripple around the operating point defined in Fig.3, respectively.

First we prove that the converter can be approximated by a linear system in the steady-state.

Using equations (1-3), we obtain :

$$v_{swss}(t) = D'V_o + D'v_{or}(t) + d'_r(t)V_o +$$

$$+d'_r(t)v_{or}(t) = V_{sw} + v_{swr}(t), \tag{4}$$

$$i_{Dss}(t) = D'I_L + D'i_{Lr}(t) + d'_r(t)I_L +$$

$$+d'_r(t)i_{Lr}(t) = I_D + i_{Dr}(t). \tag{5}$$

Large capacitor is assumed so that $V_o >> v_{or}(t)$ and

$$v_{swr}(t) = D'v_{or}(t) + d'_r(t)V_o. \tag{6}$$

For the diode current, we have :

$$i_{Dr}(t) = D'i_{Lr}(t) + d'_r(t)I_L + d'_r(t)i_{Lr}(t). \tag{7}$$

In general, the product $d'_r(t)i_{Lr}(t)$ is at most 25% of $i_{Dss}(t)$ near the zeros and peaks of the line voltage as shown in Fig.4. The waveforms of 400 W, 220 VRMS, and 370 VDC output HPF boost are given in Fig.4; they represent typical waveforms in HPF boost converter. In the steady-state, $d'_r(t)$ and $i_{Lr}(t)$ are approximately rectified sine-waves and in-phase, so that the product term, $d'_r(t)i_{Lr}(t)$, is dominated by the even harmonics of twice of the line frequency and contributes a DC component to the diode current.

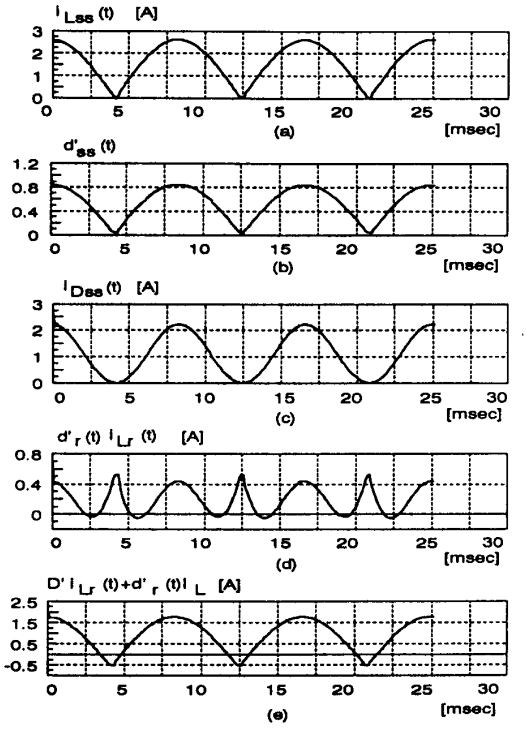

Fig.4: Steady-state waveforms of a boost HPF converter, (a) the inductor current, $i_{Lss}(t)$, (b) the complementary duty-cycle, $d'_{ss}(t)$, (c) the diode current, $i_{Dss}(t)$, (d) the non-linear part of the diode current, $d'_r(t)i_{Lr}(t)$, (e) the linear part of the diode current, $D'i_{Lr}(t)+d'_r(t)I_L$.

In Fig.5, the spectra of the diode current components are shown. The diode current is dominated by the DC and by the second harmonic of the line frequency, and the main contribution of the nonlinear term is the DC and fourth harmonic of the line; and fourth harmonic of the line is about 20% of the second harmonic. Under the assumption that there is a large output capacitor that filters the line harmonics, the significant component of $d'_r(t)i_{Lr}(t)$ is the DC current and the fourth harmonic term can be ignored, so equation (7) becomes:

$$i_{Dr}(t) = D'i_{Lr}(t) + d'_r(t)I_L + I_{dc}, \tag{8}$$

where I_{dc} is the average value of $d'_r(t)i_{Lr}(t)$. Using equations (3), (6), and (8), the linear steady-state model, described in Fig.6, is obtained.

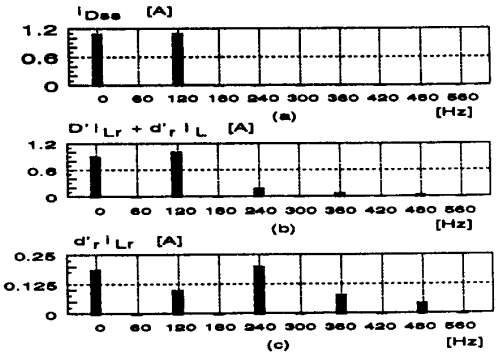

Fig.5: Spectra of the diode current components :(a) the diode current, (b) the linear part of the diode current, (c) the non-linear part of the diode current.

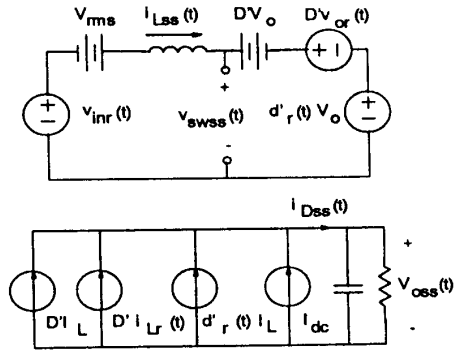

Fig.6: The steady-state linear time-invariant model of the HPF boost converter.

Step (2): Perturbation analysis : In the presence of a small-signal perturbation, the large-signal averaged variables of the system can be described as follows:

$$v_o(t) = V_o + v_{or}(t) + v_{op}(t), \tag{9.a}$$
$$i_L(t) = I_L + i_{Lr}(t) + i_{Lp}(t), \tag{9.b}$$
$$d'(t) = D' + d'_r(t) + d'_p(t), \tag{9.c}$$
$$v_{in}(t) = V_{rms} + v_{inr}(t) + v_{inp}(t), \tag{9.d}$$

where the subscript 'p' denotes the small-signal perturbations.

Assuming that

$$V_o \gg v_{or}(t) \gg v_{op}(t), \tag{10.a}$$
$$I_L \text{ and } i_{Lr}(t) \gg i_{Lp}(t), \tag{10.b}$$
$$D' \text{ and } d'_r(t) \gg d'_p(t), \tag{10.c}$$
$$V_{rms} \text{ and } v_{inr}(t) \gg v_{inp}(t), \tag{10.d}$$

and using equations (1-2), and (9-10), the switch voltage and the diode current can be approximated by :

$$v_{sw}(t) = D'V_o + D'v_{or}(t) + D'v_{op}(t) + \\ +d'_r(t)V_o + d'_r(t)v_{or}(t) + d'_p(t)V_o, \tag{11}$$

$$i_D(t) = D'I_L + D'i_{Lr}(t) + D'i_{Lp}(t) + \\ +d'_r(t)I_L + d'_r(t)i_{Lr}(t) + d'_p(t)I_L, \tag{12}$$

and using equations (4) and (5), we obtain:

$$v_{sw}(t) = v_{swss}(t) + D'v_{op}(t) + d'_p(t)V_o \\ = v_{swss}(t) + v_{swp}(t), \tag{13}$$

$$i_D(t) = i_{Dss}(t) + D'i_{Lp}(t) + d'_p(t)I_L \\ = i_{Dss}(t) + i_{Dp}(t), \tag{14}$$

where :

$$v_{swp}(t) = D'v_{op}(t) + d'_p(t)V_o, \tag{15}$$
$$i_{Dp}(t) = D'i_{Lp}(t) + d'_p(t)I_L. \tag{16}$$

It was proven, in equations (6) and (8), that the converter can be approximated by a linear system in the steady-state; therefore, equations (13) and (14) describe a linear system, and equations (15) and (16) describe the small-signal model of the converter, and the small-signal model equivalent circuit is the one shown in Fig.7. The small-signal model of the HPF boost converter in Fig.7 represents the small-signal model of a DC-DC boost converter around the operating point defined in Fig.3.

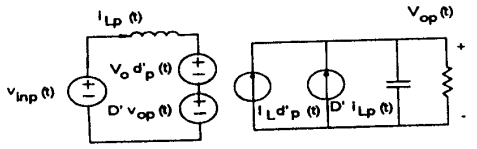

Fig.7: The small-signal model of the HPF boost converter.

The Controller Modeling:

The multiplier/divider, in Fig.1, is described by its large-signal model :

$$i_M(t) = \frac{k_i v_{in}(t) v_c(t)}{v^2(t)}, \quad (17)$$

where $v_{in}(t)$, $i_M(t)$, $v_c(t)$, and $v(t)$ are the large-signal input voltage, the multiplier/divider output current, the control voltage, and the output voltage of the low pass filter, respectively.

The controller is modeled in two steps : (1) steady-state modeling, (2) perturbation analysis.

Step(1): Steady-state modeling: The large-signal variables of the multiplier/divider can be described as follows:

$$v_{css}(t) = V_c + v_{cr}(t), \quad (18.a)$$
$$i_{Mss}(t) = I_M + i_{Mr}(t), \quad (18.b)$$
$$v_{ss}(t) = V + v_r(t), \quad (18.c)$$
$$v_{inss}(t) = V_{rms} + v_{inr}(t), \quad (18.d)$$

where the subscripts 'ss' and 'r' denote the steady-state waveforms and the variations caused by the variations of the rectified line voltage around its RMS value, respectively. It is important to notice that V_c, I_M and V are obtained by replacing the rectified line voltage by its RMS value.

Using equations (17-18), we obtain :

$$I_M V^2 + 2VI_M v_r + I_M v_r^2 + i_{Mr} V^2 + 2V i_{Mr} v_r +$$
$$+ i_{Mr} v_r^2 = k_i V_{rms} V_c + k_i V_{rms} v_{cr} +$$
$$+ k_i v_{inr} V_c + k_i v_{inr} v_{cr}. \quad (19)$$

To achieve high power factor, the bandwidth of the voltage loop and of the low pass filter are usually designed to be much lower than the line ripple frequency; therefore, it is assumed that the peak-to-peak values of : (1) $V >> v_r(t)$ and (2) $V_c >> v_{cr}(t)$, so that equation (19) can be approximated as:

$$I_M V^2 + 2VI_M v_r + i_{Mr} V^2 = k_i V_{rms} V_c +$$
$$+ k_i V_{rms} v_{cr}(t) + k_i v_{inr} V_c, \quad (20)$$

or :

$$I_M + i_{Mr}(t) = \frac{k_i V_{rms} V_c}{V^2} + \frac{k_i V_{rms} v_{cr}(t)}{V^2} +$$
$$+ \frac{k_i V_c v_{inr}(t)}{V^2} - \frac{2VI_M v_r(t)}{V^2} = i_{Mss}(t). \quad (21)$$

Equations (20-21) are a linear time-invariant steady-state model of the controller.

Step (2): Perturbation analysis : In the presence of a small-signal perturbation, the large-signal variables of the system can be described as follows:

$$v_c(t) = V_c + v_{cr}(t) + v_{cp}(t), \quad (22.a)$$
$$i_M(t) = I_M + i_{Mr}(t) + i_{Mp}(t), \quad (22.b)$$
$$v(t) = V + v_r(t) + v_p(t), \quad (22.c)$$
$$v_{in}(t) = V_{rms} + v_{inr}(t) + v_{inp}(t), \quad (22.d)$$

where the subscript 'p' denotes the small-signal perturbations.

Assuming that

$$V_c \gg v_{cr}(t) \gg v_{cp}(t), \quad (23.a)$$
$$I_M \text{ and } i_{Mr}(t) \gg i_{Mp}(t), \quad (23.b)$$
$$V_{rms} \text{ and } V_{inr}(t) \gg v_{inp}(t), \quad (23.c)$$
$$V \gg v_r(t) \gg v_p(t), \quad (23.d)$$

and using equations (17), (21-23), the output current of the multiplier/divider can be approximated by :

$$I_M + i_{Mr}(t) + i_{Mp}(t) = k_i[\, V_{rms} V_c + V_{rms}[\, v_{cr}(t) + v_{cp}(t) \,] +$$
$$+ V_c[v_{inr}(t) + v_{inp}(t)] - 2VI_M[\, v_r(t) + v_p(t) \,]\,] / V^2 =$$
$$= i_{Mss}(t) + i_{Mp}(t), \quad (24)$$

where :

$$i_{Mp}(t) = \frac{k_i V_{rms} v_{cp}(t)}{V^2} + \frac{k_i V_c v_{inp}(t)}{V^2} - 2\frac{I_M v_p(t)}{V}. \quad (25)$$

Equations (24-25) show that the controller model is a linear system around the operating point defined in Fig.3. The small-signal model is described by equation (25) and its equivalent circuit is shown in Fig.8, where :

$$g_{in} = \frac{k_i V_c}{V^2}, \quad g_c = \frac{k_i V_{rms}}{V^2}, \quad g_m = -2\frac{I_M}{V}.$$

The complete small-signal model of the HPF boost converter is obtained by replacing the PWM-switch and the multiplier/divider with their small-signal models in Fig.7 and Fig.8.

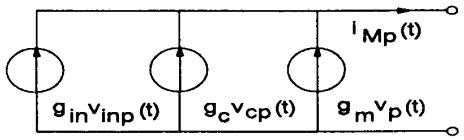

Fig.8: The small-signal model of the multiplier/divider.

ANALYSIS AND CONTROL DESIGN

The analysis and design is performed for the HPF boost converter with average current control, but in a similar way, the analysis can be carried out for other current control schemes. In this section, the small-signal duty-cycle-to-inductor current, the control voltage-to-inductor current, and the control voltage-to-output voltage transfer functions are derived, compared to previously proposed models, and used to design the current and the voltage compensation networks.

The complete small-signal model is described in Fig.9, where $H_e(s)$ is the sampling effect, and F_m is the PWM modulator gain such as were developed in [13]. As in DC-DC boost converter with resistive load:

$$\frac{v_{op}(s)}{v_{inp}(s)} = G_{vg}(s) = \frac{1}{D'} \frac{sCR_c + 1}{\Delta(s)}, \quad (26)$$

$$\frac{v_{op}(s)}{d_p(s)} = G_{vd}(s) = \frac{V_{rms}(sCR_c + 1)(1 - sL/RD'^2)}{D'^2 \Delta(s)}, \quad (27)$$

$$\frac{i_{Lp}(s)}{v_{inp}(s)} = G_{ig}(s) = \frac{1}{RD'^2} \frac{sCR + 1}{\Delta(s)}, \quad (28)$$

$$\frac{i_{Lp}(s)}{d_p(s)} = G_{id}(s) = \frac{2V_{rms}}{RD'^3} \frac{1 + sCR/2}{\Delta(s)}, \quad (29)$$

$$H_e(s) = \frac{s^2}{\omega_s^2} + \frac{s}{\omega_s Q_s} + 1, \quad (30)$$

where :

$$\omega_s = \frac{\pi}{T_s}, \quad Q_s = -\frac{2}{\pi},$$

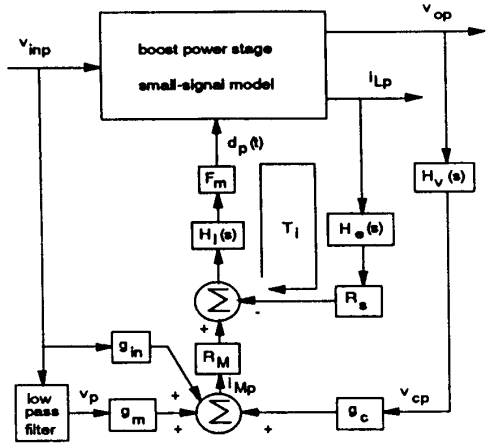

Fig.9: The small-signal model block diagram of the HPF boost converter.

$$\Delta(s) = \frac{s^2}{\omega_o^2} + \frac{s}{\omega_o Q_o} + 1, \tag{31}$$

and

$$\omega_o = \frac{D'}{\sqrt{LC}}\ ,\ Q_o = \frac{R}{L\omega_o}.$$

For constant power load :

$$\Delta(s) = \frac{s^2}{\omega_o^2} - \frac{s}{\omega_o Q_o} + 1, \tag{32}$$

$$G_{id}(s) = \frac{V_{rms}\, sC}{D'^3\, \Delta(s)}. \tag{33}$$

Current Loop Design:

The current loop, as in Fig.9, is given by :

$$T_i = F_m R_s H_e(s) H_i(s) G_{id}(s). \tag{34}$$

To achieve tight control, and good dynamic performance of the average inductor current, the current loop must have high low-frequencies gain, wide bandwidth, reasonable stability margin and reduction of the switching noise. A two-pole, one-zero compensator can be used to compensate the second order duty-cycle to inductor current transfer function given in Eq.(29). The compensator is :

$$H_i(s) = \frac{\omega_i}{s}\frac{1 + s/\omega_{zc}}{1 + s/\omega_{pc}}. \tag{35}$$

The compensation zero, ω_{zc}, is placed around the resonant frequency of the power stage, and the compensation pole, ω_{pc}, is placed above half of the switching frequency to attenuate the switching ripple in the feedback loop and to minimize the phase lag at the loop gain cross-over frequency, ω_{cc}. The DC gain of the current loop is controlled by R_s and ω_i. The DC gain is designed to maximize the current loop cross-over frequency , ω_{cc}, and as was shown in [13]. ω_{cc} is limited to be below half of the switching frequency due to the sampling effect.

It is important to notice that the current loop model in Eq.(34) describes the current loop dynamic up to half of the switching frequency, and includes the sampling effect, $H_e(s)$, and reveals that $G_{id}(s)$ is a second order system as shown in Eq.(29). In [6,11,14], the sampling effect is not taken into consideration, and a first-order model,

$$G_{id}(s) = \frac{V_o}{sL}, \tag{36}$$

was derived by replacing the output capacitor with a constant voltage source, as a result, $G_{id}(s)$ was reduced to a single pole system. The model in equation (36) agrees with equation (29) for frequencies higher than the resonance frequency of the power stage. As a result, the design procedure of the current loop presented in this paper is different form the ones described in [6,11,14]. In [14], the current loop bandwidth is limited to below third of the switching frequency to prevent subharmonic oscillations, and the zero of the compensator is below the cross-over frequency to provide 45° phase margin. As a result, the current loop bandwidth is reduced, and the low-frequencies gain is not optimized.

Outer Loop Design:

The dynamics of the converter with the current loop closed is analyzed using Fig.9 and equations (26-35). The control voltage-to-inductor current and the control voltage-to-output voltage with closed current loop are given by:

$$\frac{i_{Lp}}{v_{cp}}(s) = \frac{F_m g_c R_M H_i(s) G_{id}(s)}{1 + T_i}, \tag{37}$$

and

$$\frac{v_{op}}{v_{cp}}(s) = \frac{F_m g_c R_M H_i(s) G_{vd}(s)}{1 + T_i}. \tag{38}$$

For frequencies lower than the current loop cross-over, and the ESR zero, the following approximations are valid :

$$\frac{i_{Lp}}{v_{cp}}(s) = g_c \frac{R_M}{R_s}, \tag{39}$$

for resistive load :

$$\frac{v_{op}}{v_{cp}}(s) = g_c \frac{R_M}{R_s}\frac{V_{rms}}{V_o}\frac{R/2}{1 + sCR/2}, \tag{40}$$

and for constant power load:

$$\frac{v_{op}}{v_{cp}}(s) = g_c \frac{R_M}{R_s}\frac{V_{rms}}{V_o}\frac{1}{sC}. \tag{41}$$

The results in equations (39-41) are the same as in [3] when V=1 (the low pass filter is removed).

It is important to notice that the control voltage-to-output voltage is independent of the line and of the load conditions as seen from equation (40-41), for frequencies higher than 2/RC (which is usually very low frequency), for resistive load, and for all the frequencies in the case of constant power load.

The bandwidth of the voltage loop is designed to be less than 1/4 of the line ripple frequency to get low distortion in the inductor current (usually 10-20 Hz).

For constant power load, the compensation is :

$$H_v(s) = \frac{\omega_v}{1 + s/\omega_{pv}}, \tag{42}$$

where ω_{pv} is placed after the cross-over frequency of the voltage loop. It should be low so that the line ripple is well attenuated (usually 30-40 db), but it has to be chosen to get reasonable phase margin.

For resistive load, the compensation is given by :

$$H_v(s) = \frac{\omega_v}{s}\frac{1+s/\omega_{zv}}{1+s/\omega_{pv}}, \qquad (43)$$

where ω_{zv} is placed at 2/RC, and ω_{pv} is placed after the cross-over as in the case of the constant power load. In both cases of resistive and constant power load, ω_v is used to determine the bandwidth of the outer loop.

It is important to notice that the voltage compensation design for constant power load is the same as in [14].

The Low Pass Filter Design:

The low pass filter is used to achieve : (1) a control voltage-to-output voltage transfer function that is independent of the line load conditions, (2) the input power is independent of the line conditions and is determined by the control voltage. To reduce the harmonic distortion in the inductor current, the line ripple on the output of the low pass filter has to be very small (usually < 1%). Hence, the low pass filter is designed to have a double real pole at frequency less than 1/5 of the line ripple. This design is the same as in [14].

MODEL VERIFICATION

The small-signal model was tested using a 300 W, 300 VDC output, 160 VRMS input, and 50 KHz switching rate HPF boost converter, shown in Fig.10. The control voltage to inductor current and the control voltage to output voltage frequency responses, with the current loop closed, were measured. Two sets of measurements were performed :(1) the input voltage is a rectified 60 Hz line voltage, (2) the input voltage is a DC voltage that is equal to the RMS value of the rectified line voltage in (1). The measurements were performed for different line and load conditions, and compared to the simulations using the proposed small-signal model. The results are summarized in Fig.11. The measurements with rectified line input agree well with the measurements performed with a DC input voltage. The simulation results agree with measured data; however, there are some differences at high frequencies, but these differences are within 5 db, so that the simulation results are a good approximation of the measured data.

There was an attempt to measure the current loop. It was difficult to get the current loop information due to the high gain and noisy current loop. Future work will include attempts to measure the current loop, input impedance, and output impedance.

To summarize, the dynamics of the HPF boost converter with the current loop closed can be predicted with good accuracy, using the small-signal model in Fig.9. The most important measurement used to verify the proposed model is the control voltage to output voltage, because the critical approximation done when deriving the model is linearizing the diode current. The control to output voltage measurement agrees with the simulations, so that the authors believe that the small-signal model is a good approximation of the HPF boost converter.

CONCLUSIONS

A simple and accurate small-signal model was developed for the HPF boost converter with constant frequency current control. The model was used to analyze and design the small-signal dynamics of the HPF boost converter with average current control. The main concept used and verified in deriving the model is that the HPF boost converter can be approximated by a linear time-invariant system. Hence, to get the small-signal dynamics, the rectified line voltage can be replaced by a DC voltage equal to the RMS value of the line, so that all the analysis and design techniques used for DC-DC converters can be applied to the design of the HPF boost converter. The proposed model is applicable to all the frequencies below half of the switching frequency. The model was verified using large-signal simulations and hardware measurements. The derived model agrees with the previously published models [1,3] at low frequencies and with [6,11,14] at high frequencies.

Control design, using the proposed model, was performed and a design guideline was introduced.

The small-signal model is useful in designing the control loops, especially the current loop, and in the analysis of the dynamics of the HPF boost converter, such as the input and output impedances and the audiosuceptibility.

The model was derived for the boost converter in the CCM, but in a similar way, small-signal models can be derived for boost in DCM, or buck and buck-boost converters.

Future work will include further verification of the derived model, such as measuring the current loop, input and output impedances, extension to DCM and buck and buck-boost converters, and application of the model in the analysis and design of distributed power system that includes HPF boost converter.

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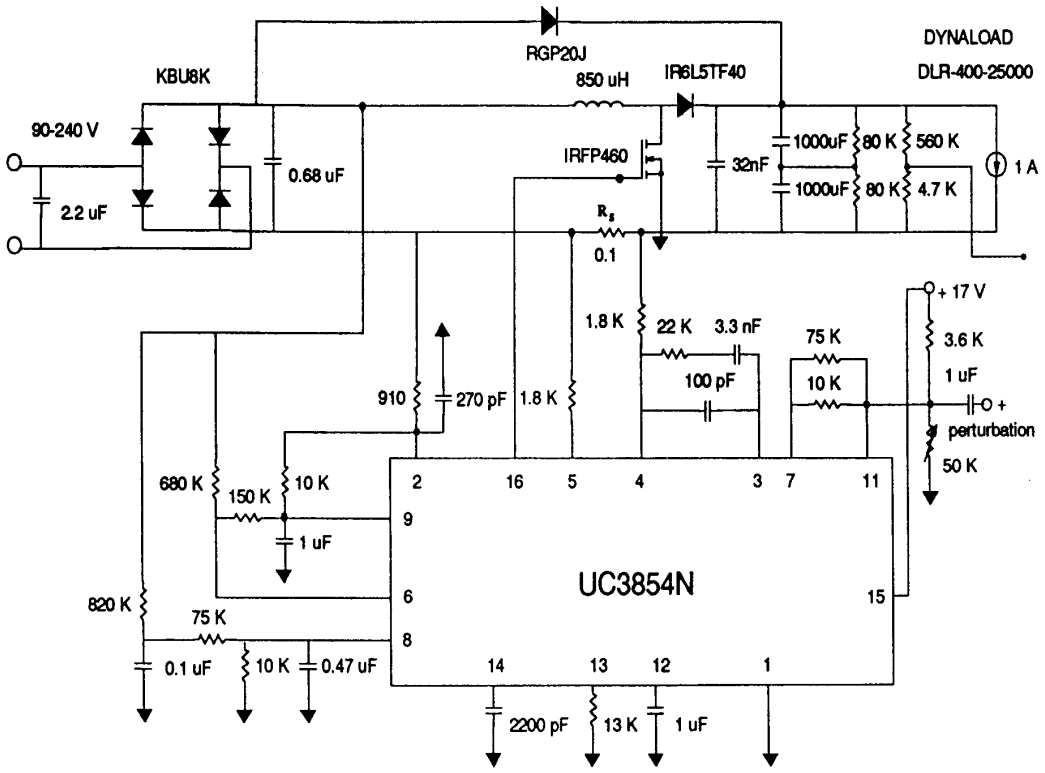

Fig.10: The HPF boost converter used to perform small-signal measurements.

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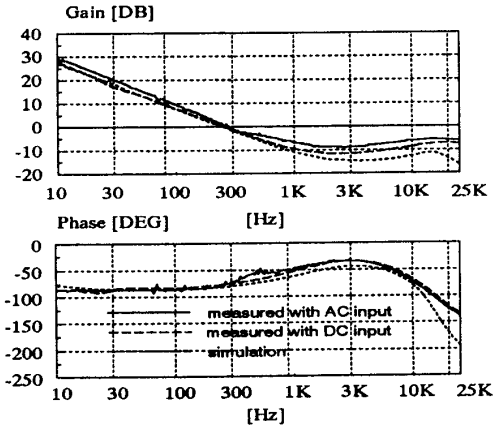
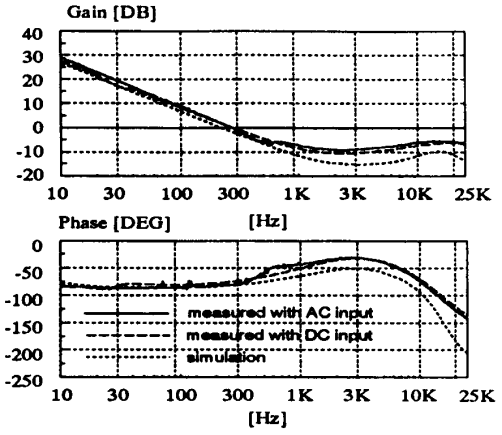
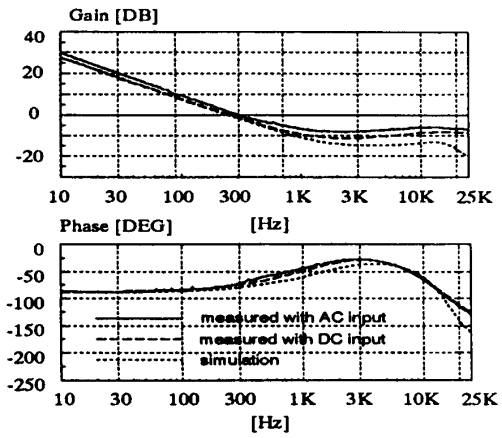


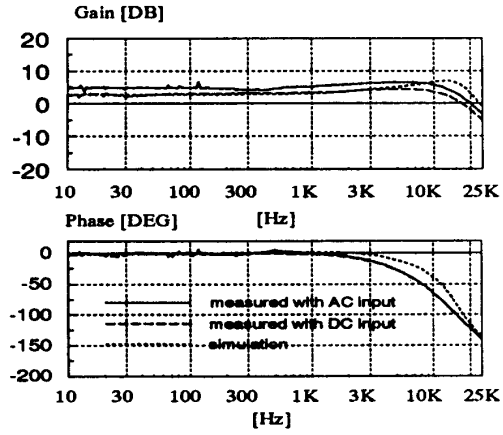
(a) v_{op}/v_{cp} :160 VRMS, 300 W, 300 VDC



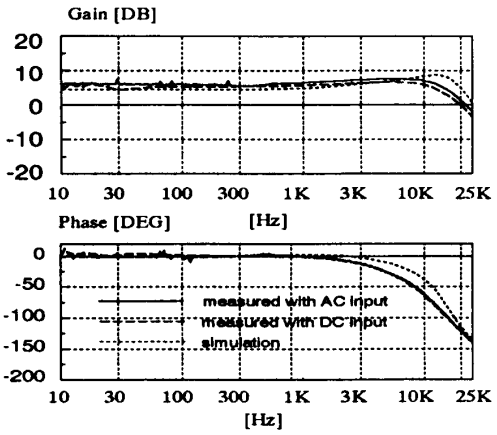
(b) v_{op}/v_{cp} :130 VRMS, 300 W, 300 VDC



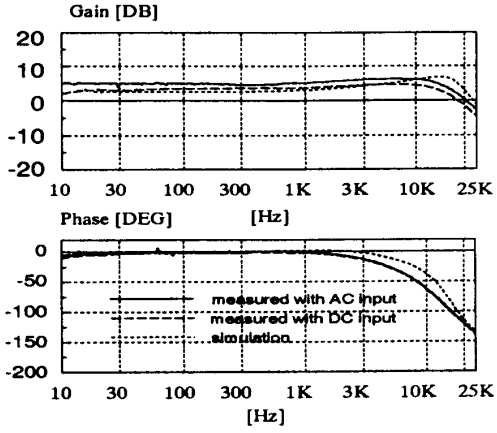
(c) v_{op}/v_{cp} :160 VRMS, 100 W, 300 VDC



(d) i_{Lp}/v_{cp} :160 VRMS, 300 W, 300 VDC



(e) i_{Lp}/v_{cp} :130 VRMS, 300 W, 300 VDC



(f) i_{Lp}/v_{cp} :160 VRMS, 100 W, 300 VDC

Fig.11: Measurements and simulations results : control-voltage to output voltage and control-voltage to inductor current with the current loop closed.