D. ANDREU, D. STEPAN, S. JOSSE
ENSEEIHT, ELECTRONIC LABORATORY
2, RUE. C. CAMICHEL, BP 7122 31500 TOULOUSE CEDEX 7 – FRANCE
andreu@len7.enseeiht.fr, stepan@len7.enseeiht.fr, josse@len7.enseeiht.fr

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INTRODUCTION TO BEHAVIORAL MODELING
and
PHASE LOOP LOCKED BEHAVIORAL MODELING (EXAMPLE WITH PSPICE)

Introduction to behavioral modeling

A. THE INTEREST OF THE SIMULATION FOR THE ANALOG DESIGN

In the world of analog ASIC's design, the simulation become a standard approach that lead to the optimal performances, with the lowest price. It enables the changing, the optimizing and the validation of the circuit performances on the whole design process, by taking into account the technology specifications and other important design parameters, as the temperature. These must be possible to perform static (DC), small signal (AC) and transient (TRAN) analysis. Moreover, for the circuit validation, the simulator must enable the sensitivity and Monte Carlo analysis on the technological parameters (transistor's parameters) and on the topological one (the values of the passive elements). The accuracy and the representativity of the results depend both on the technological parameters given by the CI vendors and on the primitive models available in the simulation packages.

B. AVAILABLE TOOLS

The SPICE type simulator tool offers a great variety of primitives (transistors, resistors, capacitors and inductors) for the circuit description purpose. Each primitive has a corresponding model those us more or less accurate (the transistor levels). The information linked with the technology is delivered to the simulator as specific IC technology parameters. The so-called transistor level description consists in using these primitives to model a given circuit. For this type of simulators, the order of the matrix system to be solved is proportional with the number of nodes within the circuit [2]. There can be concluded that when the number of transistors become significant (from some hundreds to some thousands depending on the analog circuit topology) the simulation time become prohibitive and the convergence problems risk also rises [1].

C. ENHANCEMENTS

In order to decrease the simulation time, there must be decreased the number of circuit's internal nodes, without a significant loose of information. In fact, the simulation used in the design process must be as much accurate and representative as possible. Till here the modeling has been performed at component level (transistor, capacitor, resistor) [3]. These must be developed new primitives for the circuit description purpose that are situated at a higher level than the one of components and which keeps the maximum amount of information concerning the technological parameters, the topological one.

D. THE LEVEL CONCEPT

When investigating the analog circuit structure, several levels of function description can be distinguished. Firstly, the lowest transistor level containing the simulator's primitives (transistors, passive elements) [4]. Then the basic building functions that are the elementary bricks for the ICs (current mirrors, differential stages, current and voltage sources, VCO) [5]. Then a circuit can be investigated at the functional level (OpAmp, PLL, Filters etc) [6], and finally, the circuit can be modeled at its global function level, or the so-called system level description. In practice, when we pass of a higher hierarchical description level, the information loose increases and the simulation time decrease. Therefore, the challenge is how to solve the conflict between the accuracy and the simulation time. The SPICE simulator is actually the standard CAD tool for the IC design. It contains intrinsic models for most of the IC devices, that give a good accuracy for the purely electrical simulations within the device safe operating area. However, the bipolar and MOS transistor intrinsic models were developed for the standard IC technologies and thus they give considerable errors when simulating the new types of IC bipolar transistors, or the sub micron MOS transistors.

Actually there exist four methods to improve the accuracy of the SPICE models [1]: the structural macro modeling, the C codes modeling, the AHDL (Analog Hardware Description Language) modeling and finally the Analog Behavioral Macro modeling (ABM).

The structural macro modeling consists in building a sub circuit description of a given device, using the existing SPICE2 intrinsic models (primitives). This method is mainly used for modeling the parasitic elements of an IC device.

The C code modeling consists in changing the existing C code subroutine of the SPICE intrinsic models (the Device Equation facility of the PSPICE simulator [9]), or in creating a new C code subroutine that describes device's internal static and dynamic equations (the C code modeling facilities of the Is SPICE simulator [5]). This modified or new C code subroutine is compiled and linked as a DLL file to the simulator.

The C code modeling was used to develop both an avalanche breakdown model [6], and an electrothermal model [7] for the IC and power semiconductor devices. The great advantage of the C code modeling is the flexibility, as any kind of nonlinear algebraic and differential equations can be modeled. The drawbacks are the leak of portability from a simulator to another (as there does not exist an universal accepted C code modeling standard) and the difficulty to investigate and to solve the analysis convergence and the simulator's stability problems.

The Analog Hardware Description Languages (AHDL) is more and more used to develop new high accuracy mixed technologies models (electrical-thermal-mechanical-optical). The most used AHDL is the MAST language implemented in the SABER simulator. There were already developed avalanche breakdown and electrothermal MAST models for the power semiconductor devices [8]. The main advantage of the MAST modeling is that the language is integrated in the simulator, that needs no more to be recompiled and/or linked with the new model. The drawback is again the leak of the portability to the SPICE like simulators.

The VHDL – AMS (for Very High Speed Integrated Circuits Hardware Description Language – Analog and Mixed Signal) is the last standard IEEE VHDL 1076.1.This language extends the existing VHDL 1076 language for analog and mixed circuits.

The last generation of SPICE simulators have introduced a new and powerful modeling technique : the so called Analog Behavioral Macromodeling (ABM), that consists in building a sub circuit description of the device, using the nonlinear controlled voltage and current sources to implement the device's internal static and dynamic equations. The great advantages of the ABM method are the portability to all the modern SPICE simulators that support the ABM facilities and also the free user's access to the macro model's internal equations and variables. Although actually there does not exists a standard for the ABM facilities, most of the modern SPICE simulators support the Berkeley SPICE3 syntax, that can be considered almost a standard (Is SPICE, AIM-SPICE).
The PSPICE simulator has a different syntax [11], but the translation between the SPICE3 and PSPICE needs minimal syntax adjustments.

The ABM method is a serious competitor of the C code and AHDL modeling techniques, as it assures a comparable accuracy, with a simpler and easier modeling procedure and it brings only a slightly increase of the simulation time (the ABM macro models are not compiled models and thus they are interpreted by the simulator at each analysis time step).

To contrast the high-level and low-level modeling approaches, we consider a simple phase-locked loop (figure 1). The phase locked loops contain three major components: a voltage-controlled oscillator (VCO); a phase detector that compares the output of the VCO with the input (target) signal to derive an error signal; and a loop filter. The inverted output of the loop filter becomes the controlling voltage for the VCO, thus forming a negative feedback control loop [14].

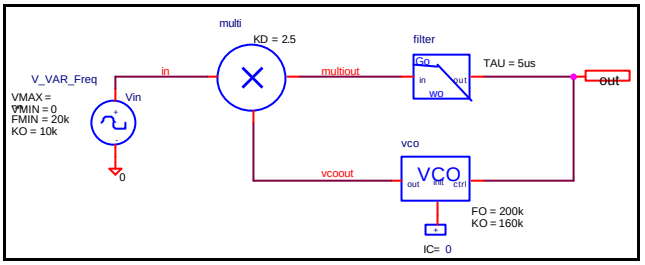


Fig. 1 : Behaviorial modelling of the three devices (phase detector, filter and vco) and the PLL.

Phase Loop Locked Behavioral Modeling
(Example with PSPICE)

I. PSPICE MACROMODELING

The principle of the PSpice ABM - Analog Behavioral Modeling - consist to model the internal maws that describes behavior of device or circuit with non-linear controlled voltage and current sources. In PSpice we have two types of ABM sources : time domain behavioral sources and frequency domain behavioral sources.

A. THE TIME DOMAIN NONLINEAR CONTROLLED SOURCES

"In line equation" sources, that enable the simulation of practically all the mathematical nonlinear expression. We have two types of devices :

1/ EVALUE voltage controlled voltage source
2/ GVALUE voltage controlled current source

At the beginning these sources were controlled only in voltage, but now they can be controlled by a voltage, a current, or even by an expression that contains different circuit voltages and currents. The value type sources have the general form **:**

1/ Ename N+ N- VALUE ={control expression}
2/ Gname N+ N- VALUE ={control expression}

The "TABLE defined" control sources, that permits the piece-wise-linear approximation of the input-output transfer function. We have also two types of devices :

1/ ETABLE voltage and current controlled voltage sources ;
2/ GTABLE voltage and current controlled current sources.

This kind of controlled sources has the general form :

1/ Ename N+ N- TABLE {input expression } = (input1, Vout1) (input2, Vout2) . .
2/ Gname N+ N- TABLE (input expression } = (input1, Iout1) (input2, Iout2) . . .

B. FREQUENCY DOMAIN CONTROLLED SOURCES

"In line LAPLACE function" sources, that enable the simulation of the Laplace transfer functions directly as controlled voltage and current sources. So an entirely electronic bloc, for which we know the transfer function, can be modeled as a simple controlled source.

This approach is used in system level simulations. We have two types of devices:

1/ ELAPLACE voltage or current controlled voltage source ;
2/ GLAPLACE voltage or current controlled current source.

The general form for this type of source is :

1/ Ename N+ N- LAPLACE {input expression }={S form expression}
2 /Gname N+ N- LAPLACE {input expression}={S form expression}

II. THE PLL MODELING

The Phase Locked Loop used in this project is the NE565 IC PLL. This is a standard PLL integrated circuit that, apart from the bias circuitry, contains a Schmitt trigger for the VCO and a Gilbert multiplier for the phase detector. It has 28 transistors, 10 diodes and many resistors. The simulation of this circuit at the transistor level is especially difficult and not sure because not all the values for the IC internal elements are available and because the topology is too complex. However, it is out of the aim of this project. The goal here is to use an IC whom the characteristics are given in the data-sheets and not to perform an accurate simulation of IC internal behavior. Thus, a behavioral macro model is sufficient for the required accuracy. This one has also the advantage of being tractable by the evaluation version of PSPICE and thus, of an easy portability. The PLL will be modeled by using a cascade of a multiplier function, a first order filter and a VCO. The multiplier function is defined as the multiplication of the two input voltages (the first one is the signal to be demodulated and the second one is the VCO output) that have also a K_D factor, representing the voltage to delta phase conversion. The filter is defined with its Laplace domain transfer function. Finally, the VCO is implemented with a sinus function in which the phase is linked to the VCO control voltage [6].

The behavioral model : each one of the three main components of the PLL can be expressed succinctly in PSpice's extended behavioral modeling syntax.

1/ the phase detector is a multiplier with the output range constrained to [-1, +1]. It uses gain blocks, limiters, and a multiplier.

2/ the VCO is described as a sinusoidal function of time with an additional term controlling the phase.

3/ the loop filter is described by giving its Laplace Transform, using s-domain notation.

A complete description of the PLL consists of these three “devices,” along with a test stimulus (a VCO).

SPICE MODEL FOR PLL

In that follows we are going to show the netlist of the PLL macro model in ORCAD-PSPICE that contains the following sub circuits : a phase detector, a filter and a VCO that haves some parameters.

The phase detector has the kd like parameter, the filter have tau and the VCO have two parameters : fo and ko. In this way we can make parametric simulations.

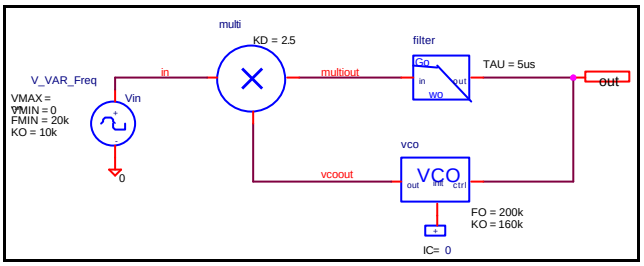


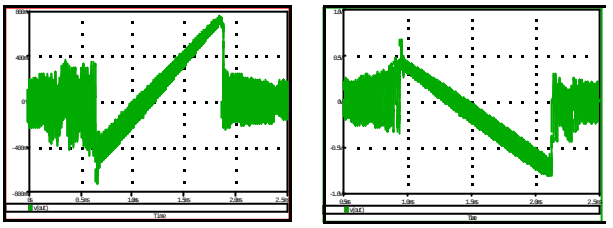
Fig. 1 : Behaviorial modelling of the three devices (phase detector, filter and vco) and the PLL.

```
*phase detector
.SUBCKT mult in1 in2 produit params:
+ kd=2.5
E_E1 produit 0 TABLE
+ {{kd}*V(in1)*V(in2)}
.ENDS mult

*filter
.SUBCKT filtre in out params: tau=5u
E_E1 out 0 LAPLACE
{V(in,0)}={1/(1+tau*s)}
.ENDS filter

*VCO
.SUBCKT vco ctrl init out params:
+ fo=200k ko=160k
* the node “init” is necessary to
* initialize the transient simulation

C_C1 0 init 1u
R_R1 0 init 1g
G_G1 0 init VALUE {ko*V(ctrl,0)*1e-6}
E_E1 out 0
VALUE{sin(6.28*(fo*time+V(init,0)))}
R_R3 out 0 1g
.ENDS    vco


* PLL
X_MULT1 VCOOUT IN MULTIOUT MULT
+ params: kd=2.5

X_vco1  OUT N014830 VCOOUT vco
+ params: fo=200k ko=160k

X_filter MULTIOUT OUT filtre-X
+ params: tau={tconst}

V_V1 IN 0  SFFM 0 1 200k 10 5k

.IC  V(N014830 )=0
.PARAM  tconst=5u
```

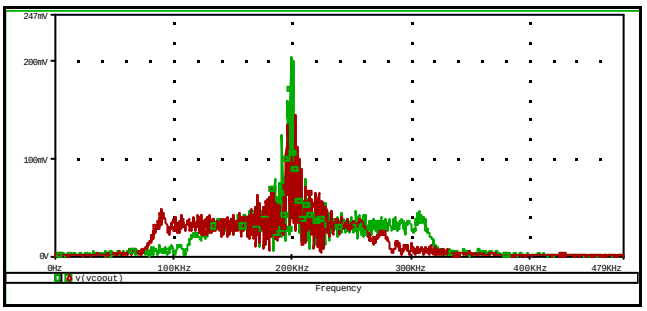
A transient analysis is run to analyze capture and lock ranges. The PLL does not respond to the input signal until the input frequency reaches the lower edge of the capture range. Up to the lower capture frequency, the VCO output frequency does not change significantly since the average voltage of the beat frequency is zero. The model then suddenly locks to the input signal, causing a negative jump in loop error voltages. Here we see the nonlinear capture transients.

Once locked the error signal tracks small frequency changes of the input signal by generating additional phase error between the VCO and the input signal. This signal is converted to the DC error voltage by the phase detector and low-pass filter.

At the upper lock range frequency, the model loses lock, and the error voltage suddenly drops. And then becomes a beat note.

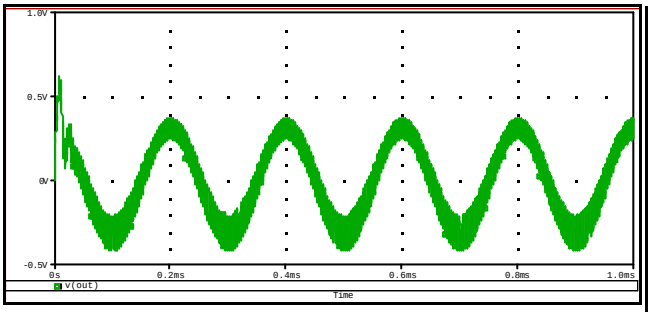


(a)

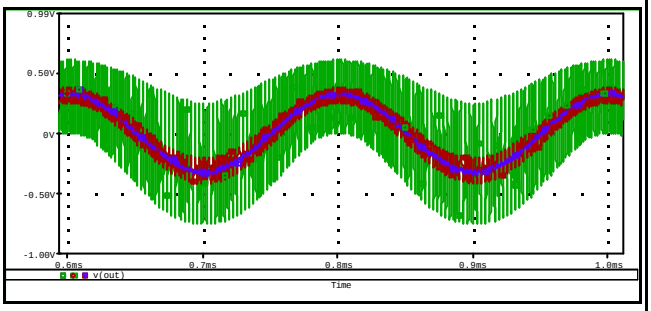


(b)

Fig. 2 : (a) the output statemt of filter (increasing and deacresing entrance frequency) and (b) frequency response of the VCO



(a)



(b)

Fig. 3 : (a) demodulation and (b) demodulation for different values of tau

PARAMETRIZATION

The time required to run the analysis of the PLL is significant. The behavioral model allows many more analyses to be run in a given time, permitting a higher degree of design refinement and/or test.
Consider modeling devices with different parameters from the example set used above, for example to produce a library of devices for general use. It may be possible to define a *"generic"* device and map inputs and outputs appropriately. The differents parameters of the PLL are the folowing : fo and ko for the VCO, kd for the multiplier and tau for the filter.

III. CONCLUSION

This paper presents a synthesis on the types of electronic circuits modeling (structural modeling, behavioral modeling, modeling in high level programing languages) while showing what are advantages and inconveniences of each one. In a second time we will demonstrate on a complex circuit how from a common methodological approach (decomposition of the PLL in fundamental bricks : VCO, filter, etc...) we can define a behavioral model of a circuit or a some complex system either the language that we have PSpice or VHDL-AMS.
The methodological approach for the development of a behavioral model is a primordial stage that allows to the designer to have a some uniform gait either the used tools.

THE AUTHORS

Dr. Danielle Andreu, Daniela Stepan and Josse Steve are with the Microelectronic Laboratory of National Polytechnic Institute ENSEEIHT- INP, Toulouse, France.
E-mail: andreu@len7.enseeiht.fr
stepan@len7.enseeiht.fr
josse@len7.enseeiht.fr

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