Analysis and Design of Self-Oscillating Flyback Converter

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Abstract –The self-oscillating flyback converter is a popular circuit for cost-sensitive applications due to its simplicity and low component count. It is widely employed in mobile phone chargers and as the stand-by power source in off-line power supplies for data-processing equipment. However, the optimization of this circuit is almost exclusively performed by a cut-and-try approach since its operation is generally not well understood. This paper presents a detailed steady-state analysis of the self-oscillating flyback converter along with its small-signal model. Design guidelines of the control circuit and loop compensation are presented and verified on an off-line, stand-by, 5-V/ 2-A power supply.

I. INTRODUCTION

The self-oscillating flyback converter, often referred to as the ringing choke converter (RCC), is a robust, low-component-count circuit that has been widely used in low-power off-line applications. Since the control of the circuit can be implemented with very few discrete components without loss of performance, the overall cost of the circuit is generally lower than the conventional PWM flyback converter that employs a commercially available integrated control .

Generally, the operation of the circuit is not well understood. This is primarily due to the fact that existing literature deals with the circuit in a very superficial manner [1]-[2]. Therefore, the design of this converter usually follows a cut- and-try approach, which is a time consuming process and which usually doesn't lead to an optimized design.

The purpose of this paper is to present a complete design-oriented steady-state analysis and small-signal model of the self-oscillating flyback converter that can be used in the optimization of this circuit. In addition, a step-by-step design procedure of the control circuit is presented and verified on an off-line, 5-V/2-A, stand-by power supply.

II. ANALYSIS OF OPERATION

The self-oscillating flyback converter operates at the boundary of continuous/discontinuous conduction mode (CCM/DCM) and utilizes peak current mode control. Therefore, the circuit operates with a variable switching frequency. The implementation of the control is done discretely, which is simple and cost effective since the pulse-width modulator (PWM) and switch driver are implemented with a single transistor, a positive-feedback winding, and a resistor divider network. In applications which do not require tight regulation, a simple feedback control consisting of a single zener diode may be implemented. However, in applications which require a tight output regulation, such as applications with a wide range of input voltage and load current, an error amplifier is often implemented.

The circuit diagram of an isolated self-oscillating flyback converter with output voltage control is shown in Fig. 1. Transformer T_1 consists of 2 secondary windings: output winding N_{S1} and positive-feedback winding N_{S2}. Main output V_{O1} is isolated, and tightly regulated by error amplifier E/A, whereas auxiliary output V_{O2} is not isolated, and is loosely regulated by main output V_{O1} through transformer T_1. Output voltage V_{O1} is sensed through a resistor divider consisting of resistors R_{d1} and R_{d2}, and compared at the input of a transconductance type amplifier (TL431) to a stable voltage reference located within the TL431 device. Components C_{EA1}, C_{EA2}, and R_{EA1} are used as compensation to stabilize the voltage control loop. The difference between the sensed output voltage and the voltage reference is amplified by TL431 and reflected to the primary side through optocoupler IC_1 as error current i_e, which in turn develops error voltage V_e across (the sum of) resistors R_S and R_F. Error voltage V_e is summed with a voltage proportional to switch current i_{S1} and compared at the PWM modulator, which is implemented with bipolar junction transistor (BJT) Q_1, to a fixed voltage threshold, which, in this case, is cut-off voltage V_γ of transistor Q_1. Zero-current detect components C_{ZCD} and R_{ZCD}, along with winding N_{S2}, sense, with some delay, the continuous/discontinuous conduction mode (CCM/DCM) boundary of transformer T_1, and delivers charge to main switch S_1 to initiate switch turn-on. Finally, circuit start-up is
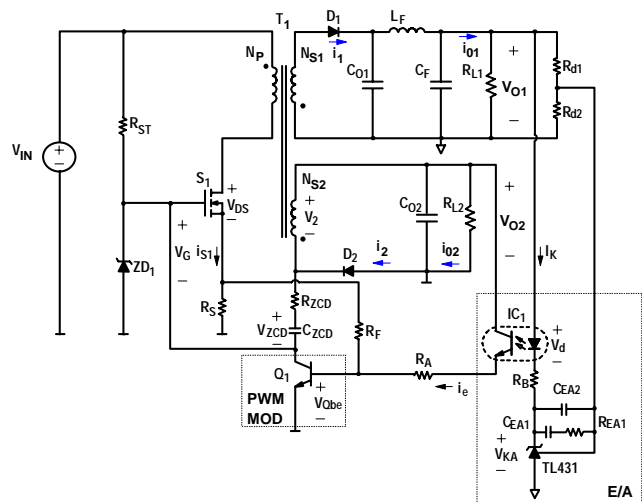

Fig. 1 Circuit diagram of self-oscillating flyback converter

initiated through resistor R_{ST}, which delivers charge to input capacitance C_{ISS} of main switch S_1 from input voltage V_{IN}.

A. Steady-State Operation

In order to simplify the explanation of the converter shown in Fig. 1 during steady-state operation, several approximations have been made. The first approximation is to neglect the leakage inductance of transformer T_1. This eliminates the need to consider the action of a voltage clamp across primary winding N_P which is implemented to protect main switch S_1 from voltage ringings. The second approximation is to model error current i_e as a constant-current source, i.e., to replace compensated error amplifier TL431, opto-coupler IC_1, capacitor C_F, and resistors R_{d1}, R_{d2}, R_A, and R_B with constant-current source i_e. The final approximation is to neglect the capacitance C_{GD} between the gate and drain terminals of main switch S_1 and to model the terminal capacitances between the gate and source C_{GS} and between drain and source C_{DS} as input capacitance C_{ISS} and output capacitance C_{OSS} respectively. In addition to these approximations, it is assumed that $C_{O1} >> C_{O2}$, and $R_{L1} << R_{L2}$. The assumption $C_{O1} >> C_{O2}$ implies that the ripple voltage of output V_{O2} is greater than the ripple voltage of main output V_{O1}. Another assumption is that time constant $R_{ST}C_{ISS}$ is much greater than switching period T_S, i.e., $R_{ST}C_{ISS} >> T_S$. With this assumption, it is possible to ignore start-up resistor R_{ST} during steady-state operation. Finally, it is assumed that rectifiers D_1 and D_2 are ideal i.e., have zero forward voltage drop while conducting.

To facilitate the explanation of the converter operation, Fig. 2 shows eleven topological stages of the circuit in Fig. 1 during a switching cycle, including the reference directions of currents and voltages, whereas Fig. 3 shows key waveforms of the power and control stage.

Prior to $t = t_0$, current i_{Qce} and voltage V_{CZCD} is positive, and switch S_1 is turning off because charge is drawn from input capacitance C_{ISS} of main switch S_1 by transistor Q_1. As a result, drain-source voltage V_{DS} increases towards $V_{IN} + NV_O$. When, at $t = t_0$, voltage V_{DS} reaches $V_{IN} + NV_O$, rectifiers D_1 and D_2 start conducting. During this stage, which is shown in Fig. 2(a), magnetizing current i_M is instantaneously commutated from switch S_1 to output rectifiers D_1 and D_2 since it is assumed that leakage inductance L_{lkg} of the transformer is zero. In the presence of winding resistances (not shown in Fig. 2), the selection of output capacitors $C_{O1} >> C_{O2}$ causes voltage V_{O1} to be approximately constant while voltage V_{O2} increases, which results in a faster decrease of current i_2 with respect to current i_1, as shown in waveforms (d) and (e) of Fig. 3. Because during this topological stage rectifier D_2 is conducting, voltage V_{RZCD} across resistor R_{ZCD} is equal to $-(V_{GS} + V_S + V_{CZCD}) \approx -(V_{GS} + V_{CZCD})$ since $V_S << V_{GS} + V_{CZCD}$. This voltage induces current i_{ZCD} through resistor R_{ZCD} which discharges capacitors C_{ISS} and C_{ZCD}. At the same time, transistor Q_1 is off and current i_e flows through the loop consisting of resistors R_F, R_S, and R_{L2}. It should be noted that

transistor Q_1 will be in the off state only if it's base-emitter voltage V_{Qbe} is below it's cut-off voltage V_γ. Since, from Fig. 2(a), $V_{Qbe} = i_e R_F + i_{S1} R_S \approx i_e R_F$ because $i_{S1} R_S << i_e R_F$, transistor Q_1 is off during $t_0 < t < t_1$ if $i_e R_F < V_\gamma$. The stage in Fig. 2(a) ends at $t = t_1$ when voltage V_{GS} has decreased to the voltage level which is approximately one diode voltage drop below voltage V_{Qbe} of transistor Q_1 so that its base-collector pn junction becomes forward biased.

After base-collector diode D_{bc} starts conducting at $t = t_1$, current i_e is divided between resistor R_F and the base of Q_1. Because collector-emitter voltage V_{Qce} is negative, transistor Q_1 operates in the inverse-constant-current region and current i_{Qce} flows from the emitter to collector, as shown in Fig. 2 (b). During this stage, capacitor C_{ZCD} continues to discharge by the sum of currents i_{Qce} and i_{Qbc}. As a result, voltage V_{Qbe} increases exponentially as illustrated in waveform (f) of Fig. 3. At the same time, currents i_1 and i_2 continue to decrease. This stage ends at $t = t_2$ when rising voltage V_{O2} reaches the winding voltage V_2 and rectifier D_2 turns off. Meanwhile, capacitor C_{ZCD} continues to discharge through winding N_{S2}, as shown in Fig. 2(c). During this stage, current i_1 continues to decrease. This stage ends at $t = t_3$ when current i_1 reaches zero, i.e., when magnetizing energy of the transformer is completely discharged.

Since at $t = t_3$, drain-source voltage V_{DS} of switch S_1 is higher than input voltage V_{IN}, capacitor C_{OSS} starts to resonantly discharge through magnetizing inductance L_M, as can be seen in waveform (b) of Fig. 3. As a result, primary voltage V_P decreases, causing a proportional decrease in secondary voltage V_2. As the secondary voltage decreases, the voltage across resistor R_{ZCD} also decreases which decreases current i_{ZCD}. This topological stage ends at $t = t_4$ when current i_{ZCD} reaches zero.

After $t = t_4$, current i_{ZCD} starts flowing in the opposite direction so that capacitors C_{ZCD} and C_{ISS} start to charge, as shown in Fig. 2(e). Since the increase of voltage V_{GS} leads to the increase of collector-emitter voltage V_{Qce}, diode D_{bc} turns off, causing the turn-off of transistor Q_1. At the same time, capacitor C_{OSS} continues to resonantly discharge, which further decreases secondary winding voltage V_2. As a result, the voltage across resistor R_{ZCD} increases which causes a further increase of current i_{ZCD}. This topological stage ends at $t = t_5$ when the voltage across the windings of the transformer become equal to zero. After $t = t_5$, capacitor C_{OSS} continues to discharge and the winding voltages change polarity, as shown in Fig. 2(f). Because in this topological stage voltage $V_{O2} + V_2$, which drives current i_{ZCD}, continues to increase, current i_{ZCD} also continues to increase. This increased current i_{ZCD} causes an increase of voltage V_{GS}, which in turn produces a further discharge of capacitor C_{OSS} and consequently a further increase in the sum of voltages V_{O2} and V_2. This positive feedback continues until voltage V_{GS} reaches voltage V_{TH} at $t = t_6$ and switch S_1 is turned on by entering it's constant-current region.

After $t = t_6$, gate-source voltage V_{GS} continues to increase
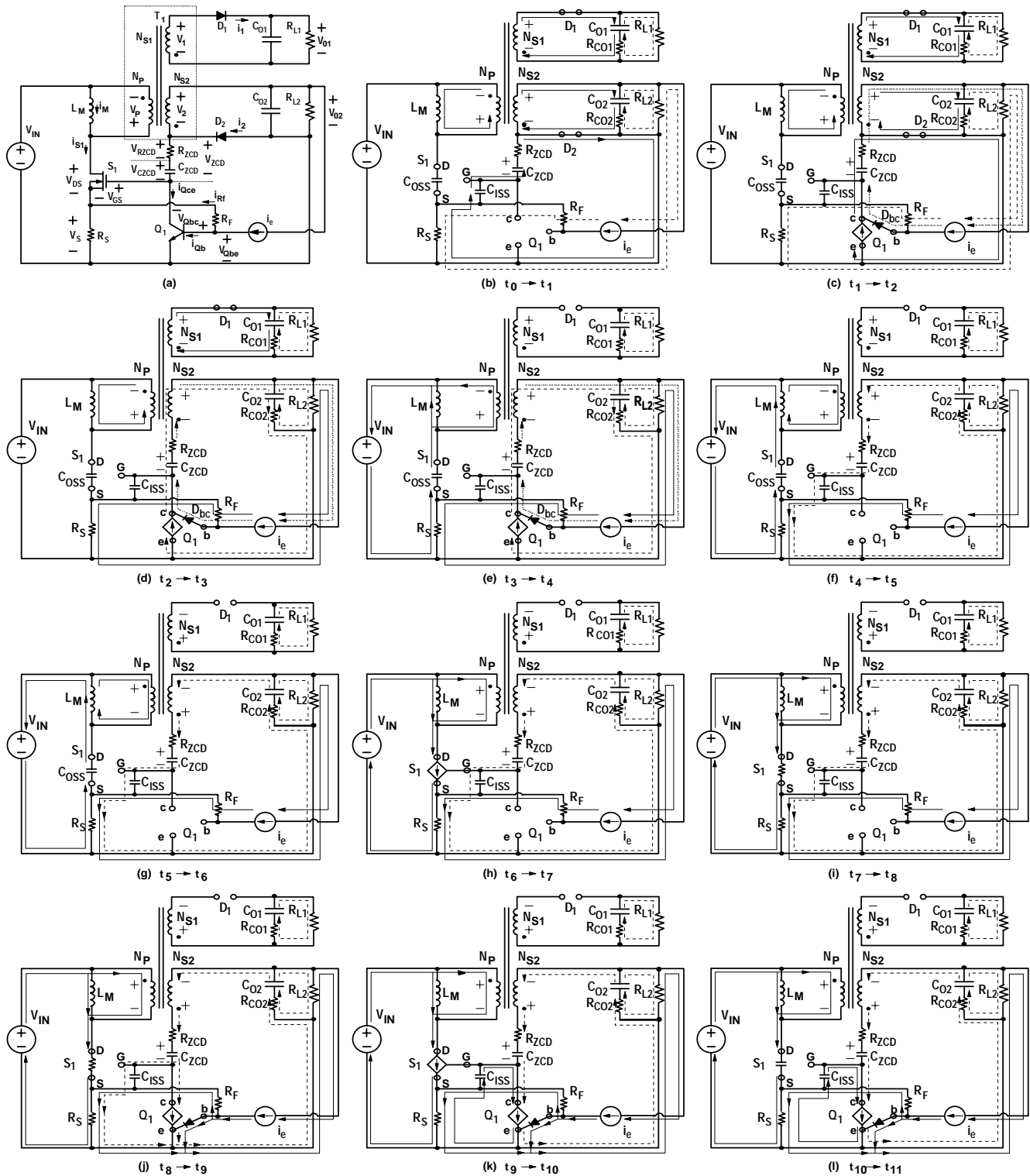
Fig. 2 (a) Simplified circuit diagram of self-oscillating flyback converter which contains voltage and current designators. (b) – (l) Topological stages of self-oscillating flyback converter.

as current i_{ZCD} continues to flow through capacitor C_{ISS}, as shown in Fig. 2(g). This stage ends at $t = t_7$ when gate-source voltage V_{GS} reaches the level where switch S_1 begins operating in the ohmic region, i.e., when switch S_1 is fully turned on. After switch S_1 is fully turned on at $t = t_7$, drain-source current i_{S1} starts increasing linearly with slope $di_{S1}/dt = V_{IN}/L_M$. As a result, voltage drop $V_S = i_{S1}R_S$ across sensing resistor R_S also increases with the same slope. This
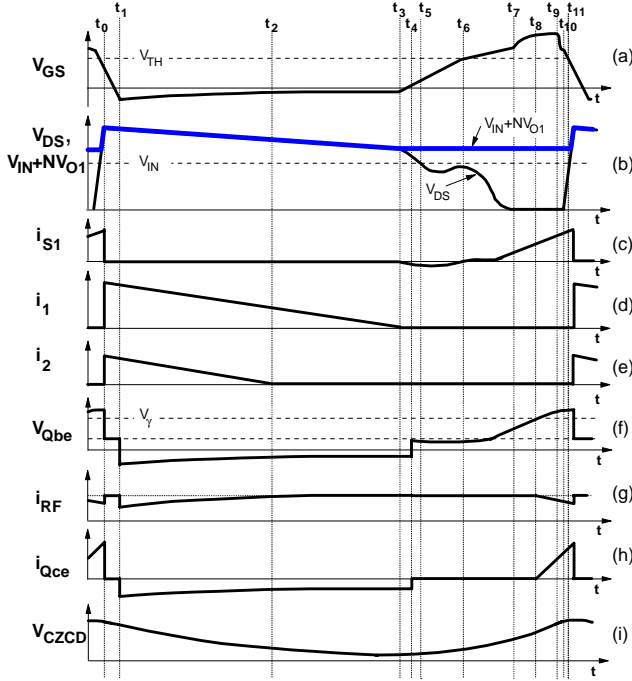
Fig. 3 Power stage and control stage key waveforms

increases the potential of the source terminal of switch S_1, which also increases the potentials of the gate terminal of S_1 and the base terminal of Q_1, as shown in waveforms (a) and (f) of Fig. 3. When, at $t = t_8$, base-emitter voltage V_{Qbe} reaches it's cut-off voltage V_γ, transistor Q_1 starts conducting, as shown in Fig. 2(i). It should be noted that to prevent the gate voltage of switch S_1 of exceeding the maximum rated voltage, a voltage clamp (such as a zener diode) should be connected between the gate terminal of S_1 and ground. Once the gate voltage is clamped, current is diverted from input capacitance C_{ISS} to the voltage clamp until the gate voltage falls below the clamp voltage level.

Since after $t = t_8$ voltage V_{Qbe} continues to increase because voltage $V_S = i_{S1}R_S$ increases, base current i_{Qbe} of Q_1 increases causing the increase of current i_{Qce}. This topological stage ends at $t = t_9$ when current i_{Qce} becomes equal to current i_{ZCD} and gate-source capacitance starts discharging, as shown in Fig. 2(j). As voltage V_{GS} decreases, switch S_1 is turning off. At $t = t_{10}$, voltage V_{GS} decreases to threshold voltage V_{TH} of switch S_1 so that S_1 is turned off. After switch S_1 is turned off at $t = t_{10}$, output capacitance C_{OSS} of switch S_1 begins to charge so that voltage V_{DS} begins to increase. This topological stage shown in Fig. 2(k) ends when voltage $V_{DS} + V_S \approx V_{DS}$ reaches $V_{IN} + NV_O$. At the same time, secondary rectifiers D_1 and D_2 start conducting and transistor Q_1 turns off, which completes a switching cycle.

A. Small-Signal Model

To achieve tight output voltage regulation and good dynamic performance while ensuring system stability, compensation components C_{EA1}, C_{EA2}, and R_{EA1} need to be determined. However, the design optimization of the error amplifier compensation requires knowledge of the small-signal transfer functions in the control loop. Since the self-oscillating flyback converter operates with a variable switching frequency, the small-signal block diagram model differs from that of the conventional, constant-frequency type PWM converter, as discussed in [3].

To facilitate the design optimization of the control loop, the self-oscillating flyback circuit in Fig. 1 has been simplified to include only circuit elements which plays a role in the feedback control, as shown in Fig. 4. Zero-current-detect components R_{ZCD} and C_{ZCD}, which are related to the switching transitions, and zener diode ZD_1, which clamps the potential of the gate terminal of switch S_1, are neglected. Also, since small-signal error current $\hat{i}_e$ is not a function of output voltage V_{O2}, but rather is a function of small-signal error amplifier current $\hat{i}_{EA}$, auxiliary winding N_{S2}, capacitor C_{O2}, resistor R_{L2}, and rectifier D_2 can be neglected. Small-signal error current $\hat{i}_e$ can, therefore, be represented as a dependent current source, as shown in Fig. 4. Finally, start-up resistor R_{ST} is neglected.

Based on this equivalent circuit, the small signal block diagram is derived, as shown in Fig. 5. The block diagram consists of control-to-output voltage transfer function $G_{VeVo}(s) = \hat{V}_O/\hat{V}_e$, output voltage sensing gain $K_d = \hat{V}_1/\hat{V}_O$, error amplifier transfer function $G_{EA}(s) = \hat{V}_{EA}/\hat{V}_1$, transconductance gain $G_1 = \hat{i}_{EA}/\hat{V}_B$, opto-coupler gain $G_2 = \hat{i}_e/\hat{i}_{EA}$, and transresistance gain $G_3 = \hat{V}_e/\hat{i}_e$. The transfer function expressions are summarized in Table 1. The block diagram is further simplified by incorporating transfer function blocks $G_{VeVo}(s)$, G_1, G_2, and G_3 into block $G_{V_{EA}Vo}(s) = \hat{V}_O/\hat{V}_{EA}$ to form a single loop system, where

$$G_{V_{EA}Vo}(s) = \frac{\hat{V}_O}{\hat{V}_{EA}} = \frac{G_1 G_2 G_3 G_{VeVo}(s)}{1 + G_1 G_2 G_3 G_{VeVo}(s)} = \frac{T_{INNER}}{1 + T_{INNER}}, (1)$$
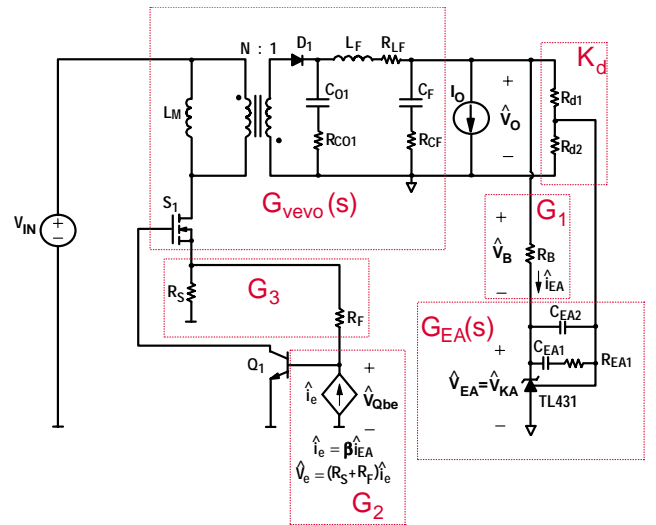

Fig. 4 Simplified circuit diagram of self-oscillating flyback converter for small-signal modeling and analysis
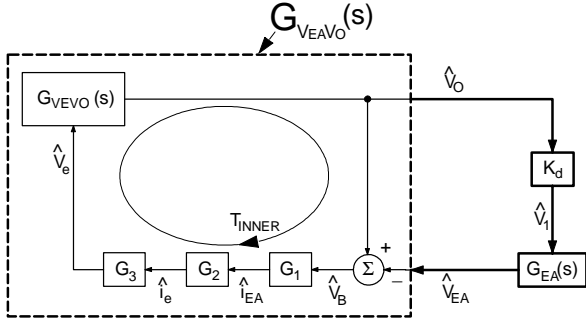
Fig. 5 Small-signal block diagram of self-oscillating flyback converter

and where $T_{INNER} = G_{V_eV_O}(s)G_1G_2G_3$.

As can be seen from Eq. (1), transfer function $G_{V_{EA}V_O}(s)$ has a low frequency gain which is less than 1. Also, poles of transfer function $G_{V_{EA}V_O}(s)$, which are within the bandwidth of inner loop T_{INNER}, are shifted to higher frequencies with respect to power stage transfer function $G_{V_eV_O}(s)$, whereas the location of power stage transfer function zeroes are unaffected by the existence of the inner loop. Assuming that only the first pole, i.e., s_{p1}, of power stage transfer function $G_{V_eV_O}(s)$, is within the bandwidth of inner loop T_{INNER} (i.e., that second stage LC filter resonant frequency $\omega_O > \omega_{INNER}$, where $T_{INNER}(@\ \omega_{INNER}) = 0$ dB), transfer function $G_{V_{EA}V_O}(s)$ can be written in pole-zero form as

$$G_{V_{EA}V_O}(s) = \frac{G_1G_2G_3M_{dc}}{1+G_1G_2G_3M_{dc}} \cdot \frac{(s/s_{z1}+1)(s/s_{z2}+1)}{(s/s_{p1}^*+1)(s^2/\omega_O^2 + s/Q\omega_O + 1)}, \quad (2)$$

where $M_{dc}, s_{z1}, s_{z2}, s_{p1}^*, \omega_O,$ and Q are summarized in Table 1.

By defining transfer function $G_{V_{EA}V_O}(s)$, the system is reduced to a single loop system with loop gain

$$T_1 = K_d G_{EA}(s)G_{V_{EA}V_O}(s). \quad (3)$$

II. DESIGN GUIDELINES

The design of the power stage of the self-oscillating flyback converter follows the well established design rules

for the flyback converter operating at the boundary of continuous conduction mode and discontinuous conduction mode (CCM/DCM), and is out of the scope of this paper. However, the selection of zero-current-detect components R_{ZCD} and C_{ZCD}, as well as the components related to the feedback loop, is generally not well understood, and is therefore discussed below in detail.

A. Steady-State Considerations

To achieve good output voltage regulation during steady-state operation, ramp voltage $i_{S1}R_S$ summed with dc voltage $i_e(R_F+R_S)$ must fit within the "regulation window" throughout the line and load range, as illustrated in Fig. 6. The upper limit of the regulation window is the cut-off voltage V_γ of transistor Q_1, which is inherent to the transistor selected, whereas the lower limit of the regulation window is defined by the full load current. To achieve output voltage regulation, resistors R_B, R_S, and R_F must be carefully selected to limit the error current within this regulation window.

Maximum error current i_e^{max} occurs at minimum load, as shown in Fig. 6. At minimum load, less energy is needed to maintain the output voltage which is why the on time of switch S_1 is very short. Conversely, minimum error current occurs at full load because a longer on time is needed to store the required energy. It should be noted that unlike the standard PWM, whose on time is determined at the moment the ramp voltage reaches the control voltage, the on time of this control circuit is determined once sufficient charge is removed from input capacitance C_{ISS} by transistor Q_1, which is turned on the moment base voltage V_{Qbe} reaches its intrinsic cut-off voltage V_γ.

The design constraints for the selection of the control circuit components for steady state operation are based on the operating range of the circuit as well as on component ratings. Specifically, cathode-anode voltage V_{KA} and cathode current I_K of error amplifier TL431 are limited to $V_{REF}<V_{KA}<36$ V and 1 mA$<I_K<100$ mA. Voltage V_{KA} can be expressed as

TABLE 1
SMALL-SIGNAL TRANSFER FUNCTIONS

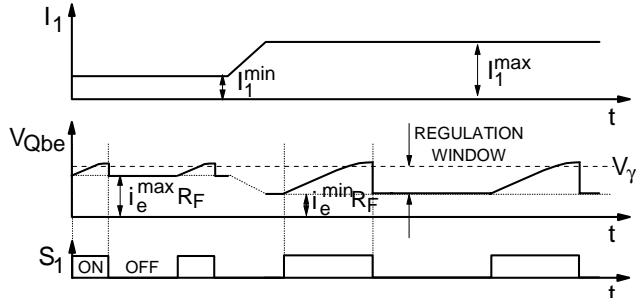| $G_{V_eV_O}(s)$	$M_{dc}\dfrac{(s/s_{z1}+1)(s/s_{z2}+1)}{(s/s_{p1}+1)(s^2/\omega_O^2 + s/Q\omega_O + 1)}$			M_{dc}	$-\dfrac{V_{IN}}{2R_SI_O}$	s_{z1}	$\dfrac{1}{C_{O1}R_{Co1}}$
s_{z2}	$\dfrac{1}{C_FR_{CF}}$	s_{p1}	$-\dfrac{K_r}{C_{O1}+C_F}$	ω_O	$\dfrac{1}{\sqrt{L_F/(1/C_{O1}+1/C_F)}}$	K_r	$-\dfrac{I_ON}{V_{IN}(1+N V_O/V_{IN})}$
Q	$\sqrt{L_F\dfrac{C_F+C_{O1}}{C_FC_{O1}}}\left(\dfrac{1}{R_{Co1}+R_{CF}+R_{lf}+K_r(R_{Co1}R_{CF}-L_F/(C_{O1}+C_F))}\right)$				K_d		$\dfrac{R_{d2}}{R_{d1}+R_{d2}}$
G_1	$1/R_B$	G_2	β	G_3	R_F+R_S	s_{p1}^*	$(1+G_1G_2G_3M_{dc})s_{p1}$
$G_{EA}(s)$	$\dfrac{A}{s}\dfrac{s/s_{zcomp1}+1}{s/s_{pcomp2}+1}$			s_{zcomp1}	$\dfrac{1}{R_{EA1}C_{EA1}}$	s_{pcomp2}	$\dfrac{1/C_{EA1}+1/C_{EA2}}{R_{EA1}}$
A	$\dfrac{R_{d1}+R_{d2}}{R_{d1}R_{d2}(C_{EA1}+C_{EA2})}$						

Fig. 6 Key control circuit waveforms of self-oscillating flyback converter at minimum and maximum load current

$$V_{KA} = V_O - V_d - I_K R_B . \qquad (4)$$

Since at minimum load, current I_K is maximum, as seen from Fig. 5, where $I_K = i_e/\beta$, and, therefore, voltage V_{KA} is at a minimum. Resistor R_B can be expressed as

$$R_B < \frac{V_O - V_d - V_{KA}^{min}}{I_K^{max}} . \qquad (5)$$

The selection of sense resistor R_S is limited by its maximum power dissipation, which, if set to 0.1% of circuit's maximum input power P_{IN}^{max}, is

$$R_S = \frac{0.001 \cdot P_{IN}^{max}}{\left(i_{S1}^{pk}\sqrt{D^{max}/3}\right)^2} . \qquad (6)$$

The selection of resistor R_F is limited at minimum load by maximum error current i_e^{max}, sense resistor R_S, and cut-off voltage V_γ,

$$i_e^{max}(R_F + R_S) \le V_\gamma , \qquad (7)$$

where resistor R_F should be selected much greater than resistor R_S, i.e., $R_F \gg R_S$. At full load, the selection of resistors R_F and R_S are further limited by minimum error current i_e^{min} and maximum switch current i_{S1}^{pk},

$$i_e^{min}(R_F + R_S) + i_{S1}^{pk(max)}R_S > V_\gamma , \qquad (8)$$

where $i_{S1}^{pk(max)} = V_{IN}^{max}D^{max}/L_M f_S^{min}$.

Finally, error current i_e is related to cathode current I_K through dc current transfer ratio β of optocoupler IC_1,

$$i_e = \beta I_K . \qquad (9)$$

The design procedure for the selection of the control circuit components R_F, R_S, and R_B for steady state operation can be broken down to five design steps, summarized in Table 2. It should be noted that resistor R_B, whose value also affects the voltage loop dc gain, should be chosen as low as possible while adhering to step 5 in order to maximize the loop gain. Generally, a 20-Ω resistor serves as a good first iteration for output voltage V_{O1} less than 35-V. Later, when system stability is considered, the value of resistor R_B will be re-evaluated.

The design of components R_A, C_{ZCD}, and R_{ZCD} can be determined independently from steps 1-7 of Table 2. For example, the role of resistor R_A is to reduce power loss P_{IC1} of the phototransistor within optocoupler IC_1, where P_{IC1} is

$$P_{IC1} = V_{CE}i_e^{max} = \left(V_{O2} - i_e^{max}R_A - V_{Qbe}\right)i_e^{max} < \text{device power rating} \quad (10)$$

TABLE 2
STEP-BY-STEP DESIGN PROCEDURE

Step 1	Choose I_K^{max} based on TL431 current limits
Step 2	Determine i_e^{max} from Eq. 9
Step 3	Determine R_S from Eq. 6
Step 4	Determine resistor R_F from Eq. 7
Step 5	Determine resistor R_B from Eq. 5
Step 6	Check I_K^{min} from Eq. 8 to ensure within TL431 limits
Step 7	Check V_{KA}^{max} using Eq. 4 at $i_K = i_K^{min}$

The role of capacitor C_{ZCD} is to block dc current during start-up, allowing charge to be delivered from the input voltage through start-up resistor R_{ST} until switch S_1 turns on for the first time. Otherwise, capacitor C_{ZCD} merely delays the full turn-on of switch S_1 by increasing the length of time spent by switch S_1 in the constant-current region, which is undesirable from a power conversion efficiency point of view. Therefore, it is recommended that capacitor C_{ZCD} be set ten times greater than input capacitance C_{ISS}. Since capacitors C_{ZCD} and C_{ISS} form a voltage divider at the gate of switch S_1, steps should be taken to clamp the gate voltage with zener diode ZD_1 to avoid exceeding the terminal voltage rating. The role of resistor R_{ZCD} is to limit power P_{ZD1} dissipated by zener diode ZD_1,

$$R_{ZCD} = \frac{V_{IN}^{max}\left(N_{S2}/N_P\right) - V_{ZD1}}{P_{ZD1}}V_{ZD1} . \qquad (11)$$

Generally, voltage V_{O2} should be chosen high enough to drive switch S_1 into its ohmic region (e.g., $V_{O2} = 12$-V to 15-V is often sufficient).

The value of start-up resistor R_{ST} is limited by its power dissipation, since a high voltage (approximately equal to input voltage V_{IN}) is across it at all times. As a good rule of thumb, its power dissipation should be less than 1% of the converters maximum output power.

B. Compensation Calculations

Compensation components C_{EA1}, C_{EA2}, and R_{EA1} of error amplifier TL431 are determined so that the control loop achieves the desired regulation accuracy and dynamic response of the output voltage while maintaining an acceptable phase margin (typically $>45^o$) in the entire line and load range. Generally, a good regulation accuracy and fast transient response requires that closed loop T_1 has a high dc gain and high bandwidth. Typically, a dc gain of 20 to 60 dB is sufficient for good regulation accuracy, whereas a crossover frequency (f_C) of less than one-fourth of the minimum switching frequency is usually designed for.

The optimum compensation of the voltage control loop consists of an error amplifier with 2 poles and 1 zero. Error amplifier transfer function $G_{EA}(s)$, given in Table 1, can be realized with capacitors C_{EA1} and C_{EA2} and resistor R_{EA1}. For a desired crossover frequency f_C of loop T_1, the selection of compensation zero f_{zcomp1} should equal pole frequency f_{p1}^*,

and the selection of compensation pole f_{pcomp2} should be greater than $4f_C$, i.e., $f_{zcomp1}= f_{p1}^*$ and $f_{pcomp2} > 4f_C$. Using this criteria, compensation components C_{EA1}, C_{EA2}, and R_{EA1} are then expressed as

$$C_{EA1} = 0.73/2\pi f_C R_{d1} \ , \qquad (12)$$

$$R_{EA1} = 1/C_{EA1}s_{p1}^* \ , \qquad (13)$$

$$C_{EA2} = C_{EA1}/10 \ . \qquad (14)$$

The small-signal block diagram model was verified by comparing it to measurements made on a 5-V, 2-A self-oscillating flyback converter operating from a 400-V nominal dc voltage under full load conditions, as shown in Fig. 7. As can be seen, both the measured and calculated Bode plots show an excellent agreement up to one-tenth of the minimum switching frequency, i.e., up to 4 kHz, where the minimum switching frequency is equal to 40 kHz. Beyond one-tenth of the switching frequency, the compared phase plots are shown to diverge, possibly due to a right-half-plane RHP zero which is not described by either the small-signal model presented in Table 1, or by the small-signal model presented in [3].

III. SUMMARY

A detailed design-oriented steady-state analysis and a complete small-signal model of the self-oscillating flyback converter were presented. It was found that the steady-state operation of the converter can be described by eleven topological stages. Based on this analysis and the small-signal model, a step-by-step design procedure for a feedback control of the circuit was defined. This design procedure was verified on a 5-V/2-A, off-line experimental circuit. The measured and calculated loop gain of the experimental converter are in a very good agreement.

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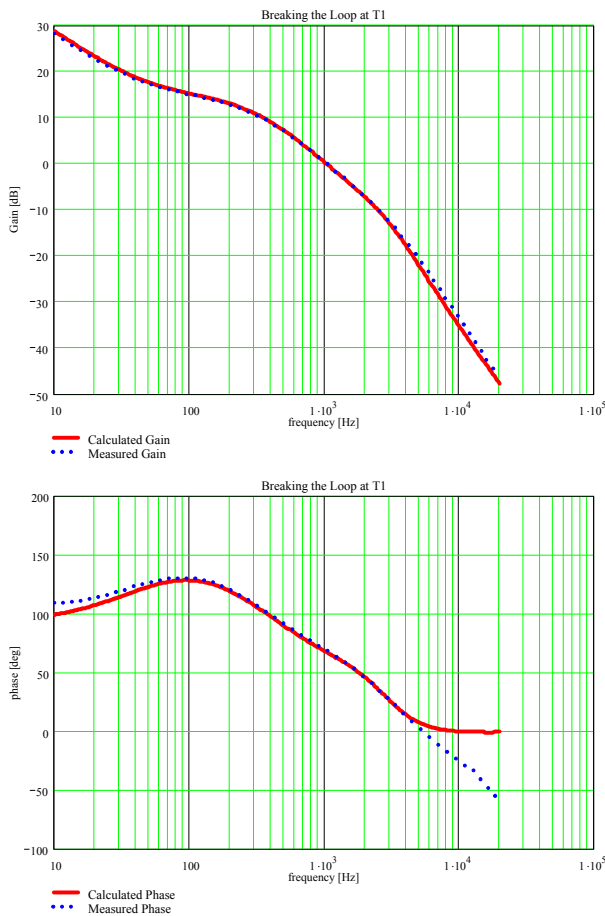
Fig. 7 Calculated and measured Bode plots of loop gain T_1 of off-line, 5-V/ 2-A self-oscillating flyback converter