Synchronous Rectifier for Low Voltage Switching Converter

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Abstract

A new self-driven MOSFET synchronous rectifier in a forward converter is presented. This topology is realized by adding only a few components to the conventional synchronous rectifier. MOSFETs are driven by the optimum waveforms and the operation is very simple. High efficiency has been achieved in an actual circuit. The efficiency is improved about 1.5% (5V, 10A) by the new configuration compared to the forward topology with active clamp technology.

Introduction

The number of IC systems that need power supplies with low output voltage, which is less than 5V, is gradually increasing. It is difficult for these power supplies to achieve high efficiency because of the power losses caused by offset voltage of Schottky diodes in the rectification stage. Therefore offset voltage drop of the rectifier should be reduced to obtain high efficiency. Self-driven synchronous rectifier has been proposed to solve this problem [1]. In this topology, two diodes in the rectification stage of a forward converter are replaced by two MOSFETs that have no offset voltage. Fig. 1 shows the self-driven synchronous rectifiers (*SRs*) in a forward converter with third winding reset scheme. The MOSFETs Q_2 and Q_3 are interconnected so that the gate-to-source voltage of one device is the same as the drain-to-source voltage of the other. MOSFETs are turned on and off by the voltage V_t in the secondary winding of the transformer. The advantage of this configuration is its simplicity to give gate-drive waveforms to MOSFETs. There are three states in one switching cycle of this topology as shown in Fig. 2. The operation is as follows. MOSFET Q_1 and Q_2 are turned on and Q_3 is turned off in State 1. MOSFET Q_1 and Q_2 are turned off in both states 2 and 3. The magnetizing energy of the transformer returns to the input through the third winding and the flyback voltage generates in the winding in State 2. MOSFET Q_3 is turned on by the flyback voltage in this state. However, the gate-drive voltage V_{gs3} of Q_3 becomes zero in State 3 because that the demagnetization of the core

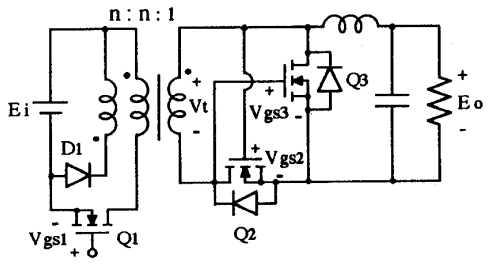

Fig. 1 Conventional self-driven *SR* in forward converter.

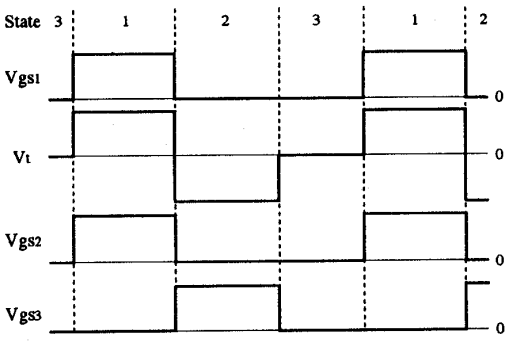

Fig. 2 Waveforms.

finishes at the end of State 2 and V_t becomes zero in State 3. As a result, the output current flows through the body diode of Q_3 in State 3. The high offset voltage drop and poor reverse recovery characteristics of the body diode deteriorate the efficiency of this converter. Therefore it is necessary to eliminate the interval of State 3, namely, dead time in this topology for increasing the efficiency of low voltage converters.

To solve this problem, the following forward topologies with synchronous rectifier have been proposed: Forward topology with Resonant Reset [2], Forward with multi-resonant switch [3], Forward PWM topology with active clamp technology (*FAC*) [4, 5, 6]. These topologies have been compared and it has been reported that *FAC* topology

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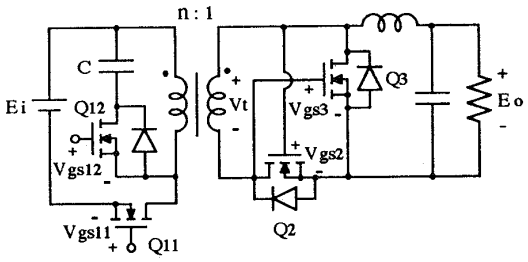


Fig. 3 *SR* in forward converter with active clamp technology.

is the best choice for the converter with constant switching frequency [7]. *FAC* topology is shown in Fig. 3.

The main switch Q_{11} is turned on when the auxiliary switch Q_{12} is turned off and vice versa. The transformer demagnetization is carried out over the clamp capacitor *C*. The energy stored in this capacitor is given back to the transformer through the auxiliary switch Q_{12}. The gate-drive waveforms V_{gs2} and V_{gs3} of this topology are shown in Fig. 4. By delaying the turn-off timing of Q_{12}, the interval of State 3 (dead time) in Fig. 4 can be made short compared with that of the conventional *SRs* in Fig. 2 [4, 5, 6]. In this case, however, the turn-on loss of the main switch Q_{11} increases. On the other hand, the turn-on gate voltage level of V_{gs3} has been expressed as follows by considering the voltage-second balance in the transformer [5]:

$$V_{gs3} \approx \frac{D E_i}{(1-D) n} \qquad (1)$$

where *D* is the turn-on duty ratio of the main switch and *n* is the turn ratio of the transformer. The interval of State 3 is eliminated in this equation for simplicity. It is seen from (1) that the turn-on gate voltage level of V_{gs3} varies according to the duty ratio *D* of the converter. On-resistance of MOSFET Q_3 will increase and make the efficiency worse unless enough gate-drive voltage is obtained. *FAC* topology also needs additional power of gate-drive for the auxiliary switch Q_{12}. For reasons mentioned above, this topology seems to be inadequate for improving the efficiency of low voltage converter.

For these subjects, we propose a forward topology with a new self-driven *SR* in this paper. New configuration only needs a few additional components and the operation is very simple. The gate-drive waveforms in this topology are almost ideal, therefore, high conversion efficiency is achieved. Practical circuits with new topology and *FAC* technology have been built and their efficiencies are compared.

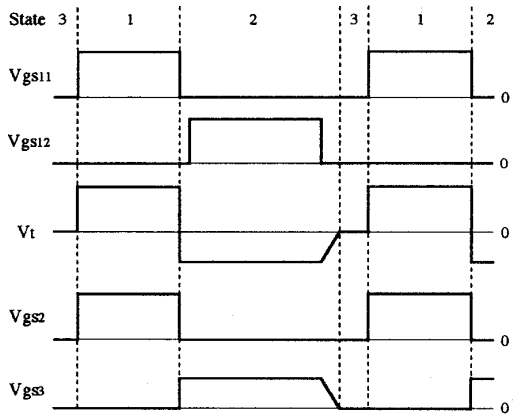


Fig. 4 Waveforms.

New Self-Driven Synchronous Rectifier

Fig. 5 shows a forward converter with the new self-driven *SR*. This configuration is based on the conventional self-driven *SR* as shown in Fig. 1. The purpose of the diode D_2, the MOSFET Q_4 and the saturable transformer T_2 in Fig. 5 is to drive MOSFET Q_3 properly. The key waveforms that define the circuit operation are represented in Fig. 6. There are four operating states in one switching cycle of this topology. The operation of this circuit is as follows. MOSFET Q_1 and Q_2 are turned on and Q_3 is turned off in State 1. The transformer T_2 is saturated due to the current in the primary during this interval. Therefore the gate-drive voltage V_{gs4} is zero and MOSFET Q_4 is turned off in this state. In State 2, MOSFET Q_1 and Q_2 are turned off and Q_3 is turned on because the flyback voltage V_t of the winding in the transformer T_1 becomes negative value and the parasitic input capacitance C_{iss} of MOSFET Q_3 is charged through diode D_2. In this state, transformer T_2 is not saturated and V_{gs4} becomes small negative value, therefore, Q_4 is still turned off. In State 3, V_t becomes zero because the reset operation of transformer T_1 is finished by the third winding at the end of State 2. In State 3, however, MOSFET Q_3 is still turned on because Q_4 is turned off and C_{iss} holds the charge to keep MOSFET Q_3 turned on. In State 4, Q_1 is turned on and the current flows rapidly in the primary winding of T_1 and T_2. By this current, the voltage is induced in the transformer T_2 and it makes V_{gs4} positive. Therefore MOSFET Q_4 is turned on in this state. The parasitic capacitance C_{iss} of MOSFET Q_3 is discharged through Q_4, and MOSFET Q_3 is quickly turned off. MOSFET Q_2 is also tuned on in this state. At the end of State 4, transformer T_2 is saturated and V_{gs4} becomes zero.

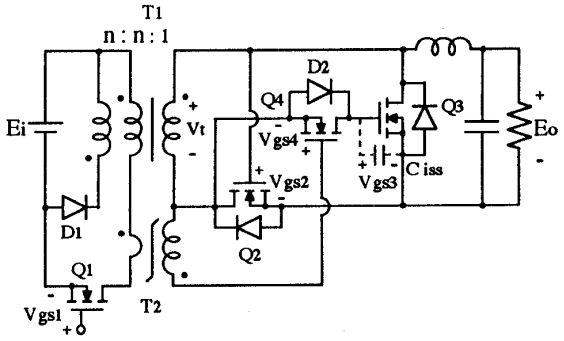


Fig. 5 New self-driven *SR* in forward converter.

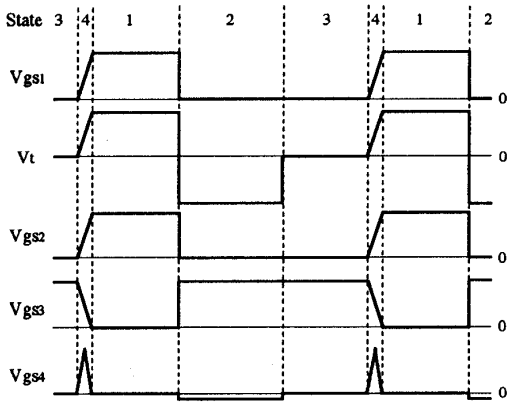


Fig. 6 Waveforms.

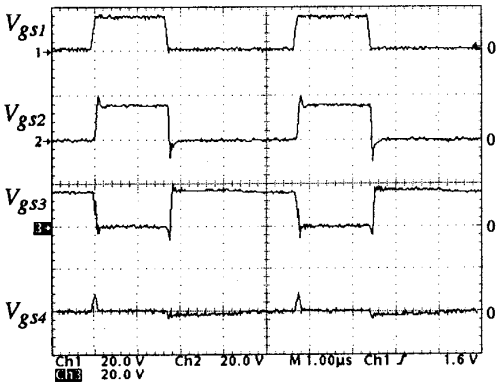


Fig. 7 Observed gate-drive waveforms of forward converter with new *SR* (20V/div, 1 µs/div).

The peak voltage of V_{gs4} in State 4 and the negative voltage of V_{gs4} in State 2 are determined by the voltage-second balance of the saturable transformer T_2.

The new configuration needs adding a few components to the conventional *SR*, however, the operation is very simple. The advantage of this topology is that the gate-drive waveforms for *SRs* are ideal and they have no dead time. Moreover, the turn-on voltage level is independent of the duty ratio of the converter. Therefore the design to achieve high efficiency is simple. The diode D_2 can be removed because MOSFET Q_4 has a body diode and it plays the same role as the additional diode D_2 does. However, the body diode has poor reverse recovery characteristic. Therefore it is desirable that a Schottky diode is used for D_2. MOSFET Q_4 , the diode D_2 and the saturable transformer T_2 do not need to have high power ratings because their purpose is only to charge and discharge the parasitic capacitance C_{iss} of MOSFET Q_3.

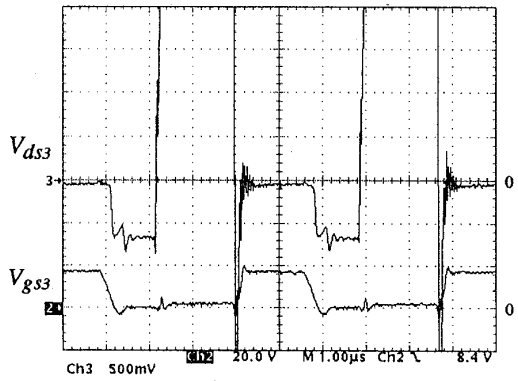
Experimental Results

Fig. 7 shows the observed gate-drive waveforms of the forward converter with new self-driven *SR*. It is seen from this figure that the waveform of V_{gs3} has no dead time and MOSFET Q_3 is driven properly.

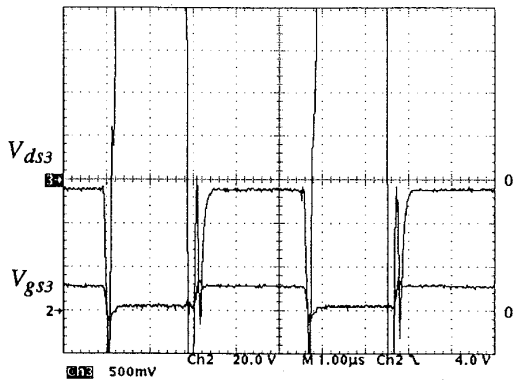
Three forward converters with different *SR* topology have been built and tested to compare the performance: *SR* with the proposed topology, *SR* with *FAC* topology and the conventional *SR* topology. Fig. 8 shows the way synchronous rectification works in these topologies under the same operating conditions for the frequency of 210 kHz and the output current of 10A. In each figure, the lower voltage is the gate-drive waveform V_{gs3} of MOSFET Q_3 and the upper one is the voltage drop V_{ds3} of MOSFET Q_3. The Fig. 8 (a) shows that V_{ds3} increases up to -700mV when V_{gs3} becomes zero because the body diode of the MOSFET Q_3 conducts in State 3 by using the conventional *SR* topology.

The Fig. 8 (b) shows that the voltage drop V_{ds3} of *FAC* topology is about -110mV in almost the turn-on interval for an output current of 10A. The voltage drop V_{ds3} is not sufficiently low because the gate turn-on voltage level is not high enough. As we have mentioned before, the gate turn-on voltage level of this topology varies according to the duty ratio. This figure also shows that the body diode of MOSFET Q_3 conducts for a short interval at the end of the turn-on time. This interval, namely, dead time is about 200ns in this figure. The dead time has to be introduced to avoid the undesirable short-circuit in this topology.

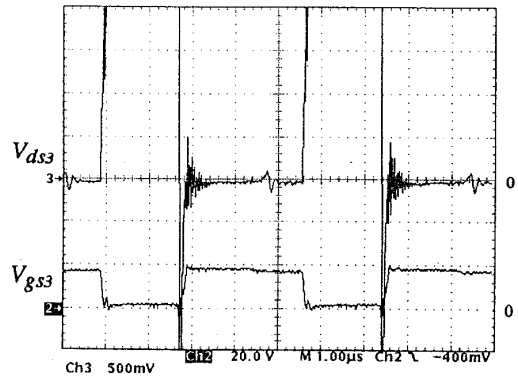
On the other hand, Fig. 8 (c) shows that the voltage drop V_{ds3} is about -50mV during the turn-on interval by the new *SR* topology. The gate turn-on voltage level of MOSFET Q_3



(a)



(b)



(c)

Fig. 8 Gate-drive waveform V_{gs3} (20V/div, 1µs/div) and voltage drop V_{ds3} (500mV/div, 1µs/div) in MOSFET Q_3. (a) with conventional *SR*. (b) with *FAC* topology. (c) with new *SR*.

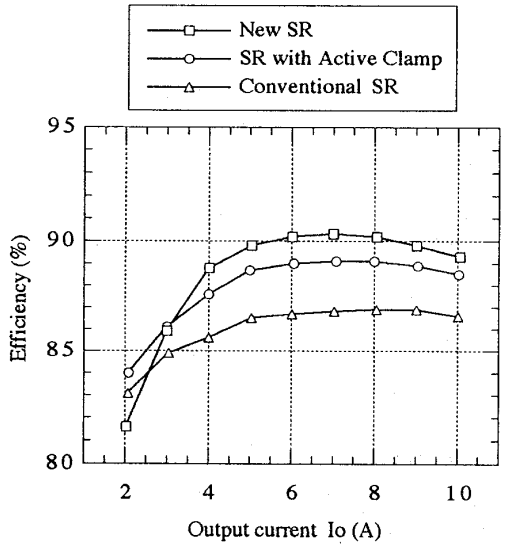


Fig. 9 Efficiency versus output current (Ei = 48V, Eo = 5V, Q_1, Q_{11}, Q_{12} : IRF640, Q_2, Q_3 : MTP75N05HD, Q_4: 2SK1719, n = 3).

is sufficiently high and it is independent of the duty ratio. Therefore V_{ds3} during the turn-on interval is very low. This figure also shows that no body diode of Q_3 conducts during the turn-on interval.

Fig. 9 shows the measured efficiencies versus output current of three forward converters with different *SR* topology of 210kHz, 48V input and 5V output. The loss of gate-drive and control circuit in the primary of the new *SR* topology is 0.15W, that of the conventional *SR* topology is the same value and that of *FAC* topology is 0.68W. The efficiencies are plotted in consideration of these losses in this figure. The dead time of *FAC* topology is made as short as possible to obtain high efficiency. It is seen from this figure that the efficiency of the forward converter with proposed *SR* topology is 1.5% higher than that of *FAC* topology. The efficiency of new *SR* topology is about 89% for the output current of 10A. The efficiencies are reversed when the output current is less than 3A. The reason seems to be the loss in the saturable transformer T_2. However, it seems to be no problem for a heavy load.

Conclusions

A new self-driven MOSFET synchronous rectifier in a forward converter has been presented. The configuration is realized by adding a few components to the conventional self-driven *SR* topology and the operation is very simple. In this topology, MOSFETs are driven by the ideal

waveforms, therefore, high efficiency (89%) has been obtained in an actual circuit (5V, 10A). About 1.5% efficiency improvement compared to *FAC* topology is achieved by the proposed circuit.

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