Input Filter Design for Multiple-Module DC Power Systems

Martin Florez-Lizarraga and Arthur F. Witulski

Abstract—**When multiple dc/dc converters are operated from a dc bus with a nonzero source impedance, undesirable interactions can occur between an individual regulator and the input impedance of the other regulators on the bus. Consequently, criteria for input filter design in the presence of a significant source impedance are developed, which, when used in conjunction with already-known input filter criteria, permit the input filter to be designed so that each regulator operates reliably. Proper filter design tends to decouple the negative regulator impedances from the bus, leaving only the passive input filter impedances to affect the other converters. These filter impedances appear in parallel with the source impedance and reduce the overall source impedance. Hence the use of multiple modules on the same bus actually improves the performance of the individual regulators. An example, the buck current mode controlled converter, is examined in detail. Extensive experimental evidence is presented to verify the analytical results.**

I. Introduction

CONVENTIONAL power supplies consist of an ac/dc converter followed by a dc/dc regulator that provides power to the load (Fig. 1). At low power levels, this arrangement works well. An input filter is generally required between the ac/dc converter and the dc/dc converter to prevent switching harmonics from propagating back to the power source. The effects of this input filter have been examined extensively, both for voltage-and current-mode control [1], [2]. In most cases the output impedance of the ac/dc source is assumed to be negligible. Since the dc/dc converter functions as a constant-power load to the dc bus, the input impedance can be negative over a given frequency range. Hence the primary concern is to design the output impedance Z_s of the input filter so that it does not degrade the stability of the feedback loops or the output impedance of the dc/dc regulator.

More complex electronic equipment often requires a different power system architecture, as shown in Fig. 2. A centralized ac/dc converter is still present, but multiple dc/dc modules are operated on the central dc power bus. Each dc/dc module requires its own input filter, which must be designed so that it does not interfere with the operation of the feedback loops and the regulation properties of the individual converter. However, the problem is more complicated than for a centralized architecture because the individual converters

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M. Florez-Lizarraga is with the International Power Systems, Carretera Internacional, Km. 6.5, Nogales, Sonora, Mexico.

A. F. Witulski is with the Dept. of Electrical and Comp. Eng., University of Arizona, Tucson, AZ 85721 USA.

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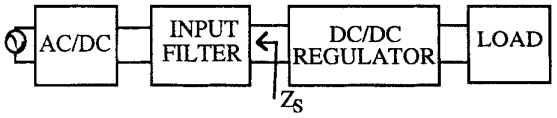

Fig. 1. Centralized power system architecture.

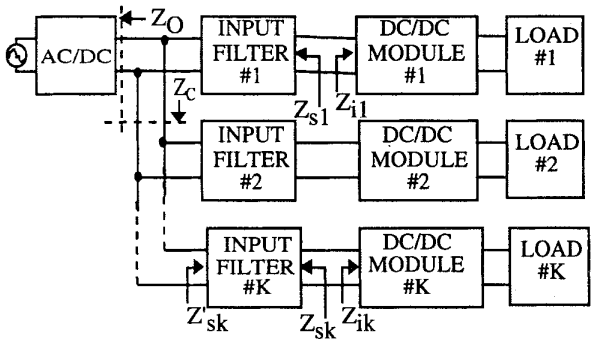

Fig. 2. Multiple-module dc power system.

"sees" not only the input filter output impedance Z_S, and the output impedance of the ac/dc converter, but also the input impedance of all the filter-regulator modules that operate on the central dc power bus. Since each of these dc modules presents a constant power load to the dc power bus, each one may have a negative impedance over some frequency range. Hence the possibility exists of reduced stability margins and degraded performance on each dc/dc regulator because of interactions with the input impedance of the other regulators on the bus. If the output impedance of the ac/dc converter were zero, the impedances of the other regulators would have no effect on the performance of each regulator module, but if the ac/dc converter output impedance is nonzero, the collective impedance of the other filter-regulator modules can be significant.

Consequently, to ensure the stable and effective operation of the entire power system, it is desirable to investigate the effects on an individual regulator of the output impedance Z_O of the ac/dc converter, and the effect of the cumulative input impedances of the other converters on the bus. From the standpoint of an individual dc/dc regulator, the input impedances of all the other regulators of the bus appear in parallel, and may be designated as the impedance Z_C, as shown in Figs. 2 and 3. If the modules are identical, then the analysis for one converter is equally valid for all other converters, i.e.,

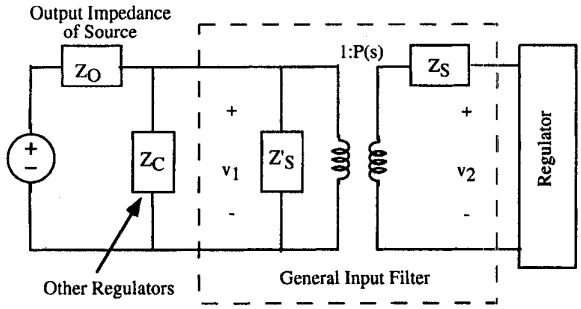

Fig. 3. AC/DC output impedance and cumulative regulator impedance as seen by an individual regulator.

each converter sees the same Z_O and Z_C. To analyze the stability of a dc/dc converter, the effect of an input filter, the output impedance Z_O, and the cumulative regulator impedance Z_C on an individual converter is examined. The input filter's two-port parameters and the Extra Element Theorem [3] will be used to find the effect of each of these impedances on a converter function $F(s)$. In previous work [4] the output impedance Z_O and the cumulative impedance Z_C of the other regulators connected to the dc bus are lumped together as part of the output impedance Z_S of the input filter. In this work each impedance is analyzed separately for design purposes. Design equations are derived which show the effect of each of these impedances in terms of the input filter and properties of the dc/dc converter. It is shown that the magnitude of the output impedance Z_O can be large and still not degrade the performance of the system. It is also shown that, if the input filter of the dc/dc converter is designed correctly, and the source impedance satisfies certain conditions, the negative impedances of the regulators are "decoupled" from the dc bus. Since the central dc power bus does not see the negative input impedance of the regulators, the impedance Z_C is simply a positive impedance in parallel with Z_O, thus reducing Z_O and actually improving the overall performance of the power system. Consequently, the presence of several converters on the bus is actually desirable. The more converters that are present, the more the individual converter performance is improved. These general results are applied to a buck current-mode converter, and extensive experimental verification of the results is presented.

II. Effects of Z_S, Z_O, Z_C on DC/DC Regulator Properties

The analysis is organized in the following manner: First, the effect of a general input filter operating from an ideal bus on a converter transfer function $F(s)$ is analyzed in terms of the filter two-port parameters and the Extra Element Theorem [3]. Second, the effect of the filter in the presence of the output impedance Z_O of the ac/dc converter is analyzed. Third, the effect of the filter in the presence of Z_O and the collective impedance Z_C of the other regulators is analyzed. In each case inequalities in terms of the input filter and converter impedances are derived which permit the undisturbed operation of the regulator.

A. Effect of Input Filter Output Impedance, Z_S

First, the input filter is characterized using the two-port parameters (with $Z_O = 0$ and $Z_C = \infty$), this keeps the analysis general and independent of specific filter topology. Application of the two-port parameters to the general filter shown in Fig. 3 yields

$$\begin{aligned} h_{11} &= \left.\frac{i_1}{v_1}\right|_{i_2=0} \\ &= \frac{1}{Z'_S} \\ h_{21} &= \left.\frac{v_2}{v_1}\right|_{i_2=0} \\ &= P(s) \qquad (1) \\ h_{22} &= \left.\frac{v_2}{i_2}\right|_{v_1=0} \\ &= Z_S \\ h_{12} &= \left.\frac{i_1}{v_1}\right|_{v_1=0} \\ &= h_{21} \\ &= P(s) \qquad (2) \end{aligned}$$

where Z_S is the filter output impedance, Z'_S is the input impedance, $P(s)$ is the forward transfer function. The term h_{12} is equal to h_{21} because the input filter is assumed to be entirely passive so that the reciprocity theorem applies. Hence the filter can be modeled as an ideal transformer with turns ratio $1 : P(s)$, together with a shunt impedance Z'_S on the primary side and a series impedance Z_S on the secondary side. By means of the Extra Element Theorem [3], the effect of the filter itself ($Z_O = 0$, $Z_C = \infty$) on any transfer function $F(s)$ of the regulator (Fig. 3), such as loop gain or output impedance, is given by

$$F'(s) = F(s)\frac{1+\dfrac{Z_S}{Z_n}}{1+\dfrac{Z_S}{Z_d}} \qquad (3)$$

where Z_n is the impedance at the regulator input port when the output is nulled, Z_d the impedance when the input voltage is shorted, and Z_S is the output impedance of the filter. Clearly, $F(s)$ is unaltered if the following conditions are satisfied

$$|Z_S| \ll |Z_n| \qquad (4)$$

$$|Z_S| \ll |Z_d|. \qquad (5)$$

These conditions have been reported in the previous literature [1], [2], [5], and [6] for both voltage-and current-mode control.

B. Effect of Source Impedance, Z_O

When the output impedance of the ac/dc converter is now included ($Z_O \neq 0$, $Z_C = \infty$), the expression for the new transfer function can be found by another application of the Extra Element Theorem to find the effect of Z_O when the

input filter is already present

$$F(s) = F(s)\frac{1+\dfrac{Z_S}{Z_n}}{1+\dfrac{Z_S}{Z_d}} \cdot \frac{1+\dfrac{Z_O}{Z'_S \left|\left| \dfrac{Z_S+Z_n}{P^2}\right.\right.}}{1+\dfrac{Z_O}{Z'_S \left|\left| \dfrac{Z_S+Z_d}{P^2}\right.\right.}}. \tag{6}$$

If conditions (4) and (5) are already satisfied by the filter design, then the criteria for not modifying the function $F(s)$ in (6) can be written

$$|Z_O| \ll \left| Z'_S \left|\left| \frac{Z_S+Z_n}{P^2}\right.\right.\right| \tag{7}$$

$$|Z_O| \ll \left| Z'_S \left|\left| \frac{Z_S+Z_d}{P^2}\right.\right.\right|. \tag{8}$$

Here Z_n and Z_d are properties of the dc/dc regulator for the transfer function under consideration, and Z'_S, P, and Z'_S are properties of the input filter. Consequently, these equations put constraints on the allowable magnitude of the output impedance Z_O if the input filter and regulator are already designed.

C. Effect of Collective Input Impedance Z_C

Finally, when the effect of the other regulators is included ($Z_O \neq 0$, $Z_C \neq \infty$), the application of the extra element theorem to find the effect of Z_C in the presence of the input filter and Z_O yields the following expression:

$$F'(s) = F(s)\frac{1+\dfrac{Z_S}{Z_n}}{1+\dfrac{Z_S}{Z_d}} \cdot \frac{1+\dfrac{Z_O}{Z'_S \left|\left| \dfrac{Z_S+Z_n}{P^2}\right.\right.}}{1+\dfrac{Z_O}{Z'_S \left|\left| \dfrac{Z_S+Z_d}{P^2}\right.\right.}} \cdot \frac{1+\dfrac{Z_O||Z'_S \left|\left| \dfrac{Z_S+Z_n}{P^2}\right.\right.}{Z_C}}{1+\dfrac{Z_O||Z'_S \left|\left| \dfrac{Z_S+Z_d}{P^2}\right.\right.}{Z_C}}. \tag{9}$$

The extreme cases occur when $Z_C \to \infty$ and (9) reduces to (6), and when $Z_C \to 0$, in which case the impedance Z_C shorts out the impedance Z_O, and (9) reduces to (3).

III. Examination of the Collective Regulator Input Impedance, Z_C

Now that an expression determining the effect of Z_C on a multiple-module system has been found, an expression relating Z_C to the filter parameters and converter input impedance is required. Since Z_C is the impedance sum of all the regulators connected to the same bus, an expression for each individual converter is required. Two cases are possible: the case in which the converters are all identical and share a common load (converters are operating in parallel), and the case in which each individual converter could be different and have a different load. In general, the impedance Z_{ik} is the input impedance for an individual regulator (Fig. 2), and each regulator could have a different input filter Z_{sk} connected. The collective impedance Z_C for a system of k converters can be written as the parallel combination of the impedances "seen" looking into the input terminals of each input filter

$$Z_C = \left[Z'_{S1} \left|\left| \frac{Z_{S1}+Z_{i1}}{P_1^2}\right.\right.\right] \left|\left| \left[Z'_{S2} \left|\left| \frac{Z_{S2}+Z_{i2}}{P_2^2}\right.\right.\right] \right|\right| \cdots \left|\left| \left[Z'_{S(k-1)} \left|\left| \frac{Z_{S(k-1)}+Z_{i(k-1)}}{P_{(k-1)}^2}\right.\right.\right] \right|\right|. \tag{10}$$

In a well-designed dc/dc converter, the output impedance of the input filter is chosen much less than the input impedance of each individual regulator

$$|Z_{Sm}| \ll |Z_{im}|. \tag{11}$$

Consequently the input impedance for each regulator will be positive if the parallel combination of Z'_{sm} and Z_{im}/P_m^2 is a positive quantity, or

$$|Z'_{Sm}| \ll \left| \frac{Z_{im}}{P_m^2}\right|. \tag{12}$$

If (12) is satisfied for each individual converter, then the collective impedance Z_C in (10) will be a positive impedance. In this case Z_C can be viewed as simply a positive impedance in parallel with Z_O, so if the conditions for Z_O are satisfied (7) and (8) then the addition of Z_C actually even improves the inequalities (7) and (8) because the magnitude of the parallel combination of Z_O and Z_C is smaller than the magnitude of Z_O. If the inequality (12) is violated for one or more converters, then the total impedance Z_C may be negative. Consequently the Z_C term in (9) must be evaluated as a "loop gain" using the Nyquist criterion to determine stability of the system, remembering to apply the complete Nyquist criterion because of the possibility of roots in the right half plane. If all the filter converter modules are the same with separate loads, (10) can be simplified to

$$Z_C = \frac{1}{k-1}\left[Z'_S \left|\left| \frac{Z_S+Z_i}{P^2}\right.\right.\right] \tag{13}$$

[If the converters share the same load, the factor in front is $k/(k-1)$ instead of $1/(k-1)$.] In the event that converters are different, a suitable approximation for (10) can be found, especially if the converters operate with approximately the same switching frequency and hence require approximately the same filter cut-off frequency, in which case (13) can be used as an approximate expression for Z_C.

IV. Application of Design Criteria to Current- and Voltage-Mode Buck Converters

In the last section expressions were found which show the effect of Z_O and Z_C on a converter function $F(s)$ in general. Now, these expressions are applied to both current-

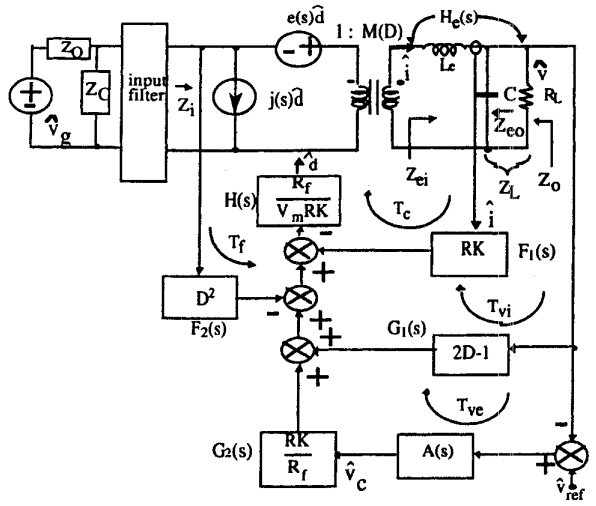

Fig. 4. Small-signal model of buck current mode controlled converter.

and voltage-mode buck converters. A small signal model of the buck converter with the feedback loops arising from current-mode control is shown in Fig. 4 [2], [8]. In the current-mode case, the addition of Z_O and Z_C must not modify the inner loop voltage loop T_{vi}, the current loop T_c, the feedforward loop gain T_f, the external voltage loop T_{ve}, or the output impedance of the regulator [2], as shown in Fig. 4. The impedances Z_n and Z_d must be found individually for each converter topology and loop gain. Specific values for Z_n and Z_d are given for the loop gains T_c and T_f in this paper. These loops are the main cause of instability [2]. Values for other transfer functions and loop gains for current and voltage mode are given in [7]. The necessary parameters to evaluate Z_n and Z_d are shown in Fig. 4. The conduction parameter is defined as $K = 2L/RT_s$. The value of R_s represents the current sense resistance. The value N is the current sense amplifier gain. The value V_m represents the peak voltage of the compensating ramp. The converter effective low-pass filter has an input impedance Z_{ei} and output impedance Z_{eo} at the ports indicated under open loop conditions. The impedance Z_L is the parallel combination of the resistor R and the capacitor C. The impedance Z_i and Z_O are the closed loop regulator input and output impedances, respectively. The converter low-pass filter is defined to have a voltage transfer function $H_e(s)$ under open-loop conditions in the presence of the external load R. The buck parameters are defined as $L_e = L$, $M(D) = D$, $e(s) = V/D^2$ and $j(s) = V/R$. Also, the quantity $A(s)$ is the gain of the error amplifier when the converter is operated in the closed loop configuration. As shown in Fig. 4, the gain $F_1(s)$ is equal to RK. The quantity $G_2(s)$ is equal to RK/R_f. The quantity $F_2(s)$ is equal to D^2. The parameter $G_1(s)$ and $H(s)$ are equal to $2D - 1$ and R_f/V_mRK respectively, and $R_f = nR_s$. The small signal model of a voltage-mode controlled converter is obtained from Fig. 4 by setting the gains $F_1(s)$, $F_2(s)$, and $G_1(s)$ to zero, in which case only the external voltage loop $T_{ve}(s)$ remains.

Instead of deriving the effect of Z_O and Z_C on all system transfer functions, only those loops which are known to be the cause of instability, are discussed below. As [2] shows, the loops gains of an initially stable current-mode converter are not modified by the addition of an input filter if the following conditions are met:

$$|Z_s| \ll |Z_{dc}| \tag{14}$$

$$|Z_s| \ll |Z_{nc}| \tag{15}$$

$$|Z_s| \ll |Z_{nf}| \tag{16}$$

where the impedances are defined for the buck current-mode converter

$$Z_{dc} = \frac{Z_{ei}}{M^2} \tag{17}$$

$$Z_{nc} = \frac{-R}{D^2} \tag{18}$$

$$Z_{nf} = \frac{RK}{D^3} \cdot \frac{R||Z_{ei}}{\dfrac{R_f V}{V_M D}\Big|\Big|Z_{ei}}. \tag{19}$$

The impedance Z_{ei} is the reflected converter filter impedance. The impedance Z_{nc} is the closed-loop low-frequency incremental input resistance and Z_{nf} is the impedance at the converter's input when the output to the feedforward loop is nulled. The conditions (14)–(16) are relationships found by [1], [2] and are required for stability and undisturbed performance in the presence of an input filter and a zero source impedance.

The conditions (14) and (15) are required for voltage-mode and (14)–(16) are required for current-mode. One further constraint is required for both voltage and current mode, the output impedance condition. For nondegradation of the close-loop impedance the following condition must be met:

$$|Z_s| \ll \left|\frac{R_e + sL_e}{M^2}\right|. \tag{20}$$

Three new conditions are found from (9), (10) when the source impedance is nonzero to prevent instability of the current and voltage loops

$$|Z_O| \ll \left|Z_S'\right|\left|\frac{Z_{nc}}{P^2}\right| \tag{21}$$

$$|Z_O| \ll \left|Z_S'\right|\left|\frac{Z_{dc}}{P^2}\right| \tag{22}$$

$$|Z_O| \ll \left|Z_S'\right|\left|\frac{Z_{nf}}{P^2}\right|. \tag{23}$$

As before, the first two conditions apply to voltage-mode and all three apply to current-mode. The new conditions also put a constraint on the magnitude of the source impedance. Also, an addition condition is required to avoid degradation of the output closed-loop impedance

$$|Z_O| \ll \left|Z_S'\right|\left|\frac{Z_{Li}}{P^2}\right| \tag{24}$$

where the quantity Z_{ei} is given by

$$Z_{Li} = \frac{R_e + sL_e}{M^2}. \tag{25}$$

If conditions (14)–(16), (21)–(23) are satisfied, then the addition of Z_C, which represents the total collective impedance of

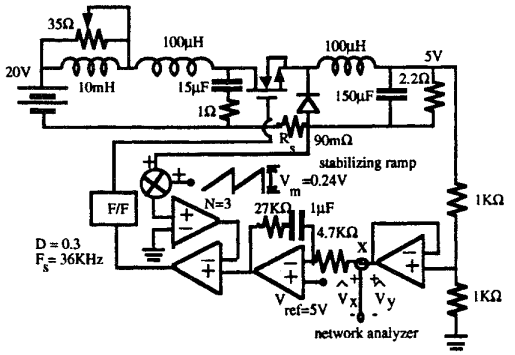

Fig. 5. Buck current-mode regulator.

other regulators operating off the same bus, has no effect on the converter. This occurs because Z_C decreases the impedance at the source terminals and because Z_C depends on the filter's passive impedances.

V. Experimental Results

In this section two buck current-mode converters operating at identical conditions are constructed to validate (21)–(24). The effect of different values of source impedance is observed on the external loop T_{ve}. Theoretical plots of loop gain T_{ve} for different values of source impedance are found to be in agreement with experimental data. The effect of Z_C is shown to improve the loop gain T_{ve}.

A. Design of Test Circuit

The schematic for one of the two continuous-inductor-current-mode buck current-controlled converters built for validating the theory is shown in Fig. 5. The input voltage is 20 V. The output voltage is 5 V. The duty cycle D is 0.3. The load resistance is $R = 2.2\,\Omega$ and is resistive to all frequencies of the measurement. The switching frequency is $f_s = 36$ kHz, for a switching period of $T_s = 27.8\,\mu$sec. A peak ramp V_m of value 240 mV was used. The conduction parameter $K = 2L/RT_s$ is 3.27. A current sense transformer with a ratio of 40 to 1 was used to sense the current. An equivalent current sense resistance R_s of 110 mΩ was measured. The Unitrode UC1846 PWM current-mode chip was used in these experiments. A gain of $N = 3$ was applied at the current sensor amplifier before comparison with the control signal from the error amplifier. The effective resistance R_f is $NR_s = 330$ mΩ. The output inductor had a value of 100 μH. The output capacitor was a 150 μF electrolytic with 0.1 Ω of equivalent series resistance.

B. Input Filter

The input filter was designed to meet the conditions (14)–(16). The input filter is an LC filter with series resistance to dampen the Q of the filter as shown in Fig. 5. The inductor was a 100 μH pot-core inductor. The filter capacitor was a 15 μF high frequency electrolytic capacitor. A 1 resistor was connected in series with the capacitor to meet the required specifications. The output impedance of the input filter with

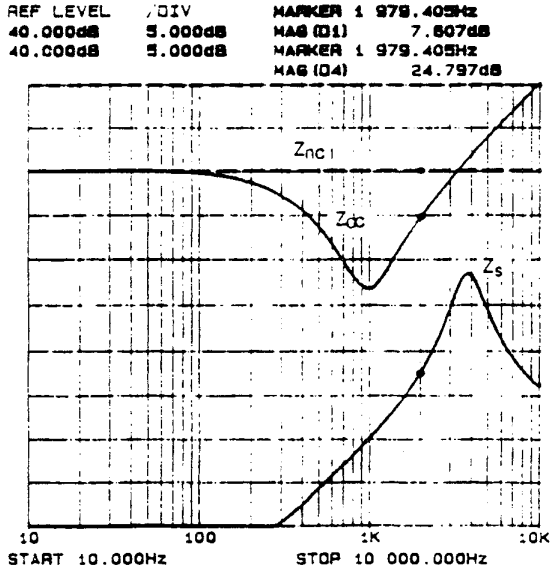

Fig. 6. Input filter output impedance Z_s with $Z_O = 0$ and $Z_C = \infty$.

$Z_O = 0$ and $Z_C = \infty$ is shown in Fig. 6 and the plot clearly shows that all specifications for stability are met.

C. Source Impedance

The impedance of the source was simulated by an inductor in parallel with a variable resistor as shown in Fig. 5. The goal was to violate conditions (21)–(23) and verify that even though the input conditions (14)–(16) are met the source impedance conditions may not be satisfied. The source inductor had a measured inductance of 10 mH. The resistance R_o was a 35 Ω variable wire-wound resistor and determined the maximum value of the source impedance. The impedance of the wire-wound resistor was resistive between the frequencies of measurement.

D. Loop Gain Measurements

The external voltage loop gain was measured using the HP 3577A Network Analyzer. To measure the voltage loop gain a current probe was used to inject a signal at point **X** as shown in Fig. 5. The voltage ratio on each side of the voltage probe is defined as the voltage loop gain $T_{ve} = -\hat{v}_y/\hat{v}_x$. The measured voltage loop gain with the source impedance negligible and an input filter which does not degrade performance is shown in Fig. 7. Using these values the theoretical voltage loop gain is

$$T_{ve} \approx \frac{R_O}{R_f} A(s) \frac{1}{1 + \dfrac{s}{\omega_1}}. \tag{26}$$

The measured gain of the error amp is $A(s)$ =2.77 V/V. Evaluating (26) with the values $R_O = 2.2\,\Omega$, $R_f = NR_s$, N =3, $R_s \approx 110\,\text{m}\Omega$, $\omega_1 = 1/R_oC_O$, $C_O = 150\,\mu$F gives the following equation:

$$T_{ve} \approx 18.2 \frac{1}{1 + \dfrac{s}{2\pi \cdot 483}}. \tag{27}$$

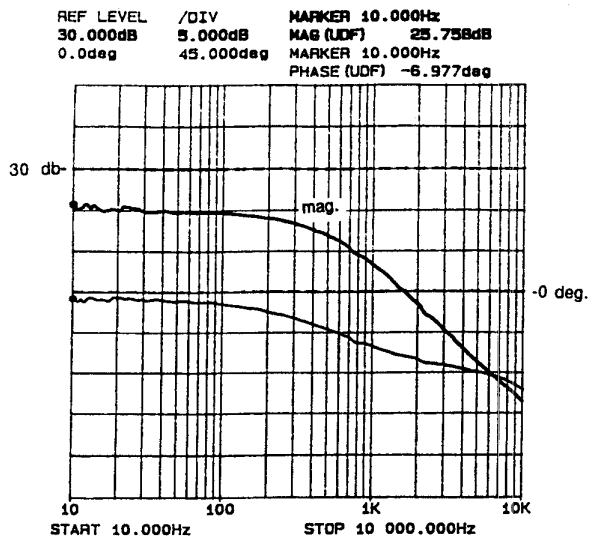

Fig. 7. Measured loop gain T_{ve} with $Z_O = 0$ and $Z_C = \infty$.

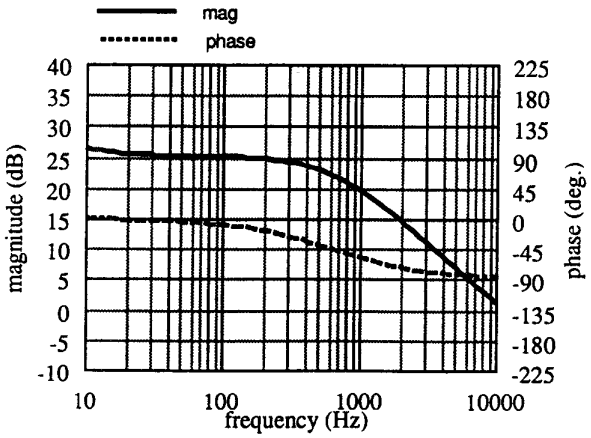

Fig. 8. Theoretical loop gain T_{ve} with $Z_O = 0$ and $Z_C = \infty$.

The other pole is at a very high frequency and out of the measurement range (10 Hz to 10 kHz). The theoretical plot using (26) is shown in Fig. 8. The theoretical and experimental plots are in excellent agreement.

E. Loop Gain for Nonzero Source

The voltage loop gain was measured for various values of source resistance R_o. The values of 10, 15, 20, and 25 Ω were used. Only the resistance value of 25 Ω made the test circuit unstable. The other values degraded the performance. Figs. 9 and 10 show the measured voltage loop gains degraded for different values of source impedance. The voltage loop gain with a nonzero source and a input filter satisfying the conditions (14)–(16) is

$$T_{ve} \approx T_{ve} \frac{1 + \dfrac{Z_O}{Z'_S \left\| \dfrac{Z_{ne}}{P^2} \right.}}{1 + \dfrac{Z_O}{Z'_S \left\| \dfrac{Z_{de}}{P^2} \right.}} \tag{28}$$

inserting the values for Z_O and the input filter gives

$$T'_{ve} \approx T_{ve} \left[\frac{s^2(L_o C_A) + s\left(\dfrac{L_o}{R_o} + \dfrac{L_o}{Z_{ne}}\right) + 1}{s^2(L_o C_A) + s\left(\dfrac{L_o}{R_o} + \dfrac{L_o}{Z_{de}}\right) + 1} \right] \tag{29}$$

where $L_o = 10$ mH is the source impedance inductance. The quantity R_o is the source resistance which is being varied between 10–25 Ω. The quantity C_A is the input filter capacitor which is 15 μF. The quantity Z_{ne} is the low frequency incremental input resistance of the closed loop regulator which is $-R/D^2$. The impedance Z_{de} is resistive in this frequency range and is equal to $-1.3R/D^2$. Substitution of these values

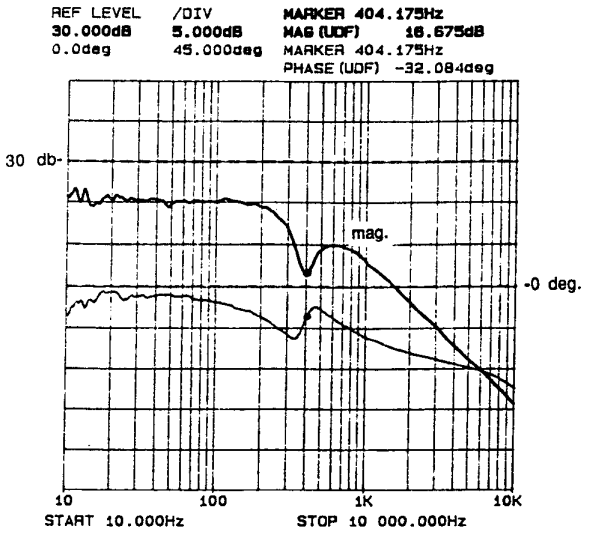

Fig. 9. Measured T_{ve} with $R_o = 20\,\Omega\,(Z_C = \infty)$.

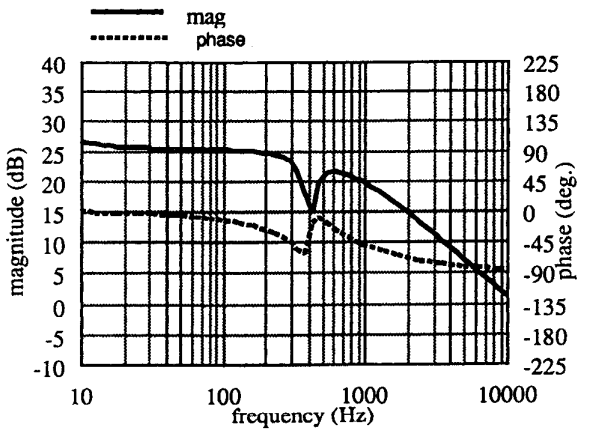

Fig. 10. Theoretical T_{ve} with $R_o = 20\,\Omega\,(Z_C = \infty)$.

into (29) gives the value when the loop will start to oscillate. When R_o is equal to Z_{de} the loop oscillates with a resonant

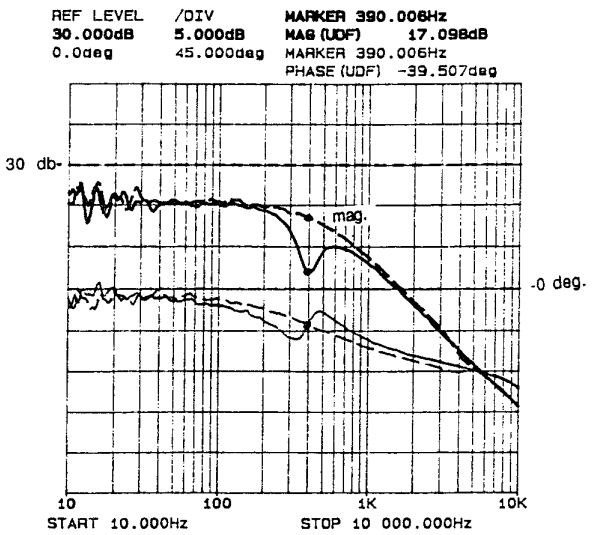

Fig. 11. Improvement in loop gain (dashed) when $R_o = 20\,\Omega$ and another current-mode regulator is operated on the same bus.

frequency equal to $\omega_0 = 1/\sqrt{L_o C_A}$ at a predicted resistance of $R_o = 31.8\,\Omega$. The resonant frequency where oscillation occurs is 410.9 Hz. These values are in agreement with the experimental data, although the damping was so small at values of R_o close to Z_{de} that oscillations were observed with R_o as low as 25 Ω. Figs. 10 and 11 show the theoretical and experimental plots of T_{ve} when the source resistance R_0 is 20 Ω. Larger values of R_0 result in progressively deeper dips in the gain and phase until instability is obtained.

F. Loop Gain for Finite Collective Impedance

It has been shown that if the input filter is designed correctly the load is decoupled and the impedance Z_C can be approximated as the impedance of the input filter Z'_S unloaded. If this impedance is a positive quantity, Z_C does not degrade the converter but improves it by making the source impedance smaller than it already is. Fig. 11 shows the improvement of the loop gain when another current-mode regulator is connected to the dc bus in parallel with the first regulator.

VI. Conclusion

To find the effect of the ac/dc converter output impedance Z_O and the cumulative impedance Z_C of the other regulators connected to the same bus, The Extra Element Theorem [3] is applied to a multiple dc/dc converter network. General design equations (9), (10) are discovered which put quantitative bounds on the allowable magnitude of the ac/dc converter output impedance Z_O for undisturbed operation of the dc/dc converter. It is discovered that if the well-known equations for good input filter design (17)–(19) are satisfied, the regulator negative impedance is approximately decoupled from the dc bus, leaving only the passive impedance of the input filter. Hence the cumulative impedance of all the dc/dc regulators Z_C is a *positive* impedance in a well-designed system. The presence of multiple converters on the same bus can improve the overall performance of the multiple-module system, because the positive impedance Z_C appears in parallel with the source impedance Z_O, thus reducing Z_O. These general results are applied to a small-signal canonical model of the buck current-mode regulator. A buck current-mode regulator is built to verify (24)–(26), which are the bounds on Z_O derived from (9) and (10) specifically for a buck current mode regulator. The source impedance is varied to violate (24)–(26) even though the input filter satisfies (17)–(19). For values of source impedance Z_O close in magnitude to Z_{nc}, the closed-loop low-frequency incremental resistance and Z_{dc}, the reflected converter impedance, the loop is degraded. When (25) is violated (the more stringent condition), the regulator starts to oscillate and to become unstable. The frequency of oscillation is theoretically predicted and agrees with the measured frequency. The loop gain T_{ve} measured for different values of source impedance is in agreement with the theoretical loop gain calculated. Experimental verification is presented which shows the improvement in loop gain T_{ve} when another regulator is connected to the source. A surprisingly large source impedance can be allowed without violating (24)–(26), which relaxes the constraint on the output impedance of the ac/dc source converter. The power supply designer now has (24)–(26) for not over-designing an ac/dc source. If the input filter is designed according to (17)–(19), and the output impedance Z_O of the ac/dc converter satisfies (24)–(26), the designer need not worry about the other regulators in a multiple module systems because of the "decoupling" effect.

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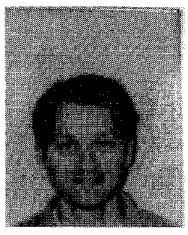

Martin Florez-Lizarraga was born in Nogales, Sonora, Mexico. He obtained the B.S. degree in electrical and computer engineering in 1986 and the M.S. degree in ECE in 1991, both from the University of Arizona.

He is currently a Product Development Engineer at International Power Systems, a division of C&D Corporation. His interests are in simulation and analysis of analog power systems, and design of microcontroller based power converters.

Arthur F. Witulski obtained the B.S., M.S., and Ph.D. degrees in electrical engineering from the University of Colorado, Boulder, in 1981, 1986, and 1988, respectively.

He has worked as a Design Engineer and Product Engineer at a major manufacturer in the area of power supply design for large magnetic data storage subsystems. He is currently an Associate Professor at the University of Arizona in the Department of Electrical and Computer Engineering. He is author or co-author of a number of publications on resonant, quasiresonant, and pulse-width modulated switching converters. His research interests are in resonant power conversion, distributed electronic power systems, high power factor rectification, modeling of magnetic components, and integration of power converters for on-chip or multichip-module power processing.