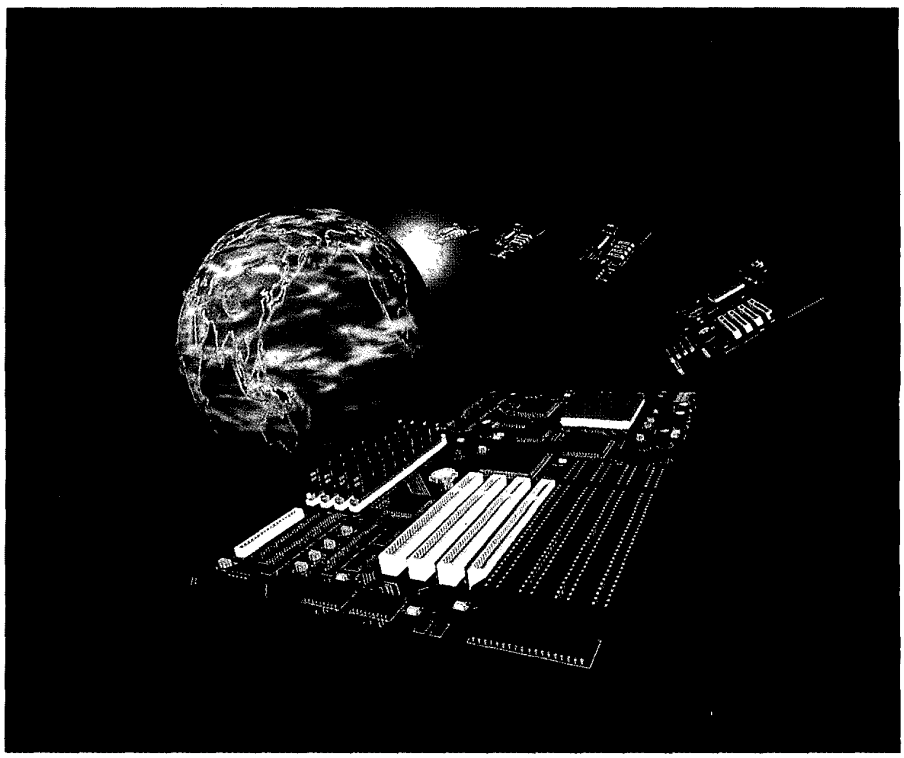
Daniel M. Mitchell

Power Line Filter Design Considerations

For dc-dc Converters



It is well known that modern electronic systems exhibit an increased use of microelectronic circuitry for reduced size and weight, as well as for increased performance and functionality. Perhaps less well known is the fact that these systems exhibit a corresponding increased use of, and dependency upon, the dc-dc converters that supply them. The dc output voltage of these converters continues to decrease in accordance with the complexity and geometry of the microcircuits themselves. There will likely be legacy 5 V dc requirements for the foreseeable future. However, there is a definite shift toward 3.3 V dc, there is already movement toward 2.2 and 1.5 V dc and, as

Mitchell (104535.1737@compuserve.com) is with DM Mitchell Consultants of Cedar Rapids, Iowa. He is a Senior Member of the IEEE. *Some of the material in this article was presented as a tutorial at the 1997 Power Conditioning Specialists Conference.*

1077-2618/99/$10.00©1999 IEEE

microelectronic geometry approaches 0.1 microns, we are likely to see dc voltage requirements of less than one volt in the not too distant future.

Especially because of the pulsed nature of typical microelectronic loads, where the power requirement of a microprocessor can jump from less than one watt to over ten watts in just a few hundred nanoseconds, it is not feasible to supply these lower voltages using a remote, centralized power supply. Instead, a distributed power system architecture, in which there are one or more "point-of-load" dc-dc converters per circuit card, is required. Typical dc-dc converter input voltage amplitudes are 28 V dc and 48 V dc, which are standard voltages for military and telecommunications systems, respectively. For modern systems with ac inputs, the power is normally first converted to a relatively high dc voltage (400 V dc for 230 V rms input, for example), often including active power factor correction. This input ac-dc converter is then followed by an intermediate, transformer-isolated, bulk dc-dc converter, which provides the lower input voltage for the "on-card" dc-dc converters. With this approach, the size of the transformer is governed by the dc-dc converter switching frequency rather than the ac line frequency, resulting in a much lighter weight system. The input ac-dc and intermediate dc-dc converters may require redundancy and/or battery backup, depending upon the criticality of the application.

DC-DC Converters Cause Interference

The switching regulators that are used in these high-efficiency dc-dc converters are notorious for generating current related interference at their inputs and voltage related interference at their outputs. Flyback and buck (Fig. 1) topologies are particularly bad for noisy input currents, since a semiconductor switch is directly in series with the input power line. Other topologies, such as the boost, SEPIC and Cuk converters [1], inherently produce less input noise, but are not always applicable for other reasons.

Output filters are used to smooth the switched output voltage waveforms to levels that can be tolerated by the load circuitry. The output filter necessarily creates phase shift and is a major influence in the design of the switching regulator feedback control circuitry that is used to assure stability, while still meeting performance requirements. Similarly, power line input filters are needed to attenuate the switched input current waveform sufficiently to prevent electromagnetic interference (EMI) problems and to assure electromagnetic compatibility (EMC) within the given system and/or with neighboring systems. As will be discussed in more detail, the power line input filter can also significantly affect the stability and performance of a dc-dc converter.

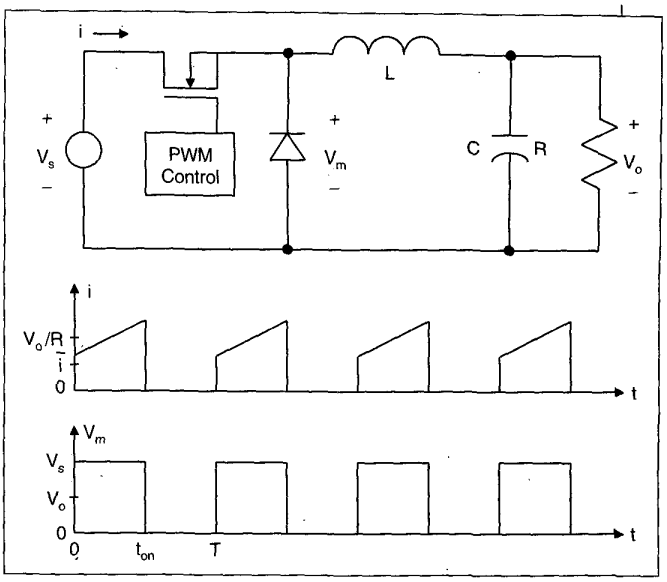


Fig. 1. Buck topology switching regulator.

Interference that is emitted by dc-dc converters can be either conducted or radiated. Power line conducted emissions, in conjunction with finite source impedance, can cause degradation in systems that operate from a common power bus. Degradation can also occur in systems that are in close enough proximity to detect the radiated emissions. Radiated emissions can be in the form of either electric or magnetic fields. Because of the relatively low voltages and high currents involved, magnetic field emissions are typically a larger dc-dc converter EMI problem in practice, although electric fields from the dc-dc converter power circuitry may cause localized EMC problems (especially to its own control circuitry!). Good physical layouts are always important and some shielding may ultimately be necessary to meet radiated emission specifications. Nevertheless, the greatest source of radiated emissions is often the conducted emissions on the input power line. To that extent, the power line filter serves a dual purpose.

Conducted emissions can be either differential mode or common mode. Differential mode emissions include the basic switching current waveform and harmonics thereof, as well as periodic current "spikes" at the switching frequency. These spikes are generally coincident with the turn-on of a power semiconductor, and are caused by phenomena such as bipolar diode recovery and charge reversal of transformer intrawinding capacitance. Common mode emissions consist of periodic current spikes through chassis ground caused by rapidly switched voltage across parasitic capacitance (C dv/dt). Sources of parasitic capacitance include transformer interwinding capacitance, transistor case-to-chassis capacitance and stray capacitance associated with the physical layout.

Good Design Practices Are Required

Power line conducted emissions, in both the differential and common mode, typically show up as a narrowband problem at the switching frequency and its harmonics, as well as a broadband high frequency problem. For example, a 200 kHz switching regulated dc-dc converter may have significant broadband emissions in the vicinity of 5 to 10 MHz due to the current spikes described above, in addition to narrowband emissions at 200 kHz, 400 kHz, etc. Of course, if either the dc source or the load is modulating, it is possible to have all manner of mixing products as well.

Depending upon the severity of the conducted emissions specification that must be met, the self-resonant frequencies of the power line filter components that are needed to attenuate the lower frequency emissions may be lower than the frequency range of the broadband emissions due to spikes. Above self-resonance, capacitors start to look like inductors and inductors start to look like capacitors. Therefore, switching regulator power line filters often, if not usually, consist of two distinct filter sections. The larger, lower frequency section is typically placed adjacent to the switching regulator itself in order to minimize the impedance and loop area of the input lines to the regulator. Depending upon the system configuration, the smaller, higher frequency section is often placed adjacent to the input connector, where it can also attenuate any additional conducted emissions caused by power line pick-up of locally generated radiated emissions.

Because spike related EMI is largely related to parasitic components and coupling, it is very difficult to predict. Therefore, the design of higher frequency power line filters often relies heavily on good design practices, such as the use of common mode inductors and strategically placed by-pass capacitors, as well as empirical post-design techniques (some would say "black magic"). Fortunately these higher frequency components are small enough that major redesign is usually unnecessary. Furthermore, the advent of board level simulators and more sophisticated estimation techniques continue to help mitigate this design problem.

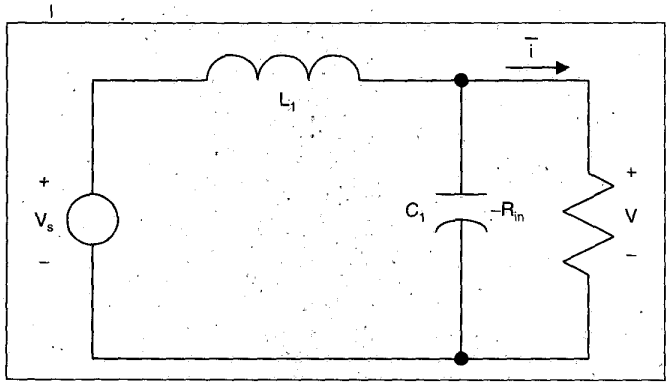


Fig. 2. Low frequency ac model of LC input filter with switching regulator load.

The lower frequency power line filters are not as amenable to the post-design trial and error techniques that may be successful for reducing high frequency broadband interference. Input filter requirements of greater than 60 dB at the switching frequency are not uncommon, requiring input filters that can easily be larger than the output filters. Therefore, a disciplined design process is required. In addition to the obvious size issue is the fact that these filters can seriously degrade the performance of a switching regulator, and even cause a switching regulator that is otherwise perfectly stable to become unstable. This is especially true if the resonant frequency of the power line filter lies well within the gain-bandwidth of the switching regulator open-loop gain function.

Several authors have written excellent books that address EMI/EMC causes, effects, specifications, analyses, measurements and mitigation techniques, including power line filters [2]-[7].

Power Line Filters Can Cause Instability

As a simplified example, let us consider a switching regulator that responds perfectly to any input voltage variation. By perfect response, we mean that the dc output voltage remains constant and unperturbed. Thus, for a given load, the output power is constant regardless of input voltage. For an ideal switching regulator, with no losses, this means that the average input power is constant as well. As the input voltage increases, the pulse-width modulated control circuitry cuts back the duty factor of the controlled switch to maintain constant output voltage. This, in turn, causes the average input current to be correspondingly decreased. Since the average input current decreases in response to an input voltage increase, and vice-versa, an ideal switching regulator behaves, on the average, like a negative dynamic resistance. As long as the frequency range of interest is much lower than the switching frequency, the system performance of a switching regulator is quite accurately represented by its average behavior [8]. Mathematically, the negative input impedance phenomenon can be demonstrated by taking the partial derivative of input voltage v with respect to average input current $\bar{i}$, while recognizing that $v = P/\bar{i}$

$$\frac{\partial v}{\partial \bar{i}} = \frac{\partial}{\partial \bar{i}}\left(\frac{P}{\bar{i}}\right) = -\frac{P}{\bar{i}^2} = -\frac{v^2}{P} = -R_{in}. \qquad (1)$$

A simple LC input filter, combined with the negative dynamic resistance model of the switching regulator, is shown in Fig. 2. This model is nonlinear since R_{in} is a function of v. However, in the neighborhood of a given operating point, where R_{in} can be considered constant and the system can

therefore be considered linear, the characteristic polynomial is $s^2 - s/R_{in}C + 1/LC$.

The negative term in the characteristic polynomial transforms to a positive exponential in the time domain, representing an unbounded, hence unstable, system. The minimum value of R_{in}, corresponding to the minimum value of v, is worst case. Of course, no switching regulator is lossless. However, because of their very high efficiencies, the constant load power will be much greater than the switching regulator losses. It has long been known that in order to assure stability, damping resistance must be explicitly included in the power line filter, thus complicating its design [9]-[12].

It is a fact that many dc-dc converters have been successfully designed and fielded, using simple LC power line input filters, by people who did not fully consider the theoretical arguments above.

There are several reasons why a switching regulator combined with a simple LC input filter might not oscillate in practice: (1) The LC input filter components and even the power line itself may include enough parasitic resistance to provide adequate damping. (2) Only interference at frequencies well above the fundamental switching frequency may be of concern, such that an LC input filter with a resonant frequency above the switching regulator gain-bandwidth (i.e., above the region where the regulator behaves as a negative resistance) is adequate. (3) The gain-bandwidth of the regulator may be artificially low relative to its switching frequency such that its gain-bandwidth, hence region of negative resistance, is below the LC input filter resonant frequency. An example of this would be a simple lag compensated switching regulator, where the gain-bandwidth is much less than the resonant frequency of the output filter, which, in turn, is much less than the switching frequency. However, the gain-bandwidth of the same switching regulator with lead compensation is higher than the output filter resonant frequency, and can easily be as much as one-tenth the switching frequency.

Almost any dc-dc converter that is intended to supply switched or modulated loads, such as microprocessors or power amplifiers, must be designed for wide gain-bandwidth. Furthermore, for some topologies, input voltage feedforward techniques can be used with either voltage mode control or current mode control that, theoretically, allow perfect input voltage regulation, hence negative dynamic input impedance behavior, independent of gain-bandwidth [13]. Examples of where these techniques are applicable include the buck converter in the continuous conduction mode (inductor current is always greater than zero) and the flyback converter in the discontinuous conduction mode (the inductor current dwells at zero for part of the switching cycle).

In the remainder of this article, power line filter design considerations will be discussed for dc-dc converters that have switching regulator gain-bandwidths much higher than the resonant frequency of its power line filters. In particular, we will discuss a design strategy, including a sample problem, that can be used to determine the *minimum-size* power line filter component values that are required to provide sufficient attenuation of switching frequency related power line conducted interference, without serious degradation to stability and performance. We will use a chopped current source model of the switching regulator for interference considerations and a negative resistance model of the switching regulator for stability considerations. For dc-dc converter performance considerations, we will use a small-signal linear model to permit frequency domain analysis using Laplace transforms. Thus, we will be able to confirm stability using Nyquist plots, as well as to assess performance, at least within the limitations of the linear model, using transfer functions such as conducted susceptibility (variation in output vs. input—also called audio-susceptibility) and output impedance. These transfer functions correspond, respectively, to dynamic line and load regulation.

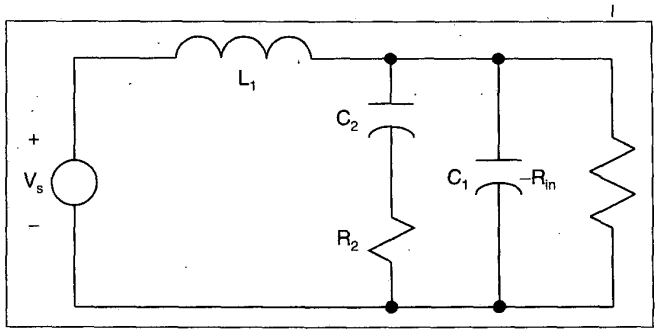


Fig. 3. Damped RC input filter.

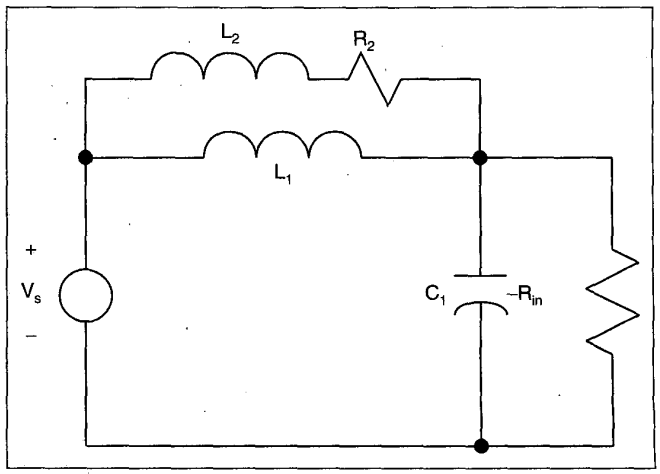


Fig. 4. Damped RL input filter.

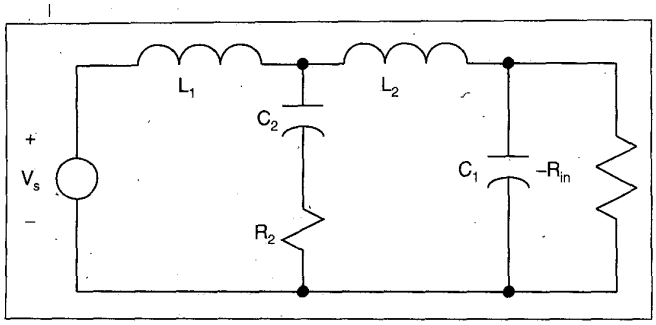


Fig. 5. Two-section damped RC input filter.

Damped Power Line Filter Configurations

It is not practical simply to add a damping resistor directly to the LC input filter. A damping resistor in series with L would seriously degrade efficiency, since it must pass all of the dc input current. A damping resistor in series with C would seriously degrade the attenuation characteristic of the filter as well as the efficiency, since it must essentially pass the entire ac input current component. A damping resistor in parallel with C must be less than the smallest expected value of R_{in} (corresponding to the minimum value of input voltage for which regulation is maintained) in order for the total parallel equivalent resistance to be positive. This approach is absurd, since the efficiency would automatically be less than 50%. However, if this parallel damping resistor $R_2 < R_{in}$ were ac coupled with a large enough second capacitor C_2 in what we will call a damped RC configuration (Fig. 3), one can imagine that adequate damping may now be achievable with negligible loss of efficiency. A fundamental requirement is that the zero frequency $1/R_2C_2$ must be less than $1/\sqrt{L_1C_1}$ so that the damping resistance is available at the resonant frequency of the filter. Typically, this requirement results in $C_2 > C_1$, thus representing a significant impact to size, if not to efficiency. Assuming that R_2 is large enough that the preferred path for the ac interference current is still through C_1, the RC damping path does not significantly reduce the value of L_1 that is needed to meet the interference attenuation specification compared to the simple LC configuration.

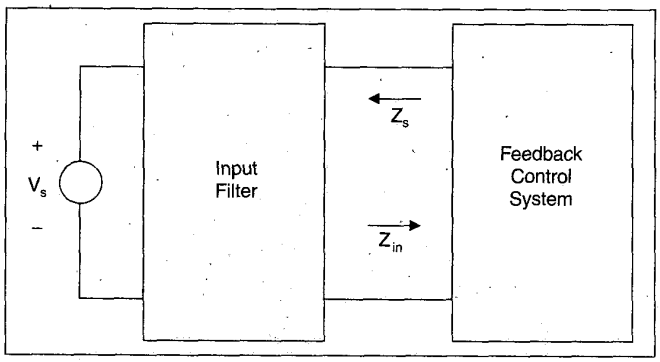


Fig. 6. Feedback control system with input filter.

In similar fashion, it is also possible to use an RL configuration (Fig. 4) to achieve damping, where L_1 provides the dc current path. In this case, the zero frequency R_2/L_2 must be greater than the resonant frequency $1/\sqrt{L_1C_1}$, which typically results in $L_1 > L_2$. For this damped RL configuration, damping degrades the attenuation of the input filter, since the damping path is in parallel with L_1 instead of C_1. Therefore, L_1 must be larger in order to achieve the same interference attenuation as the simple LC filter. Because of size and capacitor cost factors, the damped RL configuration is generally better for higher voltage applications, and the damped RC configuration for lower voltage applications. Examples of higher voltage applications include the intermediate dc-dc converters that are used with ac input off-line rectifiers and dc-dc converters that operate from higher voltage dc prime power, such as the new 270 Vdc military standard. Although the design details are naturally different, the overall design strategy is much the same for both RC and RL damped filter configurations.

For the detailed discussions that follow, we will use a modified version of the RC configuration, which would be especially applicable to lower voltage dc-dc converters. The modified filter, shown in Fig. 5, is now a two-section filter with a second inductor between the main input capacitor and the damping capacitor. Although this is a well-known configuration [14], the design strategy deserves further consideration. By choosing a small enough value of L_2, such as $L_2 = L_1/10$, the switching frequency attenuation is significantly improved with only a minor influence on the low frequency performance of the filter. Prior to discussing the design of this specific filter, it may be appropriate to provide some analytical background for the general problem of switching regulators with input filters.

Analytical Background

In linear feedback control systems, the characteristic equation can be expressed as

$$P(s)(1+G(s)H(s))=0,$$

where $P(s)$ is the characteristic polynomial of the original system to be controlled (i.e., without feedback), and $G(s)H(s)$ is the open-loop gain function. If the feedback control system is now connected to an input network, such as a power line filter, the characteristic equation for the entire system can be described by:

$$\left(1+\frac{Z_s(s)}{Z_{in}(s)}\right)(1+G(s)H(s))P(s)=0, \qquad (2)$$

where the term $Z_s(s)$ is the source impedance of the input network and $Z_{in}(s)$ is the input imped-

ance of the feedback control system (Fig. 6). If the input impedance is negative, i.e. $Z_{in}(s) = -R_{in}$, as in the case of our perfect switching regulator, then the term $-Z_s/R_{in}$ can potentially cause system instability just as surely as a phase shift of 180° in the open-loop gain function $G(s)H(s)$ can. Since 6 dB is a widely accepted gain margin for the open-loop gain function, we will use that same standard for the term Z_s/R_{in}, namely $Z_{s(\max)} < R_{in(\min)}/2$, where $Z_{s(\max)}$ occurs at the dominant resonance of the input filter.

Since a switching regulator is not even continuous, let alone linear, frequency domain analysis only applies when low frequency (relative to the switching frequency) and small-signal approximations are valid. Not all perturbations to switching regulators would qualify as low frequency or small signal. Therefore, more sophisticated simulations using numerical analysis routines are ultimately necessary to predict full performance. Nevertheless, much can be learned about switching regulator behavior from the closed-form expressions made possible by simple, linear approximations. Several excellent textbooks are available to the reader who is interested in learning more about switching regulator design and modeling [15]-[18].

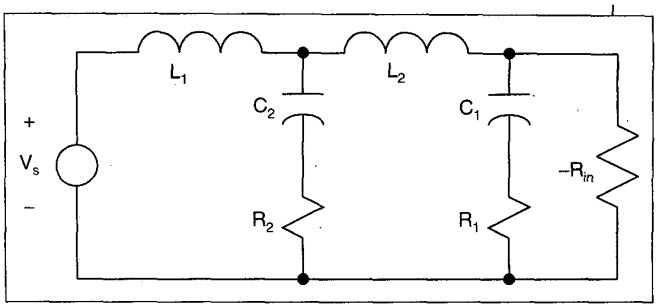


Fig. 7. Two-section damped RC input filter including ESR.

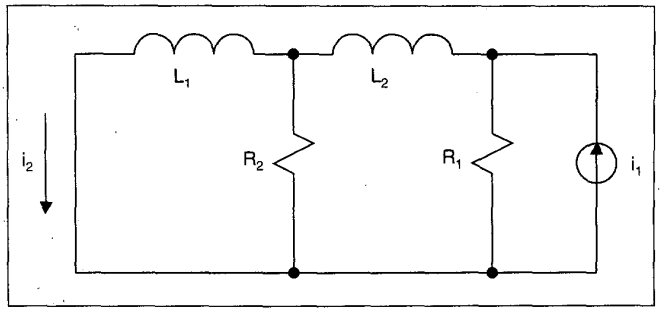


Fig. 8. Noise model of two-section RC damped input filter.

Power Line Input Filter Design Strategy

As we have discussed, the three primary requirements for the power line input filter are (1) sufficient attenuation at the switching frequency, (2) stability with the follow-on regulator and (3) minimum size. Subsequently, we will need to examine whether the input filter that does not cause instability nevertheless causes undue performance degradation. If so, performance considerations override stability considerations and additional damping would be required. For example, an input filter that is damped well enough to meet the $Z_{s(\max)} < R_{in(\min)}/2$ criterion may still have a low enough damping factor to cause unacceptable resonant peaking and an associated system conducted susceptibility (immunity) problem. However, no ac voltage source modulation is without source impedance, which must be taken into account to prevent unnecessary overdesign. As a practical matter, one needs to know not only the EMI specifications that apply to the dc-dc converter, but how it will actually be tested for EMI compliance as well. In the following, several simplifying assumptions are made in the design of the input filter besides the switching regulator linear assumptions previously discussed.

In the far majority of dc-dc converters, the power line input filter capacitors are electrolytic,

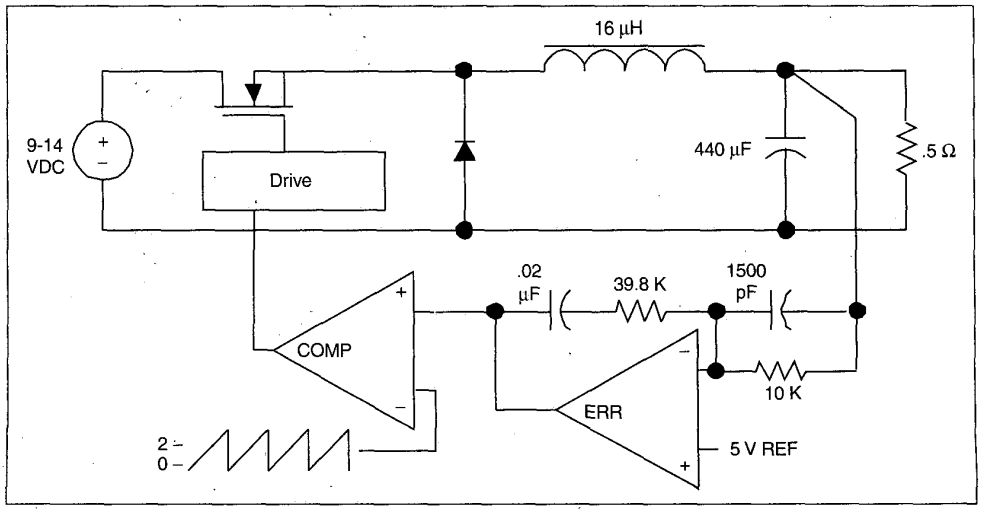


Fig. 9. Sample 50-W, 12-V to 5-V buck switching regulator.

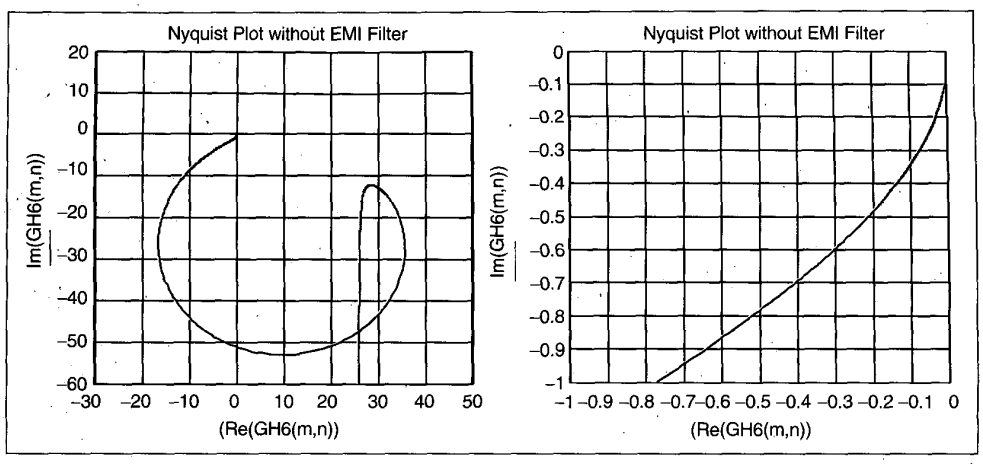


Fig. 10. Nyquist stability plot of sample buck converter without input filter.

either aluminum oxide or solid tantalum. At the switching frequency, parasitic equivalent series resistance (ESR) dominates the impedance of these capacitors. Therefore, the input filter configuration of Fig. 5 must be updated to include ESR (Fig. 7). For the worst case, we assume maximum ESR for attenuation purposes and zero for stability purposes. We will also assume zero parasitic resistance for the inductors, letting all parasitic resistance represent a stability safety factor. The input filter noise model is shown in Fig. 8, where R_2 is understood to include the maximum ESR of C_2 and i_1 is the equivalent noise source at the switching frequency. As a simplifying assumption, the low frequency effect of L_2 is ignored. Thus, the third-order model, which will be used to determine maximum input filter source impedance, hence stability, is the same as Fig. 3. Also, for worst-case stability considerations, the ESR of C_2 is assumed to be zero. (In any case, the ESR of C_2 is typically much smaller than the required damping resistance.)

Virtually all electrolytic capacitors have ripple current limits that are based on thermal constraints due to ESR-related power dissipation. Recognizing that C_1 must accommodate essentially all of the switching regulator noise current, the value of an electrolytic C_1 is constrained, in practice, by its ripple current limit and, therefore, is not part of the size minimization procedure. If we let the value of L_2 be fixed to L_1 by the equation $L_2 = L_1/K$, there are still three independent variables, namely, L_1, C_2 and R_2, available to meet our three design requirements. For applications where C_1 may be a good high frequency, non-polarized capacitor, such as a multi-layer ceramic with very low ESR, it can be included in a more complicated total input filter component volume minimization process that can benefit from Lagrangian multiplier techniques. For our purposes here, we will assume that

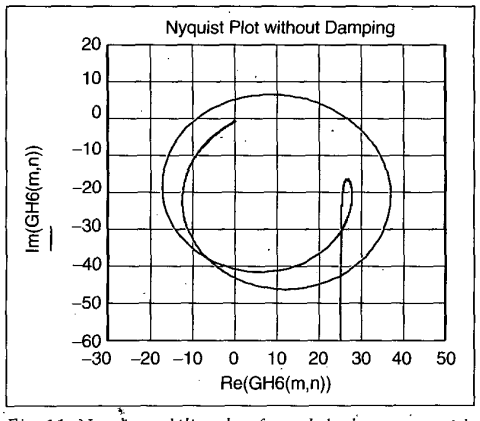


Fig. 11. Nyquist stability plot of sample buck converter with LC input filter.

C_1 is electrolytic and, therefore, is predetermined by its ripple current rating.

Assuming that $R_1 << 2\pi f_s L_2$ and $R_2 << 2\pi f_s L_1$, where f_s is the switching frequency, and letting $L_2 = L_1/K$, where $K >> 1$, the required input filter attenuation Γ can be expressed as

$$\Gamma = \frac{R_1 R_2 K}{(2\pi f_s L_1)^2}. \quad (3)$$

This equation corresponds to requirement (1) above.

We next assume that R_2 and L_2 are small enough that the dominant resonant frequency can be expressed as

$$\omega_n = \sqrt{\frac{1}{L_1(C_1 + C_2)}}. \quad (4)$$

The maximum input filter source impedance is then

$$Z_{s(\max)} = \frac{\sqrt{\omega_n^2 + \left(\frac{1}{R_2 C_2}\right)^2}}{C_1\left(\frac{1}{L_1 C_1} - \omega_n^2\right)} = \alpha R_{in}. \quad (5)$$

Using the variable α gives us the flexibility to use a smaller value than 0.5, if necessary, to account for errors due to simplifying assumptions and/or to increase damping beyond stability requirements to address possible performance concerns. Combining (4) and (5) yields:

$$(\alpha R_{in})^2 = \left(\frac{L_1(C_1+C_2)}{C_2^2}\right)\left(1 + \frac{L_1(C_1+C_2)}{R_2^2 C_2^2}\right) \quad (6)$$

This equation corresponds to requirement (2) above.

Since the size of R_2 is negligible with respect to the sizes of L_1 and C_2, the volume V to be minimized can be expressed as $V = \beta_1 L_1 + \beta_2 C_2$, where β_1 is the size coefficient for L_1 in in^3/henry for a given current, and β_2 is the size coefficient for C_2 in in^3/farad for a given voltage. If the final values of L_1 and C_2 are too far removed from the values upon which β_1 and β_2 were based, a second design iteration may be required. Naturally, the size factors β_1 and β_2 are also dependent upon the capacitor and inductor types used. The minimum size requirement (3) above then corresponds to (7) below:

$$\frac{\partial V}{\partial R_2} = \beta_1 \frac{\partial L_1}{\partial R_2} + \beta_2 \frac{\partial C_2}{\partial R_2} = 0. \quad (7)$$

We next define some intermediate variables that simplify notation and permit the reader to follow the algebra more easily.

$$\lambda = \sqrt{R_1 K/\Gamma (2\pi f_s)^2} \quad (8a)$$

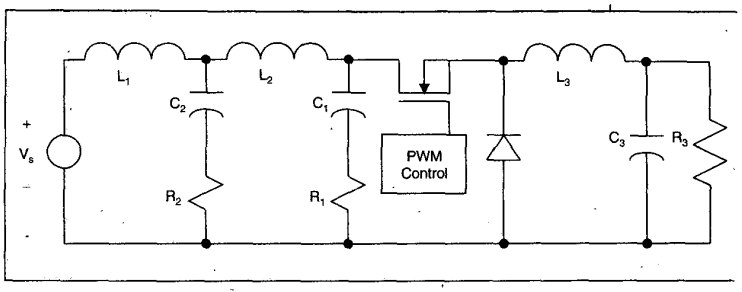


Fig. 12. Sample buck converter with two-section rc damped input filter.

$$\sigma = \lambda(C_1 + C_2)/C_2^2. \quad (8b)$$

Substituting (8a) and (8b) into Eq. (6) results in

$$\sigma = \frac{\sqrt{R_2^3 + 4R_2(\alpha R_{in})^2} - R_2^{3/2}}{2}. \quad (9)$$

Since we know that σ must be positive, (9) sets an upper bound on R_2, namely $R_2 < \alpha R_{in}/\sqrt{2}$. With substitutions, (7) becomes

$$\beta_1\lambda\left(1 + \frac{2\sigma}{R_2^{3/2}}\right) = \frac{\beta_2 C_2(C_1+C_2)}{R_2^{1/2}(2C_1+C_2)}\left(\frac{\sigma}{R_2^{3/2}} - 1\right) \quad (10)$$

Although a computerized approach using the Mathcad "find" function, for example, can be used to great advantage, the conceptual design procedure is as follows:

Step 1. Start with $R_2 = \alpha R_{in}/\sqrt{2}$

Step 2. Determine σ from Eq. (9)

Step 3. Determine C_2 from Eq. (8b)

Step 4. Check the integrity of Eq. (10)

Step 5. If necessary, return to Step 1 using an incrementally smaller value of R_2

Step 6. Determine L_1 (hence L_2) from Eq. (3)

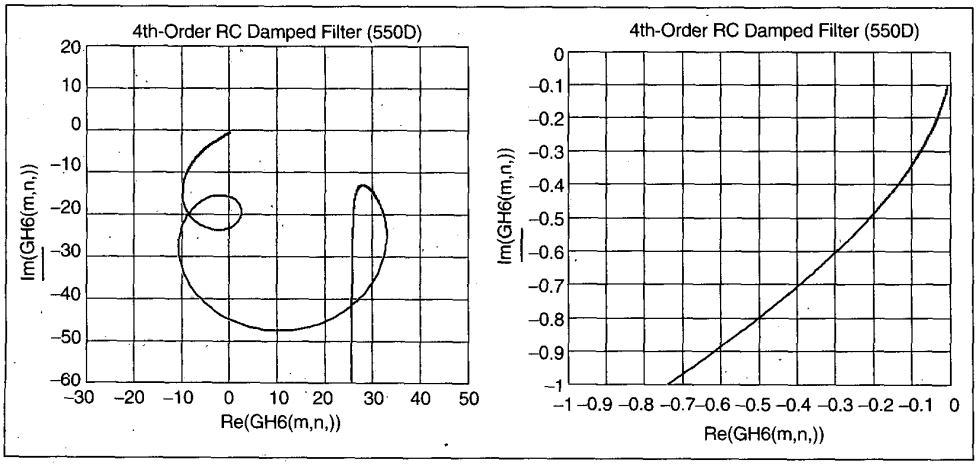


Fig. 13. Nyquist plot for sample buck converter with two-section RC damped input filter.

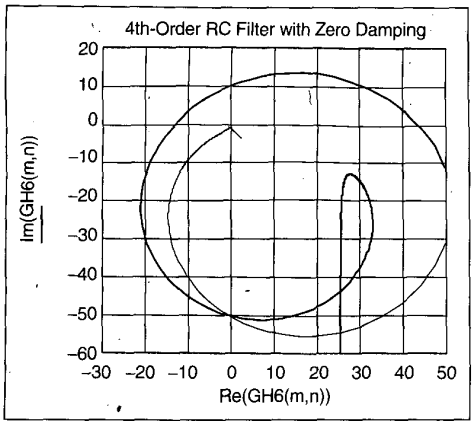


Fig. 14. Nyquist plot for sample buck converter with two-section undamped input filter.

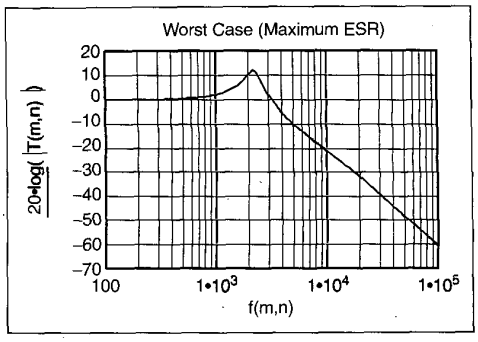


Fig. 15. Interference current attenuation plot for two-section RC damped input filter.

A Detailed Design Example

For our design example, we will consider a dc-dc converter that would be suitable for automotive applications. The objective is to design a power line input filter of the configuration shown in Fig. 7 for the 50-watt, 12- to 5-volt buck switching regulator shown in Fig. 9. The output filter inductor is large enough that the switching regulator input current can be approximated as a quasi-square wave. (This will almost always be the case for buck regulators whose output filters are designed for minimum size at full load.)

Taking semiconductor losses into account, the input power will be very close to 60 watts and the duty factor will be very close to 0.5 nominally, which causes a worst-case power line conducted emission of 5 amperes rms. For simplicity, as well as a safety factor, we will assume that all of the ac current is at the switching frequency of 100 kHz. To meet the Society of Automotive Engineers (SAE) conducted emission specification of 5 mA at 100 kHz, the input filter attenuation must be at least 60 dB. The efficiency of a switching regulator is at least somewhat independent of input voltage. At higher input voltage the switching losses are generally greater but the conduction losses are generally less due to the lower duty factor. Therefore, we will make the worst-case assumption that the 60 watt input power is constant. For an input voltage range of 9 to 14 volts, the worst-case (i.e. minimum) value of Z_{in} is $-(9)^2/60 = -1.35\Omega$.

As far as the control circuitry is concerned, we will assume lead compensation with a phase margin of slightly greater than 45° but no input voltage feedforward control. This will allow us to treat the input impedance as a negative resistance in the vicinity of the input filter resonance, but it will also allow us to see the effect of the input filter on conducted susceptibility, which feedforward control would mask. The Nyquist stability plot for the linearly approximated switching regulator without input filter is shown in Fig. 10. Note that the point $(-1+j0)$ is not circled and that for $|G(j\omega)H(j\omega)| = 1$, the phase angle is greater than 45°.

As a benchmark, we will design a simple LC filter that meets the attenuation requirement but not necessarily the stability requirement. Modern solid tantalum capacitors are selected for their high density and low ESR. Three 20-volt 100 μF capacitors in parallel are required to accommodate the 5 A rms ripple current. The maximum ESR is .025 Ω (.075 Ω per capacitor), requiring L_1 = 40 μH to meet the 60 dB attenuation requirement. Assuming that L_1 is wound on a molypermalloy powder (MPP) toroid, the total size of the simple LC filter is 1.08 in^3 with β_1 = 1.38 in^3/henry and β_2 = 1.76 in^3/farad. The Nyquist plot of the 4th-order system comprised of the linearly approximated switching regulator with LC input filter is shown in Fig. 11. Note that the system is unstable, even though we purposely included maximum ESR.

The values for the damped filter of Fig. 7, obtained using the procedure described in the previous section, are shown below:

$$C_1 = 300\mu F \quad L_1 = 8.5\mu H$$

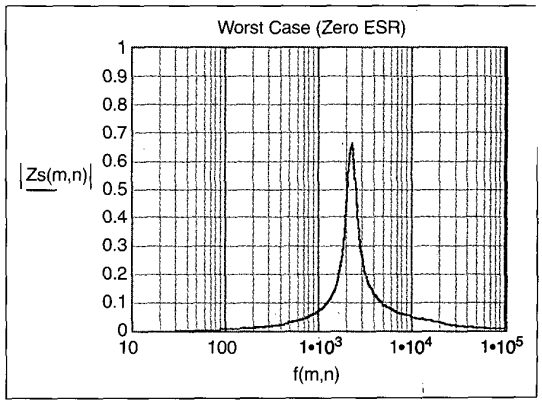


Fig. 16. Source impedance plot for two-section RC damped input filter.

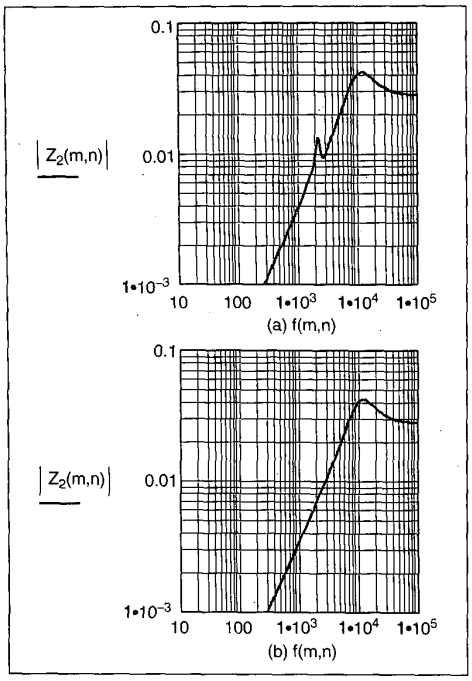


Fig. 17. Output impedance plot for sample buck converter, (a) with two-stage RC damped input filter and (b) without.

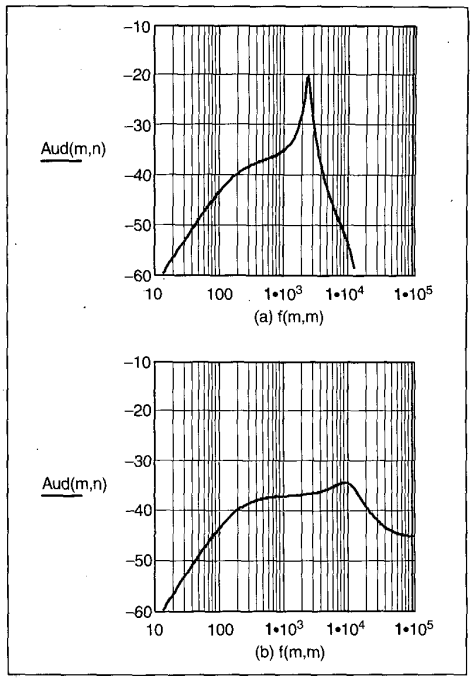


Fig. 18. Conducted susceptibility plot for sample buck converter (a) with two-stage RC damped input filter (with EMI filter), and (b) without.

$C_2 = 300\mu F$ (rounded up from 267 μF)
$L_2 = 0.85\mu H \quad R_2 = 0.11\Omega.$

The Nyquist plot for the linear approximation of what is now a 6th-order system (Fig. 12) is shown in Fig. 13, where $R_1 = 0$ for worst case. Note that the system is not only stable, the plot in the vicinity of unity amplitude is almost identical to that of the original stable regulator. To prove the need of the damping resistor R_2, the Nyquist plot for the 6th-order system with $R_2 = 0$ is shown in Fig. 14. The volume of the damped filter is 1.19 in^3, or 10% larger than the volume of the simple, unstable LC input filter. Without L_2 (Fig. 3), the volume would be 1.81 in^3, or 67% larger. The filter attenuation is plotted in Fig. 15. Remembering that the goal was to achieve a $Z_{s(max)}$ no greater than 1.35/2 = 0.675 Ω, the plot of Z_s for the damped filter is shown in Fig. 16. Although there is sufficient damping from a stability viewpoint, we need to examine whether the input filter has unduly affected performance.

Using an extension of the linearly approximated switching regulator design aids available in [19], Fig. 17 shows dc-dc converter output impedance with and without input filter. As might be expected, a 6 dB "bump" occurs at the input filter resonant frequency due to the $1 - Z_s(s)/R_{in}$ term in the characteristic polynomial. As long as the input filter resonant frequency does not occur at the frequency of maximum output impedance, the effect is minimal. On the other hand, the corresponding plots of conducted susceptibility (Fig. 18) show a 16-dB increase in the peak value, which can be attributed to the signal gain at resonance in the input filter itself, as well as to the $1 - Z_s(s)/R_{in}$ term. In theory, this problem could be eliminated, at least for the buck topology, by using input voltage feedforward control. However, at input filter resonance, the increased ac voltage excursion at the input terminals of the switching regulator itself may be beyond the range of regulation. As previously indicated, a significant mitigating circumstance is that no ac input modulation source is without source resistance. For our sample problem, an ac modulation source resistance of only 0.05 Ω is required to reduce the resonant peaking of the input filter to the point where the peak conducted susceptibility increase is only 3 dB. The source resistance associated with the conducted susceptibility (immunity) compliance test is widely variable, depending upon the equipment category and the regulatory agency, but at least some conducted susceptibility test procedures permit a source resistance of up to 0.5 Ω.

Conclusion

This article has presented an overview of switching regulated dc-dc converter electromagnetic interference problems and possible solutions, with special emphasis on power line conducted emissions

and power line input filters. Potential stability and performance problems that can be caused by the interaction between the power line input filter and the switching regulator have been discussed in detail. Candidate damped input filter structures have been presented, along with a general input filter design strategy and a detailed design procedure for one of the candidate configurations. A sample problem consisting of a damped input filter for a 50-watt, 12- to 5-volt buck switching regulator has been solved. A performance simulation of the entire dc-dc converter comprised of the input filter and buck regulator has been performed using the small-signal, linear switching regulator model.

Although the design approach presented in this article has been successfully used in delivered products, there may well be better approaches. The larger point is that unless some disciplined process is followed in which the power line filter that is intended to suppress switching regulator emissions is designed concurrently with the switching regulator itself, there is likely to be trouble ahead.

References

[1] R.P. Severns and G.E. Bloom, *Modern Dc-Dc Switchmode Power Converter Circuits*, New York: VNR, 1985.

[2] H.W. Ott, *Noise Reduction Techniques in Electronic Systems*, New York: Wiley, 1976.

[3] M.J. Nave, *Power Line Filter Design for Switched-Mode Power Supplies*, New York: VNR, 1991.

[4] R.L. Ozenbaugh, *EMI Filter Design*, New York: Dekker, 1996.

[5] L. Tihanyi, *Electromagnetic Compatibility in Power Electronics*, New York: IEEE, 1995.

[6] V.P. Kodali, *Engineering Electromagnetic Compatibility*, New York: IEEE, 1996.

[7] B. Keiser, *Priniciples of Electromagnetic Compatibility*, Norwood, MA: Artech House, 1987.

[8] G.W. Wester and R.D. Middlebrook, "Low-frequency characterization of switched dc-dc converters," *IEEE Power Processing and Electronics Specialists Conf. Rec.*, 1972.

[9] N.O. Sokal and D.E. Nelson, "Preventing input-filter oscillation in switching regulators," *Proc. Powercon 2*, 1975.

[10] R.D. Middlebrook, "Input filter considerations in design and application of switching regulators," *IEEE Power Electronics Specialists Conf. Rec.*, 1977.

[11] D.M. Mitchell, "Damped EMI filters for switching regulators," *IEEE Trans. Electromag. Compat., Vol. EMC-20, 1978.*

[12] F.C. Lee and Y. Yu, "Input filter design for switching regulators," *IEEE Trans. Aerosp. Electron. Syst.*, Vol. AES-15, 1979.

[13] D.M. Mitchell, *Dc-Dc Switching Regulator Analysis*, ch. 6, New York: McGraw-Hill, 1988.

[14] Y. Yu and J.J. Beiss, "Some design aspects concerning input filters for dc-dc converter," *IEEE Power Conditioning Specialists Conf. Rec.*, 1971.

[15] J.G. Kassakian, M.F. Schlecht, and G.C. Verghese, *Principles of Power Electronics*, Reading, MA: Addison-Wesley, 1991.

[16] N. Mohan, T.M. Underland, and W.P. Robbins, *Power Electronics*, New York: Wiley, 1989.

[17] P.T. Krein, *Elements of Power Electronics*, New York: Oxford University Press, 1998.

[18] R.W. Erickson, *Fundamentals of Power Electronics*, New York: Chapman & Hall (Kluwer), 1997.

[19] D.M. Mitchell, *Small-Signal MathCAD Design Aids*, San Rafael, CA: e/j Bloom Assoc., 1992.