

Power Conversion Techniques for Portable EMI Sensitive Applications

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Abstract

In circuit applications that demand low noise, such as in many portable wireless devices, there is a need to optimize circuit design in power converter circuits. The path to low noise performance does not necessarily require exotic circuit techniques or the latest IC features. Conventional low noise power supply techniques are “tweaked” to improve the performance of dc/dc conversion circuits. A series of improved circuit designs are outlined such as redesigns in push-pull converters, the use of negative raiing, the usage of charge pumps (also known as inductorless design), single resistance-capacitance filter, and PCB ground layout. The design techniques are explained and sample circuits are shown. Noise measurements of such re-designed circuits are performed with the improved results explained. Some final attention is paid to pitfalls occurring from using digital layout design hardware in the use of mostly analog layout methods in power conversion circuits.

Introduction

In applications that demand low noise such as in portable wireless devices, designers typically stay away from dc/dc converter circuits and instead linear supplies are used. However, linear supplies tend to put a toll in battery life since linear power supply are highly inefficient. In this work several options of improved design are explored.

Consider First a Push-Pull Converter.

A push-pull converter (also know as a forward converter) differs from the more widely used buck, boot, or inverting

converter in that its energy is never stored in the magnetic component [1]. In inductor based dc-dc converters (like the buck, boost), the inductor alternately collects the energy from the input supply and transfer it to the output. The output filter capacitor alone must support the whole load while the coil is recharging. In the proposed push pull design, the transformer does not store the energy but rather transfer it. In the proposed design of Figures 1 and 2; at any instant, one of two switches is on, and the current flows in the transformer primary and secondary windings simultaneously. The proposed design in Figures 1 and 2 are very quiet designs, specially for negative power supplies which usually exhibit a very poor rejection of noise in their negative rails. A description of the main noise reductions features of the designs in Figures 1 and 2 will be provided.

In most pre-amp applications negative power supply is needed in addition to the regular positive power supply. Filtering the positive power supply is usually sufficient, not so is the case for negative power supply rails. The designs of figures 1 and 2 are also good for negative supply except that larger capacitances C2 through C4 are needed (for figure 2) and a larger capacitance for C2 (in figure 1) is also needed.

Charge Pump Designs.

When noise sensitivity is a concern as in RF applications or where low level signals are present, charge pumps may provide better performance than dc-dc converters [2]. The most important advantage is that it eliminates the magnetic fields associated with inductors and transformers and a significant EMI source is eliminated. An

initial EMI source that remains in some designs is the initial charging current that can flow when the flying capacitors charge and discharge. The di/dt event can generate noise that may require additional capacitive filtering for its elimination. For negative power generation, the design in Figure 3 implements a capacitive charge pump. For light load applications, low noise post regulation can be included on the chip as shown in Figure 4. The paper will explain more details about these designs.

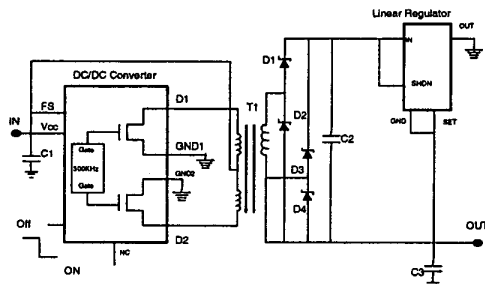


Figure 1. Forward converter design offering much quiet ripple noise environment (< 10mV p-p)

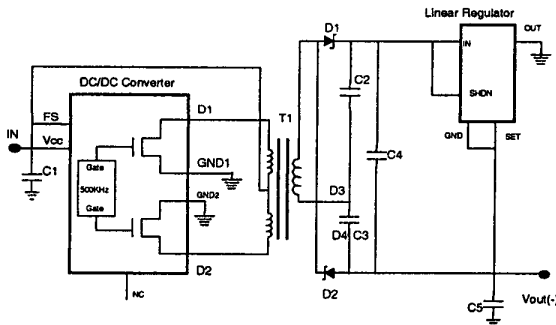


Figure 2. Low noise push-pull design connecting secondary in voltage doubling configuration

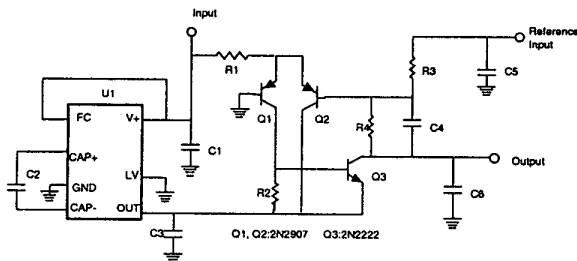


Figure 3. Charge pump with regulator

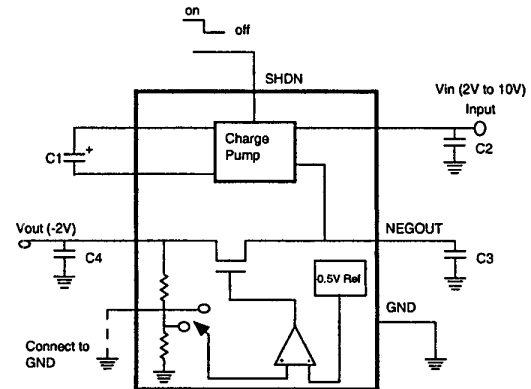


Figure 4.0 Light load application with an internal regulator within a charge pump IC.

Synchronized Design.

Filtering and shielding are the common strategies used for conducted noise suppression. An alternate design approach that can save the cost and inconvenience of these solutions is to “lock” the dc-dc converter’s operating (and noise generating) frequency to a clock source that confines the ripple and emitted spectrum to frequencies that don’t interfere with the rest of the system. This solution does not reduce the amplitude of the radiated noise, but it confines the noise spectrum to less intrusive harmonics located away from the frequencies that could hurt the performance of a device (e.g the IF frequency of a wireless device). This can be accomplished using the SYNC input of the dc-dc converter to lock the converter oscillator to an external clock source. A design implementing this type of synchronization is shown in Figure 6. The paper explains this type of synchronization circuit. Figure 7 shows a look at the spectrum with and without synchronization for the circuit in Figure 6.

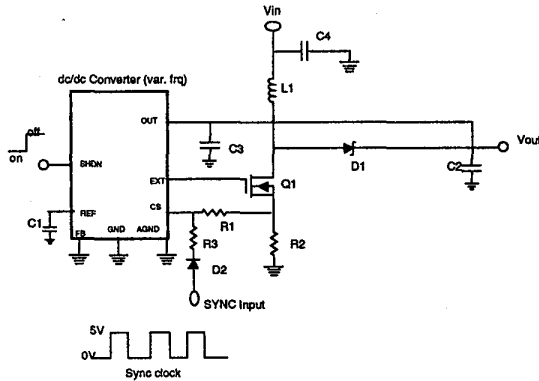


Figure 5.0 Variable frequency dc-dc converter can be synchronize through their current sense input.

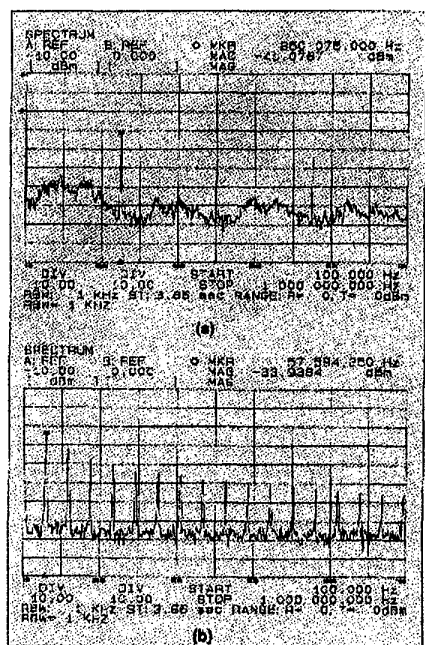


Figure 6. Noise spectrum for circuit in fig.5

Other Simple Noise Reduction Techniques.

Simple resistance RC filter: Use when the load current is low. It is the lowest cost. Feasibility of this option depends on whether it can be inserted in series with the load without a significant voltage drop in the output or a degraded load regulation. For example, at a 10 mA load, a 10 ohm resistor will drop 100 mV. A 1uF capacitor will add a 15KHz roll-off to the output. Always remember to add the filter after the circuit

feedback's connection. The RC filter can also be made just to filter out the portion of the load that needs low noise, not necessarily the whole spectrum.

Proper Selection of Power FET: Selecting the proper FET for power switching or synchronous rectification functions also helps reduce EMI generated by the supply. Some MOSFETs have a very low C_{oss} , which will create less spiking during the MOSFET's turn-off.

Figure 6.0 is the noise spectrum plots for the circuit in figure 5 showing the benefits of synchronization: (a) without synchronization, (b) with synchronization.

PCB Layout. This is the most common source of dc-dc noise problems. [3] Although the main cause of the problem is inductor fields, high dI/dt in circuit components and traces, and high dV/dt at circuit nodes can be severely aggravated by poor layout. Many poor layouts are being generated by auto route layout software intended for logic design. Of particular importance to watch are:

- a) Keep the switching nodes physically small: In conventional dc/dc converters, the nodes are where the coil, switch, and diode meet. These nodes are antennas and can radiate. The traces should be wide to carry high current and smallest as possible (lengthwise).....(more will be described in paper).
- b) In many power supply design with resistor feedback, locate feedback resistors right next to the IC feedback pin, and keep the trace area at the feedback pin minimized. The feedback pin is a high impedance node, and therefore is susceptible to noise radiate from other parts of the circuit.
- c) Identify the traces through which high currents are flowing and size them as wide and short as possible. In particular, pay attention to the vias through the PCB, because these are poor conductors

at high currents, specially in high speed switching circuits.....(more will be discussed in paper).

- d) Ensure that low noise grounds such as those in feedback resistors, reference bypass capacitors, and the IC analog ground pins are not polluted from high currents in power ground traces. Should use a separate plane from that of power ground.
- e) Avoid cutting up the ground plane with too many long jumpers traces. This is a common problem because the ground plane and the signal plane are usually one above the other but very close to each other. Signal traces are often jumpered through the ground plane (wrong thing to do) and should instead be jumpered to through a layer other than ground layer.

In a typical dc/dc converter applications there are several current loops that exist inside every switching power supply. Each of these loops must be kept separate from one another. In order of their importance to a good pc-board layout, they are: a) the power- switch ac-current loop, b) the output-rectifier ac-current loop, c) the input-source current loop, and d) the output-load current loop. These loops are present in each of the most common and major representations of switching power supply topologies (see Figure 7).

The input-source and output load current loops typically don't present problems. The current in these loops is largely composed of dc flow, with some small ac current summed onto the waveforms. Usually these loops have special filters to discourage the escape of ac noise into surrounding environment. The terminals of the input and output filter capacitors should be the only places where the input and output current loops, respectively, connect to the power supply. The input loop charges its capacitor with a near dc-current but is unable to supply the

high frequency pulses required by the switching power supply. The filter's capacitor's main role is to perform this wideband energy reservoir function. In the same manner, the output capacitor stores the high frequency energy from the output rectifier and allows the output load loop to remove that energy in a dc fashion. If the connections between the input or output loops and the power switch or rectifier loops aren't routed directly to the capacitor's terminals, then ac energy will go around the input or output filter capacitors and escape into the environment

The power switch and rectifier ac-currents loops contain very high trapezoidal current waveforms, which contain a lot of harmonics that extend far beyond the basic switching frequency. These currents can have peak currents two to five times that of the continuous or output dc currents. The transient times are typically about 50 ns. Therefore, the ac-current loops have the greatest ability to emit EMI.

These current paths should be routed before any other traces in the power supply. The three major components that make up each current loop in Figure 8 must be located adjacent to each other. They also have to be oriented such that the current paths between them are as short as possible (i.e minimize loop area). The traces of these four loops have a great effect on the converter's measured efficiency. Selecting packages where signals are shared with heatsink tabs can combine the functions of heatsink and signal transfer.

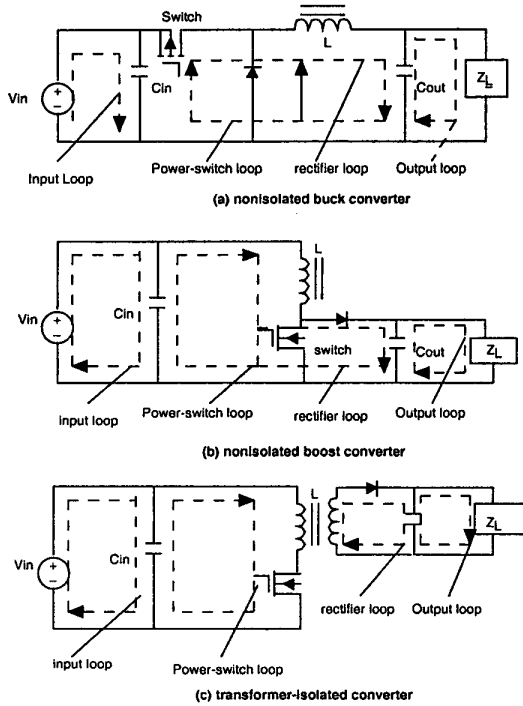
The grounds must be properly laid out (Figure 8). Crossover of grounds (i.e mixing analog and digital grounds) will cause problems with the power supply stability. An additional ground to address was the control ground. The control ground connects to the control IC and all of its associated passive components. As it is extremely sensitive, the control ground should be laid out after the other ac-current loops have been laid out. The control ground connects

to the other grounds at very specific points. The junction is a common point of any component across which the control IC wants to sense a small voltage. These points include the common end of the current sense resistor in a current mode switching converter and/or the bottom end of the output resistor driver.

Conclusion:

In this paper it is shown that improve design techniques are needed for addressing noise issues in dc-dc converters for portable electronic devices. Some of these design techniques have been addressed with appropriate sample circuits. It is expected that power supply designers can benefit from some of the insights in this discussions.

Figure 7. Major switching power topologies.



References:

[1] John D. Lenk, "Simplified design of switching power supplies," EDN series for Design Engineers, B-H Publishers, 1995.

[2] L.H. Dixon, "switching power supply topology review, Unitrode Seminar SEM 200, 1997.

[3] Perez, R. "An study in the Proper Design of Grounding for SMPS Converters and the role of CEM," 1999 ACES Symposium, Monterey, CA, March 12-15, 1999.

Figure 8. Good layout for a section of a converter (components place together).

