Line Input AC-to-DC Conversion and Filter Capacitor Design

Jesus Doval-Gandoy, Carlos Castro, and Moises C. Martínez

Abstract—The aim of this paper is to present a theoretical and practical analysis of one of the most popular ac–dc converter topologies. This topology is used to feed a dc–dc switch-mode converter from dual-input-voltage operation (230 V_{rms}, 50 Hz/115 V_{rms}, 60 Hz). For European line voltages (220, 230, and 240 V), the full-bridge rectifier complies with the IEC-61000-3-2 class A standard, if the value of the capacitor is selected with the right criterion. Simple expressions are obtained for all rms and peak currents and voltages. The mathematical analysis of this multifunctional ac–dc converter becomes very simple if the suitable assumptions are made. There is good agreement between experimental results and the mathematical analyis predictions

Index Terms—Full-bridge rectifier, IEC-61000-3-2, voltage doubler.

Fig. 1. AC–DC converter.

NOMENCLATURE

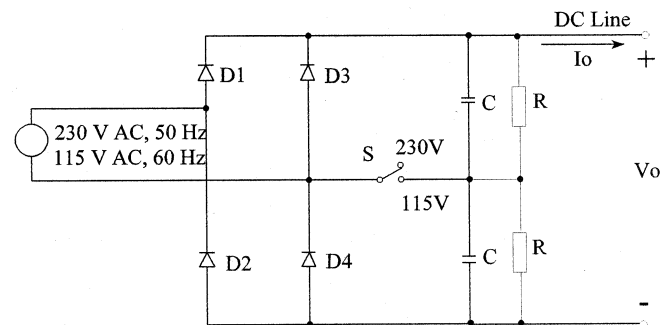|	
V_o	Input voltage of the dc–dc converter.
$V_{oripple}$	Ripple of V_o.
V_{oavg}	Average value of V_o.
I_o	Input current of the dc–dc converter.
I_{orms}	RMS value of the current drawn by the dc–dc converter.
W	Energy required by the dc–dc converter.
P	Input power of the dc–dc converter.
D	Duty cycle of the dc–dc converter.
V_{AC}	RMS value of the line voltage.
W_{C-dch}	Energy supplied by capacitance C to dc–dc converter.
W_{line-C}	Energy taken by capacitance C from ac line.
$\hat{V}_{AC}$	Peak value of the line voltage.
T	Period of the line voltage.
f	Frequency of the line voltage.
T_S	Switching period of the dc–dc converter.
$\hat{I}_{chg}$	Peak value of the filter capacitor current.
I_{dch}	Average value of the input current of the dc–dc converter.
I_{bridge}	Current through the diodes of the bridge.
I_C	Current through capacitance C.
V_C	Voltage in capacitance C.
I_{Crms}	RMS value of the current I_C.
$I_{chg-rms}$	RMS value of the capacitor charging current.
$I_{dch-rms}$	RMS value of the capacitor discharging current.
I_D	Current through diode D.
I_{D-rms}	RMS value of the current.
$\hat{I}_D$	Peak value of the diode current.
ASSn	Assumption number n.

I. INTRODUCTION

THE ac–dc converter used in low-power low-cost power supplies for universal line voltage (230 V_{rms}, 50 Hz/ 115 V_{rms}, 60 Hz) is shown in Fig. 1. This circuit has two operation modes.

- *Switch "S" opened:* The ac–dc converter is configured as a full-bridge rectifier with a capacitive filter (suitable for 230-V operation)
- *Switch "S" closed:* The ac–dc converter is configured as a voltage doubler (suitable for 115-V operation).

The first impression when analyzing, in a qualitative way, the performance of the ac–dc converter of Fig. 1 is that it is a very simple circuit. However, any attempt at mathematical analysis quickly proves otherwise. Indeed, as far as the authors know, there has never been a succesful analysis of a practical circuit. Of course, certain hypothetical cases have been treated in some papers [1]–[7].

Kammerloher [1] investigated thermoionic rectifier circuits and he was one of the first ones in doing mathematical analysis based on the assumption that the filter capacitor charges and discharges linearly. Unfortunately, not all expressions needed were derived, and the expression for the rms diode current is incorrect, because it was derived from the active power consumed by the whole circuit and not directly from the current flowing through the rectifier itself.

Schade [2] made a careful set of experimental determinations and tabulated the results in a universal system of dimensionless parameters. Moreover, the monograms given by Schade are valid for thermoionic rectifiers and the attempts to adopt them to silicon rectifiers have not been completely succesful [3].

Lieders [4], [5] made an interesting and laborious work considering that the filter capacitor charges and discharges linearly. He also obtained complex expressions which are difficult to obtain and apply. However, it is necessary to mention that he took into account the diode forward voltage, which is an important parameter when a transformer is used and the secondary voltage is small, but is not so important when working with 230-V /115-V ac line voltage. He did not calculate the rms capacitor current, which is an important parameter for choosing the suitable capacitor in a power application.

In [6], very complex expressions were obtained, whose solutions require trial-and-error methods, and it is necessary to use approximations for several exponential functions. As in [4] and [5], the rms capacitor current is not calculated.

In [7], the rectifier is analyzed under a practical point of view. The expression for the rms capacitor current is not right, because both ac and dc components of the charging and discharging currents do pass through the capacitor and, therefore, both of them contribute to capacitor heating. It is assumed that the capacitor charging current is a rectangular pulse; this assumption does not suppose greater error in rms current values but it will in peak current values.

In order to limit the harmonic content of the line current of mains-connected equipment, there are different regulations in Europe (IEC 61000-3-2 Ed. 2.0:2000) [8] and America (IEEE 519). The European standard defines four different classes for power electronic equipment. These classes establish different current harmonic limits depending on the use of the electronic equipment. In recent years, much effort has gone into finding cost-effective solutions in order to comply with these standards. Active power-factor-corrected (PFC) circuits are complex and expensive and generate electromagnetic interference. Passive PFC solutions (rectifier with *LC* filter) are quite economical, simple, and reliable. Nevertheless, the rectifier with capacitor filter as shown in Fig. 1 complies with IEC 61000-3-2 Ed. 2.0:2000 class A for input power up to 160 W if the capacitor has the suitable value.

The aim of this paper is to give information for choosing the value of the filter capacitor which complies with IEC 61000-3-2 class-A regulation and for obtaining the rms value, mean value, and peak value of currents and voltages in the rectifier.

II. DUAL-RANGE AC–DC CONVERTER

After reading the last section, it is evident that the analysis of the ac–dc converter is not easy. When the circuit of Fig. 1 is analyzed, the number of unknowns is greater than the number of equations and the set of equations is very complex to solve.

Nevertheless, the designer's objective is to solve the problem anyway, by sustitution of missing exact equations with inequalities in the form of approximations and tradeoffs. We must forget that a design is as much an art as a science, and the result must be optimum in some sense. From this point of view, there are some practical restrictions which limit the range of operation of the converter:

- If the capacitor C is too small, the resulting large ripple voltage will require increased duty cycle range and control loop gain to maintain the specified output voltage of the dc–dc converter connected to the output of the rectifier. Moreover $V_{o\,\min}$ will be lower, resulting in poor transformer utilization, high peak current through the switching power devices, and higher peak inverse voltage across the output rectifiers of the dc–dc converter.
- If the capacitor C is larger than necessary, it will not only cost more, but the recharging current pulses drawn from the line will be narrower and larger in amplitude. This hurts the line power factor and increases electromagnetic interference (EMI). The higher rms input current causes higher losses in the diodes. Moreover, the inrush current will be larger and it must be limited with an auxiliary circuit.

When the control of a dc–dc switchmode converter connected at the output of the rectifier is implemented by using an IC with *volts-second* control, the product $V_{o\,\min} \cdot D_{\max}$ defines the minimun number of turns in the primary section of the transformer, in order to limit the transformer losses or for mantaining the transformer out of saturation. If an IC without *volts-second* control is used, the minimun number of turns is defined by $V_{o\,\max} \cdot D_{\max}$. $V_{o\,\min}$ is the minimum output voltage of the rectifier, $V_{o\,\max}$ is the maximum output voltage of the rectifier, and $D_{\max}$ is the maximum duty cycle of the dc–dc converter.

From this, we conclude that the size of the transformer included in the dc–dc converter depends on the value of the output voltage of the rectifier V_o.

The value of the capacitor can be selected by using several criterions. A usual criterion is to select the capacitor from a holdup-time specification as follows:

$$20 \text{ ms @ minimum input voltage} \Rightarrow C = 0.8 - 2.5 \, \frac{\mu \text{F}}{\text{W}}$$

$$10 \text{ ms @ nominal input voltage} \Rightarrow C = 0.4 - 1.2 \, \frac{\mu \text{F}}{\text{W}}.$$

Another possible criterion is to select the capacitor from an output voltage ripple specification as used in this paper (1); the peak-to-peak ripple of the ac–dc converter output voltage is related to the minimum peak ac line voltage in accordance with the following expressions:

$$\text{full bridge: } k \in (0, 15 \div 0, 3) \quad V_{O\text{ripple}} = k \cdot \hat{V}_{\text{AC}\,\min}$$
$$\text{voltage doubler: } k' \in (0, 2 \div 0, 4) \quad V_{O\text{ripple}} = k' \cdot \hat{V}_{\text{AC}\,\min}.$$

$$(1)$$

III. ANALYSIS OF A FULL-BRIDGE RECTIFIER WITH CAPACITIVE FILTER

In Fig. 2 are represented the capacitor voltage and current through the diodes of the bridge and through the capacitor, when a switching converter is connected to the output of a full-wave bridge rectifier. There is a high-frequency ripple over the low-frequency component of the current. For simplicity in analysis in this paper, we are going to consider the waveforms of Fig. 3 instead of the waveforms of Fig. 2.
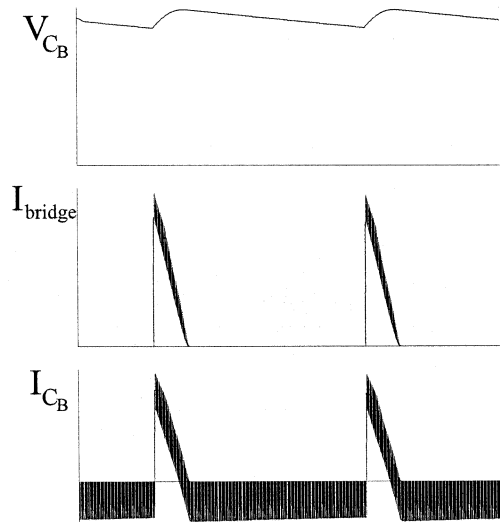
Fig. 2.   Waveforms for the bridge rectifier when connected to a switching converter.
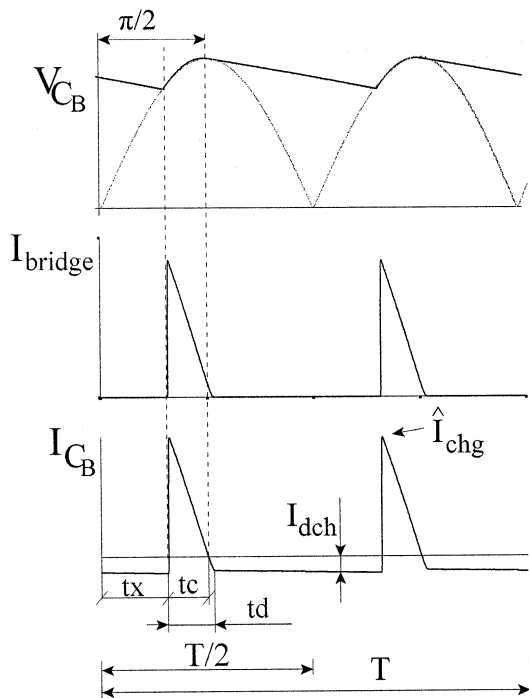

Fig. 3.   Approximation for the waveforms of Fig. 2.

In Fig. 1, full-wave bridge operation appears when the switch is in the 230-V position. The filter capacitance $C_B = C/2$ charges to peak line voltage each half cycle.

The energy required by the dc–dc switchmode converter for one ac line cycle is given by the following equation:

$$\int_0^T dW = \int_0^T P(t) \cdot dt \Rightarrow W = P \cdot T = \frac{P}{f}$$

$$\text{Assumption (Ass1)}: \ P = \text{constant.} \tag{2}$$

When working with rms ac line voltage 115 V/230 V the on-state voltage of the bridge diodes can be underestimated, and

from (1), the expression for the minimum input voltage of the dc–dc onverter is obtained as follows:

$$V_o \text{max} = \text{V\^AC}$$

Assumption (Ass2) : On-state voltage of diodes $= 0$

$$V_{o\text{min}} = V_{CB\text{min}} = (1 - k) \cdot \hat{V}_{\text{AC}}. \tag{3}$$

The energy supplied by the filter capacitance to the dc–dc converter is the same as the energy taken up by filter capacitance from ac line (4). From this equality and from (3), we can obtain the value for the filter capacitor (4)

$$W_{CB-\text{dch}} = \int_{t_c}^{T/2} P \cdot dt = P \cdot \left(\frac{T}{2} - t_c \right)$$

$$= \frac{P}{2 \cdot f} \cdot (1 - 2 \cdot f \cdot t_c)$$

$$W_{\text{line}-CB} = \frac{1}{2} \cdot C_B \cdot \left(V_{CB\text{max}}^2 - V_{CB\text{min}}^2 \right)$$

$$C_B = \frac{P \cdot (1 - 2 \cdot f \cdot t_c)}{\hat{V}_{\text{AC}}^2 \cdot k \cdot (2 - k) \cdot f}. \tag{4}$$

From Fig. 3 and (3), the charging time can be obtained as follows:

$$V_{CB\text{min}} = \hat{V}_{\text{AC}} \cdot \sin(\omega \cdot t_x) = \hat{V}_{\text{ACmin}} \cdot \cos\left(\frac{\pi}{2} - \omega \cdot t_x \right)$$

$$\text{Assumption (Ass3)}: \omega \cdot (t_x + t_c) \approx \frac{\pi}{2}$$

$$t_c = \frac{1}{2 \cdot \pi \cdot f} \cdot \cos^{-1}(1 - k). \tag{5}$$

From Fig. 3, a triangular capacitor charging current can be assumed, then, the electric charge and the capacitor peak current are given by (6). Equation (7) represents the rms value of the capacitor current.

$$\Delta Q_c = \int_{t_x}^{t_x + t_c} I_{\text{chg}}(t) \cdot dt = \frac{1}{2} \cdot \hat{I}_{\text{chg}} \cdot t_c$$

$$\Delta Q_c = C_B \cdot (V_{CB\text{max}} - V_{CB\text{min}})$$

$$= k \cdot C_B \cdot \hat{V}_{\text{AC}}$$

Assumption (Ass4) : Triangular capacitor current

$$\hat{I}_{\text{chg}} = \frac{2 \cdot C_B \cdot V_{\text{cripple}}}{t_c}$$

$$= \frac{2 \cdot C_B \cdot k \cdot \hat{V}_{\text{AC}}}{t_c}. \tag{6}$$

$$I_{C\text{rms}}^2 = I_{\text{chg}-\text{rms}}^2 + I_{\text{dch}-\text{rms}}^2$$

$$I_{\text{chg}-\text{rms}}^2 = \frac{2}{T} \int_0^{t_c} \left(\hat{I}_{\text{chg}} \cdot \left(1 - \frac{t}{t_c} \right) \right)^2 \cdot dt$$

$$= \frac{2}{3} \cdot \hat{I}_{\text{chg}}^2 \cdot t_c \cdot f$$

$$I_{\text{dch}-\text{rms}}^2 = \frac{2}{T} \int_0^{0,5 \cdot T - t_c} I_o^2(t) \cdot dt$$

$$= \frac{2}{T} \cdot \frac{0,5 \cdot T - t_c}{T_s} \cdot \int_0^{T_s} I_o^2(t) \cdot dt$$

$$= (1 - 2 \cdot f \cdot t_c) \cdot I_{\text{orms}}^2$$

$$I_{C\text{rms}}^2 = \frac{2}{3} \cdot \hat{I}_{\text{chg}}^2 \cdot t_c \cdot f + (1 - 2 \cdot f \cdot t_c)$$

$$\cdot I_{\text{orms}}^2$$

$$\text{Assumption (Ass5)}: \frac{T}{2} - t_c \gg T_s. \tag{7}$$

The current through the diodes of the bridge recharge the filter capacitor and circulates across the primary section of the dc–dc converter, because of which, the diodes current depends on the topology of the dc–dc converter. In order to simplify the calculations, we are going to make assumption (Ass6). From Fig. 3 and (Ass4), we can obtain t_d and the rms current through each diode of the bridge as in the following equation:

$$\frac{t_d}{\hat{I}_{chg} + I_{dch}} = \frac{t_c}{\hat{I}_{chg}} \Rightarrow t_d = t_c \cdot \frac{\hat{I}_{chg} + I_{dch}}{\hat{I}_{chg}}$$

$$\hat{I}_D = \hat{I}_{chg} + I_{dch}$$

Assumption (Ass6) : $I_{dch} = I_{oavg}$

$$I_{D-rms}^2 = \frac{1}{T} \int_0^{td} \left(\left(\hat{I}_{chg} + I_{oavg} \right) \cdot \left(1 - \frac{t}{t_d} \right) \right)^2 \cdot dt$$

$$= \frac{1}{3} \cdot \left(\hat{I}_{chg} + I_{oavg} \right)^2 \cdot t_d \cdot f. \tag{8}$$

In order to calculate the average voltage at the input of the switching converter we assume that the capacitor charges and discharges linearly

$$V_{oavg} = V_{CBavg} = \frac{V_{CB\,max} + V_{CB\,min}}{2}$$

Ass7: CB charges and discharges linearly. (9)

IV. DESIGNING THE RECTIFIER TO COMPLY WITH IEC-61 000-3-2:2000 CLASS A

Since the year 2000, line current content is regulated in Europe by IEC61000-3-2:2000 [8], the original version of this regulation was published in 1995.

As the original version, this new standard defines different classes for power electronic equipment: A, B, C, and D. These classes establish different current harmonic limits depending on the use of the electronic equipment. The standard applies for ac line voltages of 220, 230, or 240 V and for input power between 75–600 W

Many PFC circuits have been designed in order to limit the harmonic content of the line current of mains-connected equipment. These circuits can be classified as active or passive circuits. Active PFC solutions are complex, expensive, and generate excessive electromagnetic interference. Passive PFC solutions are simple, reliable, cheap and do not generate electromagnetic interference. Some simple passive circuits with LC [9] filter or LCD [10], [11] filter have been proposed.

According to the new version of the standard, several low-power single-phase circuits are classified as Class A, for example, audio equipment, battery chargers, nonportable tools, etc.

Class A harmonic limits allow more distortion at low power levels, due to this, it is easier to achieve compliance in Class A. For equipment classified as Class A, the maximum allowed level of line harmonic is the same whatever the line current waveform is and whatever the input power between 75–600 W is.

If the value of the bulk capacitor is set by following the criterion shown in (1), the rectifier achives compliance in Class A. The expressions shown at the bottom of the page give an approximation of the maximum power for different values of k, at which the full-bridge rectifier with capacitor filter complies with EN-61000-3-2:2000 Class A regulation. These limit values were obtained in the laboratory from a prototype, and confirmed with simulation results.

Table I shows the ratio of class A harmonic limits and harmonic components in the rectifier under the four limit conditions. The value for the bulk capacitor was calculeted by using (4) and (5). The line voltage used was 220 V which is the minimum ac line voltage defined in the standard, this value gives us the worst case.

The ratio of Class A harmonic limits and harmonic content of the input current, for the full-bridge rectifier under the four conditions presented above are shown in Table I.

The minimum ratio between Class A harmonic limits and current harmonic components in the rectifier are shadowed in Table I.

1) $I_{\lim it,A}/I_{h1} \Rightarrow V = 220$ V; $P = 150$ W; $K = 0.3$.
2) $I_{\lim it,A}/I_{h2} \Rightarrow V = 220$ V; $P = 140$ W; $K = 0.25$.
3) $I_{\lim it,A}/I_{h3} \Rightarrow V = 220$ V; $P = 125$ W; $K = 0.2$.
4) $I_{\lim it,A}/I_{h4} \Rightarrow V = 220$ V; $P = 110$ W; $K = 0.15$.

In the range of low-power applications under 160 W it is possible to comply with IEC61000-3-2:2000 Class A with the full-bridge rectifier plus C filter, if the value of the capacitor is set following (1).

V. ANALYSIS OF THE VOLTAGE DOUBLER

In Fig. 1, voltage doubler operation appears when the switch is in the 115-V position. The upper capacitor C and the lower one C alternately charge to peak line voltage (see Fig. 4). In order to analyze the voltage doubler topology a new assumption is going to be done (Ass8). Whenever the input voltage of the dc–dc converter, V_o, is at instantaneous minimum, one capacitor is at its minimun, but the other capacitor is half way between peak and minimum voltage; from (Ass8) and (Ass7), the

---

$$K = 0.3; V = 220 \text{ V} \Rightarrow P \le 150 \text{ W} \qquad K = 0.25; V = 220 \text{ V} \Rightarrow P \le 140 \text{ W}$$
$$V = 230 \text{ V} \Rightarrow P \le 155 \text{ W} \qquad V = 230 \text{ V} \Rightarrow P \le 145 \text{ W}$$
$$V = 240 \text{ V} \Rightarrow P \le 160 \text{ W} \qquad V = 240 \text{ V} \Rightarrow P \le 150 \text{ W}$$
$$K = 0.2; V = 220 \text{ V} \Rightarrow P \le 125 \text{ W} \qquad K = 0.15; V = 220 \text{ V} \Rightarrow P \le 110 \text{ W}$$
$$V = 230 \text{ V} \Rightarrow P \le 130 \text{ W} \qquad V = 230 \text{ V} \Rightarrow P \le 115 \text{ W}$$
$$V = 240 \text{ V} \Rightarrow P \le 135 \text{ W} \qquad V = 240 \text{ V} \Rightarrow P \le 120 \text{ W}$$

TABLE I
RATIO OF CLASS A HARMONIC LIMITS AND
HARMONIC COMPONENTS IN THE RECTIFIER

h	$I_{\text{limit,A}}/I_{h1}$	$I_{\text{limit,A}}/I_{h2}$	$I_{\text{limit,A}}/I_{h3}$	$I_{\text{limit,A}}/I_{h4}$
3	3.33	3.6	4	4.45
5	2.43	2.45	2.52	2.63
7	2.88	2.67	2.47	2..3
9	2.19	2.24	2.04	1.73
11	1.86	2.08	2.33	2.12
13	1.39	1.39	1.51	1.71
15	1.3	1.22	1.15	1.25
17	1.25	1.34	1.22	1.15
19	1.16	1.27	1.35	1.17
21	1.23	1.19	1.317	1.28
23	1.29	1.25	1.224	1.38
25	1.21	1.32	1.22	1.3
27	1.21	1.26	1.31	1.227
29	1.28	1.22	1.34	1.23
31	1.25	1.28	1.28	1.3
33	1.22	1.32	1.25	1.35
35	1.26	1.27	1.3	1.33
37	1.28	1.25	1.35	1.28
39	1.25	1.3	1.33	1.29

Fig. 4. Capacitor voltage and capacitor current for the voltage doubler.

minimum and maximum input voltages of the switching converter can be expressed as

$$V_{o\min} = V_{C\min} + V_{C\text{avg}} = V_{C\min} + \frac{V_{C\max} + V_{C\min}}{2}$$
$$V_{o\max} = V_{C\max} + V_{C\text{avg}} = V_{C\max} + \frac{V_{C\max} + V_{C\min}}{2}$$
$$V_{C\max} = \hat{V}_{\text{AC}}$$

Assumption(Ass8): When V_o is at instantaneous
minimum one capacitor is at its minimum,
the other capacitor is half way between peak
and minimum voltage. (10)

From (1) and (10), we can obtain the minimum and maximum values for the input voltage of the switching converter as a function of the line voltage

$$V_{o\min} = \frac{(4 - 3 \cdot k')}{2} \cdot \hat{V}_{\text{AC}}; \quad V_{o\max} = \frac{(4 - k')}{2} \cdot \hat{V}_{\text{AC}}$$
$$\text{here} \Rightarrow V_{o\max} - V_{o\min} = V_{C\max} - V_{C\min} = \hat{V}_{\text{AC}} \cdot k'.$$
(11)

Each capacitor must supply half the energy required by the switching regulator for an entire line cycle during $(T - t_c)$. This
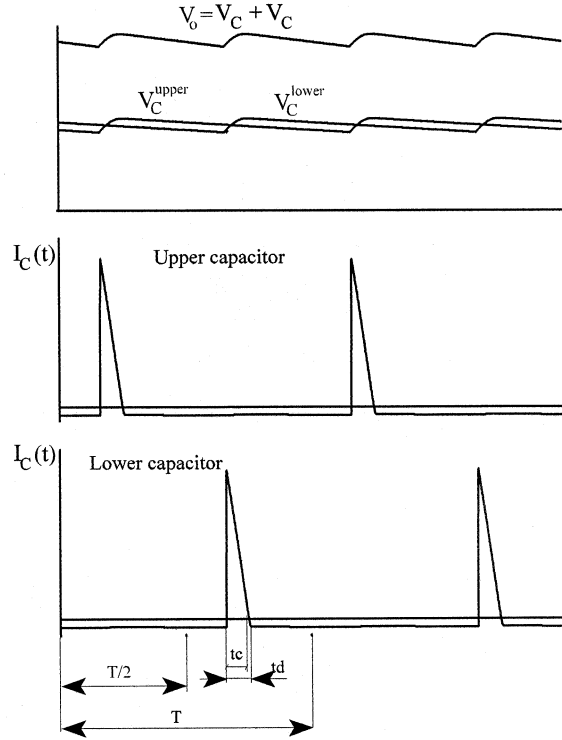
energy is equal to the energy taken up by the capacitor from the ac line

$$W_{C-\text{dch}} = \frac{1}{2} \cdot \int_{t_c}^{T} P \cdot dt = \frac{1}{2} \cdot P \cdot (T - t_c)$$
$$= \frac{P}{2 \cdot f} \cdot (1 - f \cdot t_c)$$
$$W_{\text{line}-C} = \frac{1}{2} \cdot C \cdot (V_{C\max}^2 - V_{C\min}^2)$$
$$C = \frac{P \cdot (1 - f \cdot t_c)}{\hat{V}_{\text{AC}}^2 \cdot k' \cdot (2 - k') \cdot f}.$$
(12)

From assumptions (Ass3) and (Ass4), the charging time and the capacitor peak current for voltage doubler operation are given by

$$t_c = \frac{1}{2 \cdot \pi \cdot f} \cdot \cos^{-1}(1 - k');$$
$$\hat{I}_{\text{chg}} = \frac{2 \cdot C \cdot V_{C\text{ripple}}}{t_c} = \frac{2 \cdot C \cdot k' \cdot \hat{V}_{\text{AC}}}{t_c}.$$
(13)

From assumptions (Ass4), (Ass5), and (Ass6) the rms current through each capacitor and each diode can be expressed as shown in (14) and (15)

$$I_{\text{chg}-\text{rms}}^2 = \frac{1}{T} \int_0^{t_c} \left(\hat{I}_{\text{chg}} \cdot \left(1 - \frac{t}{t_c}\right) \right)^2 \cdot dt = \frac{1}{3} \cdot \hat{I}_{\text{chg}}^2 \cdot t_c \cdot f$$
$$I_{\text{dch}-\text{rms}}^2 = \frac{1}{T} \int_0^{T-t_c} I_o^2 \cdot dt = \frac{1}{T} \cdot \frac{T - t_c}{T_s} \cdot \int_0^{T-s} I_o^2 \cdot dt$$
$$= (1 - f \cdot t_c) \cdot I_{o\text{rms}}^2$$
(14)

$$I_{C\text{rms}}^2 = \frac{1}{3} \cdot \hat{I}_{\text{chg}}^2 \cdot t_c \cdot f + (1 - f \cdot t_c) \cdot I_{o\text{rms}}^2$$

$$I_{D-\text{rms}}^2 = \frac{1}{T} \int_0^{t_d} \left(\left(\hat{I}_{\text{chg}} + I_{o\text{avg}} \right) \cdot \left(1 - \frac{t}{t_d} \right) \right)^2 \cdot dt$$

$$= \frac{1}{3} \cdot \left(\hat{I}_{\text{chg}} + I_{o\text{avg}} \right)^2 \cdot t_d \cdot f. \tag{15}$$

VI. DUAL-RANGE OPERATION

In the last sections, the bridge and voltage doubler topologies are analyzed in a separate way. In order to design the converter for dual-range operation, some points must be taken in account.

With the switched dual-range input section (115-V doubler or 230-V bridge) filter capacitor requirements are determined by the voltage doubler configuration. The steps which must be followed in the design process are the following.

- Design of the voltage doubler: $k' \in (0, 2 \div 0, 4)$ (value for the capacitors, value of currents, etc.).
- With the value for the capacitor calculated in the first step, the parameters for the bridge topology can be obtained. Solving (3), (4), and (5) we get the following equation:

$$V_{CB\,\text{max}}^2 - V_{CB\,\text{min}}^2 = \frac{P}{f \cdot C_B} \cdot (1 - 2 \cdot f \cdot t_c)$$

$$V_{CB\,\text{max}}^2 - V_{CB\,\text{min}}^2 = \hat{V}_{\text{AC}}^2 - \left(\hat{V}_{\text{AC}} \cdot \cos\omega \cdot t_c \right)^2$$

$$\hat{V}_{\text{AC}}^2 - \left(\hat{V}_{\text{AC}} \cdot \cos\omega \cdot t_c \right)^2 = \frac{P}{f \cdot C_B} \cdot (1 - 2 \cdot f \cdot t_c). \tag{16}$$

In order to calculate t_c from the last equation, a polynomial approximation was done by using the Matlab function *polyfit*. The polynomial curve fitting was done for $\{\omega t_c \in (0, 3 \div 1)\}$ which from (5) corresponds with a wide range of $k\{k \in (0, 05 \div 0, 46)\}$. We can make the following substitution:

$$\cos^2 (\omega \cdot t_c) = -0{,}2582 \cdot (\omega \cdot t_c)^2 - 0{,}5813 \cdot \omega \cdot t_c + 1{,}1206. \tag{17}$$

From (16) and (17), we attain the following second-order equation, from which we calculate the value of t_c:

$$t_c^2 + \left[\frac{0, 2 \cdot P}{C \cdot f^2 \cdot \hat{V}_{\text{AC}}^2} + \frac{0, 37}{f} \right] \cdot t_c -$$

$$- \left[\frac{0, 12}{f^2 \cdot \pi^2} + \frac{P}{\pi^2 \cdot C \cdot f^3 \cdot \hat{V}_{\text{AC}}^2} \right] = 0. \tag{18}$$

Once t_c is obtained, the equations for bridge operation presented in Section III can be used for calculating the parameters.

VII. EXPERIMENTAL RESULTS

A dual-range 200-W switching power supply is tested. In this case, we already have designed the power supply, and we will apply the method presented in the last paragraphs, in order to verify its validity, by comparing the theoretical results with experimental results. The power supply is going to be tested when connected to the 230-V/50-Hz ac line, because of which, the full-bridge configuration is adopted. The parameters for the dc–dc converter, for the ac line and the value of each capacitor C, are the following:
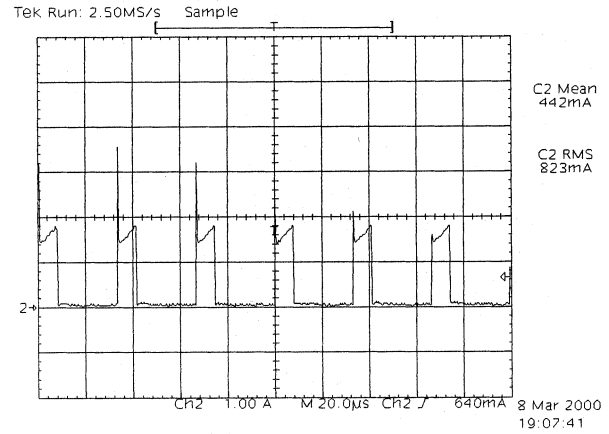
$$\hat{V}_{\text{AC}} = 324 \text{ V}$$

Fig. 5.   Current drawn by dc–dc converter. RMS value and average value on the right side.

$$f = 50 \text{ Hz}$$
$$P = 134 \text{ W}$$
$$I_{o\text{avg}} = 0.442 \text{ A}$$
$$I_{o\text{rms}} = 0.823 \text{ A}$$
$$C = 150 \ \mu\text{F}$$
$$C_B = 75 \ \mu\text{F}.$$

Once we know the value for t_c by applying (18), we can use the equations obtained in Section III in order to calculate the currents and voltages in the ac–dc converter. By using those equations, we obtain the following results:

$$k = 0.1557$$
$$V_{o\,\text{min}} = 274 \text{ V}$$
$$V_{o\,\text{max}} = 324 \text{ V}$$
$$V_{o\text{avg}} = 299 \text{ V}$$
$$I_{C\text{rms}} = 1.27 \text{ A}$$
$$\hat{I}_{\text{chg}} = 4.2 \text{ A}$$
$$I_{D\text{rms}} = 0.846 \text{ A}$$
$$\hat{I}_D = 4.65 \text{ A}.$$

The current drawn by the dc–dc converter is shown in Fig. 5. On the right side of the figure are the rms value and the average value. The dc voltage at the output of the rectifier is shown in Fig. 6. On the right side of Fig. 6 are the minimum, maximum, and average values of the dc voltage. The capacitor current and the dc voltage are presented in Fig. 7. On the right side of the figure are the rms value and the peak value of the capacitor current.

The current which circulates through the diodes of the bridge and the dc voltage are presented in Fig. 8. On the right side of this figure are the rms value and the peak value of this current. The current through each diode of the bridge is obtained by using the following equation:

$$I_{D\text{rms}} = \frac{I_{\text{bridge}-\text{rms}}}{\sqrt{2}} = \frac{1{,}150 \text{ A}}{\sqrt{2}} = 0{,}813 \text{ A}. \tag{19}$$

Table II shows the line current harmonics up to the 39th for the case under analysis $\mathbf{I_{h-1}}$, the Class A limits, and the ratio of Class A harmonic limits and harmonic content of the input
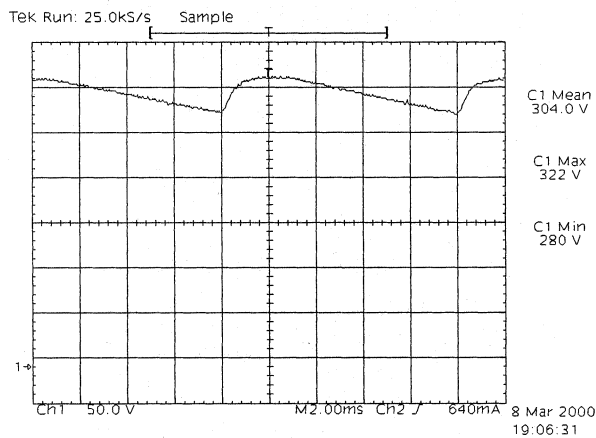
Fig. 6. DC-link voltage. Average, maximum, and minimum values on the right side.
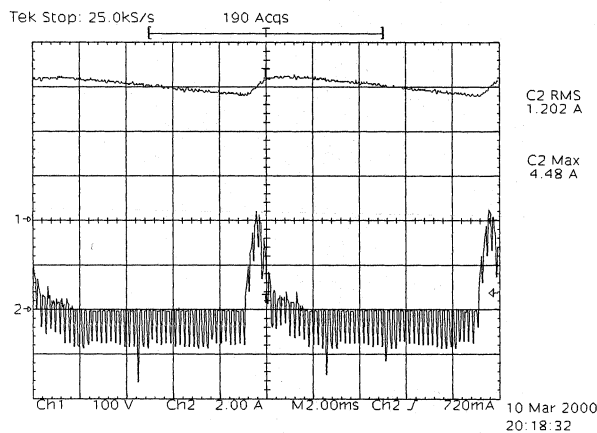

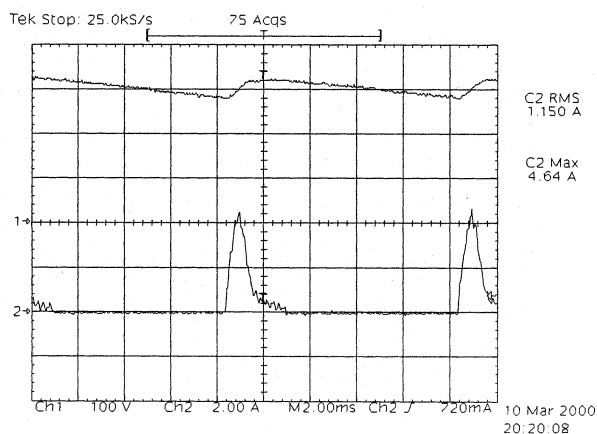Fig. 7. DC-link voltage and capacitor current. RMS value and peak value of the capacitor current on the right side.

Fig. 8. DC-link voltage and current through the bridge. RMS value and peak value on the right side.

TABLE II
RATIO OF CLASS A HARMONIC LIMITS AND HARMONIC COMPONENTS IN THE RECTIFIER FOR DIFFERENT VALUES OF THE BULK CAPACITOR

		$C_B=75\mu F$		$C_B=50\mu F$	
h	$I_{limit,A}$ Arms	I_{h-1} Arms	$I_{limit,A}/I_{h-1}$	I_{h-2} Arms	$I_{limit,A}/I_{h-2}$
3	2.3	0.568	4.05	0.558	4.12
5	1.14	0.485	2.35	0.427	2.67
7	0.77	0.382	2.015	0.283	2.72
9	0.4	0.285	1.4	0.185	2.16
11	0.33	0.21	1.57	0.158	2.08
13	0.21	0.17	1.23	0.157	1.33
15	0.15	0.178	0.84	0.142	1.05
17	0.1324	0.152	0.87	0.12	1.1
19	0.1184	0.13	0.91	0.107	1.1
21	0.1071	0.1	1.07	0.098	1.09
23	0.0978	0.069	1.417	0.085	1.15
25	0.09	0.05	1.8	0.076	1.18
27	0.083	0.041	2.03	0.06	1.39
29	0.0776	0.035	2.21	0.045	1.72
31	0.0726	0.027	2.7	0.038	1.91
33	0.0682	0.018	3.78	0.03	2.27
35	0.0643	0.013	4.94	0.025	2.57
37	0.0608	0.013	4.67	0.018	3.37
39	0.0577	0.012	4.8	0.017	3.39

current. From Table II, there is no compliance with regulation at the harmonics (15, 17, 19, 21), shadowed in Table II (columns 3 and 4).

For the case under analysis, the compliance with IEC-61000-3-2-Class A regulation can be achieved if the value for the capacitor is set by using the criterion shown in Section IV. For $P = 134$ W and $V = 230$ V,

$$V = 230\,\text{V} \quad P > 130\,\text{W} \Rightarrow k > 0.2.$$

If maintaining the value of the input power $P = 134$, we change the value of the capacitor to $C_B = 50\ \mu\text{F}$, (now $k = 0.222$), the rectifier complies with Class A regulation as shown in columns 5 and 6 of Table II.

$\mathbf{I_{h-2}}$ represents the line current harmonics up to the 39th for the new conditions, ($P = 134$ W; $C_B = 50\ \mu\text{F}$; $k = 0.222$).

VIII. CONCLUSION

To conclude this paper, note that we have achieved the goals that we set at the beginning. Specifically, we have obtained simple expressions for the currents and voltages in the ac–dc converter working as a full-bridge rectifier or as a voltage doubler. Experimental results have confirmed the validity of the proposed design method.

For Class A compliance, the rectifier with C filter is an interesting option when working with $P < 160$ W.

REFERENCES

[1] J. Kammerloher, *Hockfrequenztechnik III*. Leipzig, Germany: C. F. Winter, 1942, p. 189.

[2] O. H. Schade, "Analysis of rectifier operation," *Proc. IRE*, vol. 31, no. 7, pp. 341–361, July 1943.

[3] *RCA Designers Handbook*, RCA Solid State Division, Somerville, NJ, 1971, pp. 249–262.

[4] A. Lieders, "Single-phase rectifier circuits with CR filters, Part 1," *Electron. Comp. Applicat.*, vol. 1, no. 3, pp. 21–33, May 1979.

[5] ——, "Single-phase rectifier circuits with CR filters, Part 2," *Electron. Comp. Applicat.*, vol. 1, no. 4, pp. 37–49, Aug. 1979.

[6] B. W. Sherman and K. A. Hamacher, "Power supply design in the undergraduate curriculum," *IEEE Trans. Educ.*, vol. 40, pp. 278–281, Nov. 1997.

[7] "Line Input AC to DC conversion and input filter capacitor selection," in *Proc. Unitrode Power Supply Design Seminar*, 1994, pp. I1-1–I1-6.

[8] *Electromagnetic Compatibility (EMC) Part 3-2: Limits for Harmonic Current Emissions (Equipment Input Current $\leq$ 16 A Per Phase)*, IEC-61 000-3-2, 2000.

[9] M. M. Jovanovic and D. E. Crow, "Merits and limitations of full-bridge rectifier with *LC* filter in meeting IEC-1000-3-2 harmonic limit specifications," *IEEE Trans. Ind. Applicat.*, vol. 33, pp. 551–557, Mar./Apr. 1997.

[10] R. Redl, "An economical single-phase passive power-factor-corrected rectifier: Topology, operation, extensions and design for compliance," in *Proc. IEEE APEC'98*, 1998, pp. 454–460.

[11] W. M. Lin, M. M. Hernando, A. Fernadez, J. Sebastian, and P. J. Villegas, "A new topology for passive PFC circuit design to allow AC-to-DC converters to comply with the new version of IEC1000-3-2 regulation," in *Proc. IEEE PESC*, 2002, pp. 2050–2055.

Jesus Doval-Gandoy (M'99) received the M.Sc. degree from the Polytechnic University of Madrid, Madrid, Spain, in 1991, and the Ph.D. degree from the University of Vigo, Vigo, Spain, in 1999.

From 1991 to 1994, he worked in industry. He is currently an Associate Professor at the University of Vigo. His research interests are in the area of power converters connected to mains.

Carlos Castro received the M.Sc. degree in 1996 from the University of Vigo, Vigo, Spain, where he is currently working toward the Ph.D. degree.

He is also currently an Assistant Professor at the University of Vigo. His research interests are control techniques and modeling of dc–dc power converters.

Moises C. Martínez is currently working toward the B.Sc. degree at the University of Vigo, Vigo, Spain.

His research interests are dc–dc power converters and PWM rectifiers.