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Modeling and Computer Aided Analysis of Switching Regulators

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Abstract - A unique model of pulse-width-modulated (PWM) converters, operating in the continuous conduction mode, is developed. This model is compatible with general purpose electronic circuit programs such as SPICE. It can be used to simulate dc, small signal and transient behavior of PWM converters. The simulation of switching regulators is simplified by using this equivalent circuit model to replace the nonlinear part of the PWM converters. An effective switching regulator analysis program, called SWAN, is developed and used to simulate small-signal characteristics of a switching regulator.

I. INTRODUCTION

Analysis of switching regulators is complicated due to their switching behavior. Some analytical approaches [1] [2] [3] [4] [5] [6] [7] have been proposed. These approaches can be used to model current-mode switching regulator systems and to drive the transfer blocks required for the design of the transfer function of the feedback path. The main difficulty of these methods in practical applications is the extensive effort required for deriving analytical averaged models and transfer functions for practical systems.

In this paper, a PWM converter model is described. Based on this model a switching-regulator analysis program (SWAN) is developed. This program was linked to SPICE through an interface program and a new subcircuit model for the PWM converter. This was implemented by revising the input processing and run control subroutines of SPICE. The new implementation allows the analysis of the system under study to be carried out effectively and conveniently from the input of the system's schematic.

To examine the model and implemented SWAN program, this paper uses the parameters in [6] as an example, and presents the response curves of a real current-injected control regulator.

II. POWER STAGE MODEL

Consider a buck/boost regulator employing current injected in continuous condition mode as shown in Figure 1 [6]. The small-signal block diagram of the switching regulator is shown in Figure 2.

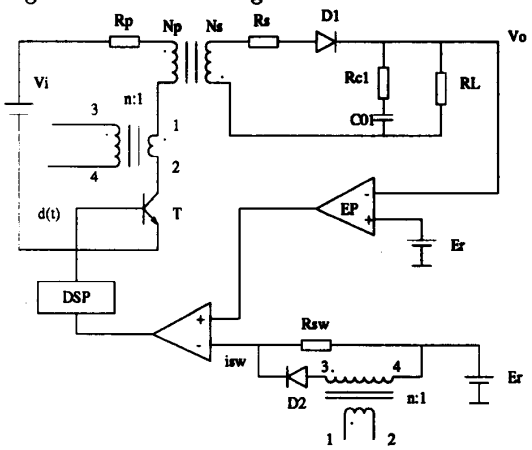

Figure 1: Circuit schematic of a current-injected control regulator

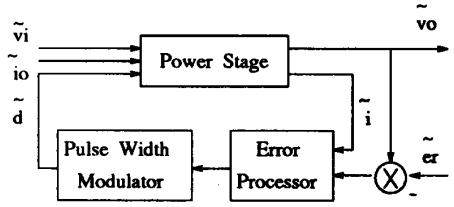

Figure 2: Small-signal block diagram of the switching regulator

The PWM DC-DC converter is nonlinear, discrete and time varying. For each switching cycle, the power stage can be modeled by two linear circuits for continuous inductor current operation. When the switch is on, the power stage is described by the following equations:

$$\dot{x} = A_1 x + B_1 u \quad (1)$$

$$y = C_1 x + E_1 u \quad (2)$$

When the switch is off, the power stage takes the following form:

$$\dot{x} = A_2 x + B_2 u \quad (3)$$

$$y = C_2 x + E_2 u \quad (4)$$

Using the state space averaging method described by R.D.Middlebrook and S.Cuk [8], one can replace the state space description of two linear circuits by a single state space description which represents the average effect of the system through one cycle of operation:

$$\dot{x} = d(A_1x + B_1u) + d'(A_2x + B_2u) \quad (5)$$

$$y = d(C_1x + E_1u) + d'(C_2x + E_2u) \quad (6)$$

where

$d = T_{on}/T_s$

$d' = T_{off}/T_s$

T_s is the period of the switching cycle, $T_{on} = T_s d$ is the period during which the switch is on, $T_{off} = T_s d'$ is the period during which the switch is off, as shown in Figure 3.

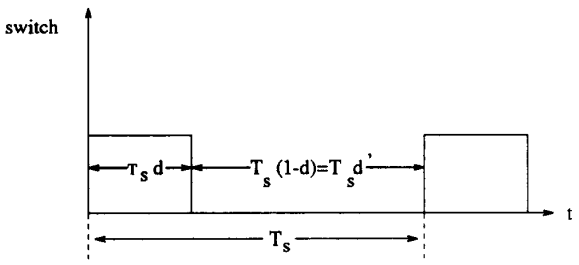

Figure 3: T_{on} and T_{off}

From equations (5) and (6), we have:

$$\dot{x} = (A_1d + A_2d')x + (B_1d + B_2d')u \triangleq Ax + Bu \quad (7)$$

$$y = (C_1d + C_2d')x + (E_1d + E_2d')u \triangleq Cx + Eu \quad (8)$$

where

$A = A_1d + A_2d'$

$B = B_1d + B_2d'$

$C = C_1d + C_2d'$

$E = E_1d + E_2d'$

Now let us assume that the duty-cycle ratio is a constant, *i.e.*, $d = D$ and $d' = D'$ (steady-state DC duty-cycle ratio). we then have:

$A = A_1D + A_2D'$

$B = B_1D + B_2D'$

$C = C_1D + C_2D'$

$E = E_1D + E_2D'$

Equations (7) and (8) represent a linear system. In order to study the small signal characteristics, we can introduce the voltage variable $\tilde{v}_i$, the duty-cycle variable $\tilde{d}$ and the output current disturbance $\tilde{i}_o$ into the system. We then have that $v_i = V_i + \tilde{v}_i$, $\tilde{i}_o = 0 + \tilde{i}_o$, $d = D + \tilde{d}$, and $d' = D' - \tilde{d}$. Here V_i is the DC input voltage, D and D' are the steady-state duty-cycle ratios, during T_{on} and T_{off} respectively.

These small signal disturbances cause corresponding disturbances to the input variables, state variables, and output stead-state variables. That is, $u = U + \tilde{u}$, $x = X + \tilde{x}$, and $y = Y + \tilde{y}$.

With the small disturbances, eqs. (7) and (8) become:

$$\begin{aligned}\dot{\tilde{x}} &= Ax + Bu \\ &= [(D + \tilde{d})A_1 + (D' - \tilde{d})A_2](X + \tilde{x}) \\ &\quad +[(D + \tilde{d})B_1 + (D' - \tilde{d})B_2](U + \tilde{u}) \\ &= AX + BU + A\tilde{x} + B\tilde{u} + [(A_1 - A_2)X + (B_1 - B_2)U]\tilde{d} \\ &\quad +[(A_1 - A_2)\tilde{x} + (B_1 - B_2)\tilde{u}]\tilde{d} \quad (9)\end{aligned}$$

$$\begin{aligned}y &= Y + \tilde{y} \\ &= [(D + \tilde{d})C_1 + (D' - \tilde{d})C_2](X + \tilde{x}) \\ &\quad +[(D + \tilde{d})E_1 + (D' - \tilde{d})E_2](U + \tilde{u}) \\ &= CX + EU + C\tilde{x} + E\tilde{u} + [(C_1 - C_2)X + (E_1 - E_2)U]\tilde{d} \\ &\quad +[(C_1 - C_2)\tilde{x} + (E_1 - E_2)\tilde{u}]\tilde{d} \quad (10)\end{aligned}$$

Equations (9) and (10) show that the description of the disturbance state space is nonlinear. Assuming that the ac variations are very small in magnitude compared with their steady-state values, *i.e.*, $\tilde{u}/U << 1$, $\tilde{d}/D << 1$, and $\tilde{x}/X << 1$, we can neglect the nonlinear terms. The simplified eqs. (9) and (10) are then obtained for the steady-state and dynamic models.

Steady-State (dc) Model:

$$X = -A^{-1}BU \quad (11)$$

$$Y = (E - CA^{-1}B)U \quad (12)$$

Linear Dynamic (ac) Model:

$$\dot{\tilde{x}} = A\tilde{x} + B\tilde{u} + [(A_1 - A_2)X + (B_1 - B_2)U]\tilde{d} \quad (13)$$

$$\tilde{y} = C\tilde{x} + E\tilde{u} + [(C_1 - C_2)X + (E_1 - E_2)U]\tilde{d} \quad (14)$$

III. POWER STAGE TRANSFER FUNCTIONS

The power stage transfer functions are obtained by the following derivation.

Taking the Laplace transform, equations (13) and (14) can be expressed as follows:

$$\begin{aligned}\tilde{x}(s) &= (sI - A)^{-1} \\ &\quad (B\tilde{u}(s) + [(A_1 - A_2)X + (B_1 - B_2)U]\tilde{d}(s)) \quad (15)\end{aligned}$$

$$\begin{aligned}\tilde{y}(s) &= C\tilde{x}(s) + E\tilde{u}(s) \\ &\quad +[(C_1 - C_2)X + (E_1 - E_2)U]\tilde{d}(s) \quad (16)\end{aligned}$$

Substituting equation (15) into (16), one has that

$$\begin{aligned}\tilde{y}(s) &= [C(sI - A)^{-1}B + E]\tilde{u}(s) \\ &\quad +(C(sI - A)^{-1}[(A_1 - A_2)X + (B_1 - B_2)U] \\ &\quad +[(C_1 - C_2)X + (E_1 - E_2)U])\tilde{d}(s) \quad (17)\end{aligned}$$

Equation (17) can be rewriten in matrix form:

$$\tilde{y}(s) = \begin{bmatrix} P & Q \end{bmatrix} \begin{pmatrix} \tilde{u}(s) \\ \tilde{d}(s) \end{pmatrix} \tag{18}$$

where

$$\begin{aligned} P &= C(sI - A)^{-1}B + E \\ Q &= C(sI - A)^{-1}[(A_1 - A_2)X + (B_1 - B_2)U] \\ &\quad +[(C_1 - C_2)X + (E_1 - E_2)U] \\ \tilde{y}(s) &= \begin{bmatrix} \tilde{v}_o(s) & \tilde{i}_p(s) \end{bmatrix}^T \end{aligned}$$

and

$$\begin{bmatrix} \tilde{u}(s) & \tilde{d}(s) \end{bmatrix}^T = \begin{bmatrix} \tilde{v}_i(s) & \tilde{i}_o(s) & \tilde{d}(s) \end{bmatrix}^T$$

If we now let

$$P = \begin{bmatrix} P_{11} & P_{12} \\ P_{21} & P_{22} \end{bmatrix} \tag{19}$$

and

$$Q = \begin{pmatrix} Q_1 \\ Q_2 \end{pmatrix} \tag{20}$$

We then have

$$\begin{pmatrix} \tilde{v}_o(s) \\ \tilde{i}_p(s) \end{pmatrix} = \begin{bmatrix} P_{11} & P_{12} & Q_1 \\ P_{21} & P_{22} & Q_2 \end{bmatrix} \begin{pmatrix} \tilde{v}_i(s) \\ \tilde{i}_o(s) \\ \tilde{d}(s) \end{pmatrix} \tag{21}$$

where

$$\begin{aligned} P_{11} &= \tilde{v}_o(s)/\tilde{v}_i(s) \\ P_{12} &= \tilde{v}_o(s)/\tilde{i}_o(s) \\ P_{21} &= \tilde{i}_p(s)/\tilde{v}_i(s) \\ P_{22} &= \tilde{i}_p(s)/\tilde{i}_o(s) \\ Q_1 &= \tilde{v}_o(s)/\tilde{d}(s) \\ Q_2 &= \tilde{i}_p(s)/\tilde{d}(s) \end{aligned}$$

The small-signal transfer function block diagram of the converter is shown in Figure 4. In this diagram, F_M is the duty-cycle modulator transformer function, F_{ac} is the error processor ac loop transformer function, and F_{dc} is the error processor dc loop transformer function.

IV. PWM CONVERTER MODEL

In order to use the proposed program to automatically obtain the coefficient matrices A_1, B_1, C_1 and E_1 of the PWM converter during the period T_{on}, and the coefficient matrices A_2, B_2, C_2 and E_2 during the period T_{off}, we developed an equivalent circuit model for the

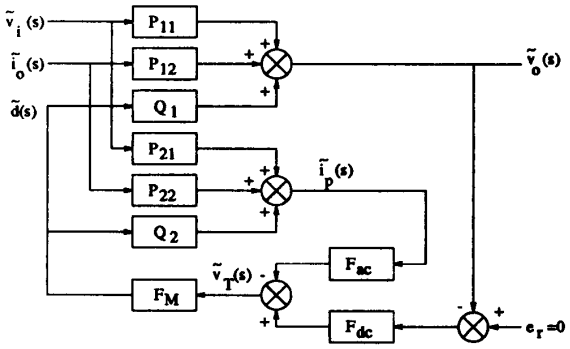

Figure 4: The transfer function block diagram of the converter

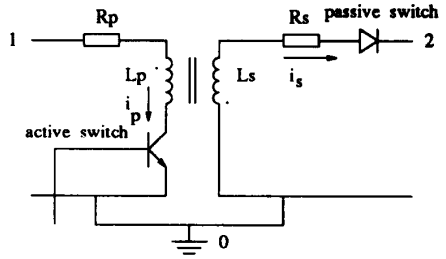

Figure 5: A PWM converter

nonlinear converter. A PWM converter circuit is shown in Figure 5.

The electronic switches (active switch and passive switch) are synchronously controlled by a PWM. The active switch and the passive switch are always in opposite states. The switching converter has different circuit topology for each interval T_{on} and T_{off} in one cycle of operation. The analysis is complicated because most available analysis packages cannot process two different input descriptions when completing one analysis run. The other difficulty is that there are some superfluous elements because the transistor and the diode operate in switching mode.

During T_{on}, the active switch is closed and the passive switch is opened. The converter is described by

$$v_1(t) = R_P + i_P(t) + N_P \frac{d\phi(t)}{dt} \tag{22}$$

During T_{off}, the active switch is opened and the passive switch is closed. The converter is described by

$$v_2(t) = R_S + i_S(t) + N_S \frac{d\phi(t)}{dt} \tag{23}$$

We use the magnetic flux $\phi(t)$ as the state variable instead of two different state variables $i_P(t)$ and $i_S(t)$. Equations (22) and (23) then become:

$$v_1(t) = R_P \frac{N_P}{L_P} \phi(t) + N_P \frac{d\phi(t)}{dt} \tag{24}$$

$$v_2(t) = R_S \frac{N_S}{L_S}\phi(t) + N_S \frac{d\phi(t)}{dt} \qquad (25)$$

Close examination of the PWM converter reveals that it relies on a nonlinear switched inductor to serve as a temporary energy storage element between the input and output terminals. Hence, modeling and simulation of switch mode converters can be simplified if the nonlinear part is replaced by an equivalent circuit.

An equivalent circuit which satisfies eqs. (24) and (25) is shown in Figure 6 and is called an SCM subcircuit. By using this model, the two linear equivalent circuit models with different topology for a switching converter are replaced by one, and superfluous elements in the circuit are eliminated. This equivalent circuit can be used to describe the average behavior of the switch mode converter in the time and frequency domains.

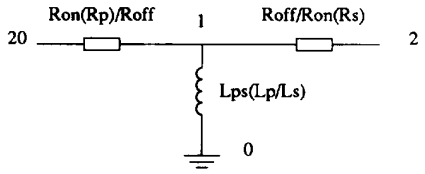

Figure 6: Equivalent circuit model

The circuit of Figure 6 can be easily simulated in the SPICE program. Its corresponding subcircuit description card is shown in Table 1.

.SUBCKT	SCM	1	2	3
Ron	1	20	1.0E-10	1
Roff	1	2	1.0E+20	3
Lps	0	1	1.0E-10	2
.ENDS	SCM			

Table 1: SCM Subcircuit Description Card

V. THE SWAN PROGRAM

A switching regulator analysis program (SWAN) was developed and linked to SPICE. The functional block diagram of the SWAN and the SPICE interface is shown in Figure 7.

In Figure 7, READIN* and RUNCON* are modifications of the READIN and RUNCON subroutines of SPICE. The revision includes the addition of new common blocks, establishing new data fields and new tables, and modifying certain pointers and setting some new ones.

The modified READIN*, RUNCON* and FIND* subroutines are described below.

*READIN**

Subroutine READIN performs the input processing of SPICE and handles the element cards and the device

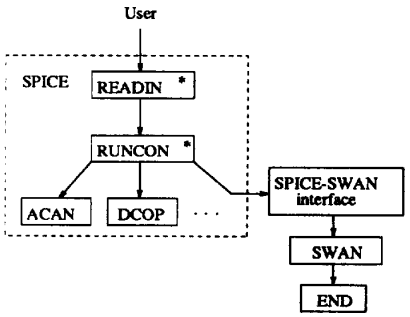

Figure 7: Functional Block Diagram of SWAN and SPICE Interface

models. It calls the subroutine CARD to scan the input lines, it calls the subroutine FIND to establish data chained lists according to the elements' name, ANAME, and type, ID. Or, it can search the list of IDs for an element with name ANAME, and call subroutine RUNCON to process the Run Control Card.

In subroutine READIN, each field of one input line is stored in a temporary data field (see Table 2). The temporary data field consists of four tables: table IFIELD in which information such as names, node-to, node-from, and value of an element, or device, are stored, table ICODE which points at attributes of IFIELD, table IDELIM in which separators are recorded, and table ICOLUM which stores column numbers of separators.

IFLD	IFIELD	ICODE	IDELIM	ICOLUM
1	element name	1	separator	column no. of separator
2	node 1	0	separator	col. no.of sep.
3	node 2	0	separator	col. no.of sep.
4	value	0	separator	col. no.of sep.
5		-1		
.	.	.	.	.

Table 2

The main data of a circuit analysis program are the element names, node numbers, and the element values. The semantic analysis of the program has to store these data in corresponding data tables according to data structures. For control cards, the program sets analysis marks and records analysis requirements. In SPICE, the data of each element and device are stored, respectively, in two tables - an integer table and a real table. As an example, a resistor table is shown in Table 3.

After being processed by the subroutine CARD, a resistor input description statement, for example *R1_8_13_50*, is stored in a temporary data field in the form shown in Table 4(a). After being processed by the subroutine READIN, the final form is shown in Tables 4(b) and 4(c).

	NODPLC(*)			VALUE(*)	
-1	O/ID				
LOC+0	chain pointer			VALUE(*)	
+1	LOCV	→	LOCV	resistor name	
+2	node 1		+1	conductance value	
+3	node 2		+2	resistor value	
+4			+3		
+5			+4		
+6					
+7					

Table 3

IFLD	IFIELD	ICODE	IDELIM	ICOLUM
1	R1	1	␣	3
2	8	0	␣	5
3	13	0	␣	8
4	50	0	␣	11
5		-1		
6				
7				

(a)

	NODPLC(*)
-1	0
LOC	0
+1	LOCV
+2	8
+3	13
+4	
+5	
+6	
+7	

(b)

	VALUE(*)
LOCV	R1
+1	0.02
+2	50
+3	
+4	

(c)

Table 4

Subroutine READIN* is the modified version of READIN for processing input description statements of SPICE. A new input description statement for an element or device includes name, node-to, node-from, value, and branch number. The new input statement for the above resistor is *R1_8_13_50_10*. It is stored in a temporary data field in the form shown in Table 5.

IFLD	IFIELD	ICODE	IDELIM	ICOLUM
1	R1	1	␣	3
2	8	0	␣	5
3	13	0	␣	8
4	50	0	␣	11
5	10	0	␣	14
6		-1		
7				

(a)

	NODPLC(*)
-1	0
LOC	0
+1	LOCV
+2	8
+3	13
+4	10
+5	
+6	
+7	

(b)

	VALUE(*)
LOCV	R1
+1	0.02
+2	50
+3	
+4	

(c)

Table 5

The branch number is stored in (LOC+4) unit in the integer parameter table NODPLC. Some new pointers and data fields have to be established and certain pointers must be revised for processing branch numbers.

*RUNCON**

Subroutine RUNCON processes Run Control Cards. The modified subroutine RUNCON* adds a SWAN analysis mark to the list of class numbers of the run control statement. The program can then turn to the corresponding SWAN control statement entrance when the SWAN analysis mark is detected.

The format of the SWAN analysis statement is as follows: .SWAN _ output branch number _ Primary inductor value _ secondary inductor value Primary coil number _ secondary coil number _ primary resistor value _ secondary resistor value compensation network R1 value _ compensation network R2 value _ compensation network R3 value _ compensation network C1 value _ compensation network C2 value _ duty ratio D _ ac loop Rsw _ transformer rate _ switching cycle Tp.

In the subroutine RUNCON*, some new common blocks, new pointers, and new data tables are set to store certain information needed by SWAN. Some error checking statements are also set.

*FIND**

FIND* revises the clear unit numbers in the integer and real tables, as well as the initial addresses of these units.

VI. CONCLUSION

A switching regulator analysis program and a versatile PWM converter model was developed. It extends the SPICE simulation domain to switches-based topology-variant circuits. A current-injected switching regulator (Figure 1) which uses a two-pole two-zero compensation network (Figure 8) was simulated. The parameter values and operating conditions are shown in Table 6.

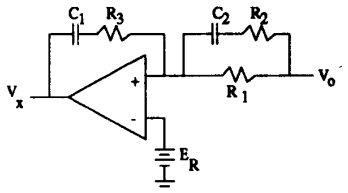

Figure 8: Two-pole two-zero compensation network

Np=22 turns	Rc1=0.07 Ω	RL=1.69 Ω
Ns=10 turns	C01=330.0 μF	D=0.35
Lp=400.0 μH	N=300	Tp=20.0 μs
Ls=82.644 μH	Rsw=53.6 Ω	R1= 10.5 $K\Omega$
Rs=0.013 Ω	Vi=23.0 V	R3=4.42 $K\Omega$
Rp=0.063 Ω	Vo=5.2 V	C1=0.1 μF
R2=210 Ω	C2=0.11 μF	

Table 6: Circuit Parameter Values and Operating Condition

The system's open-loop gain and phase curves obtained by varying the error processor ac loop transformer function, F_{ac}, using a two-pole two-zero compensation are shown in Figures 9 and 10.

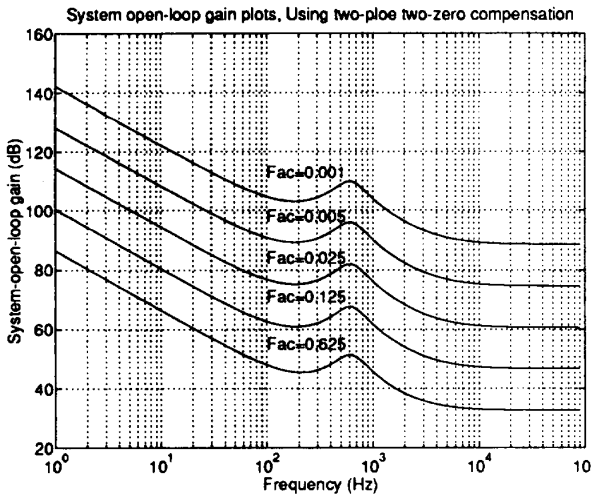

Figure 9: System open-loop gains

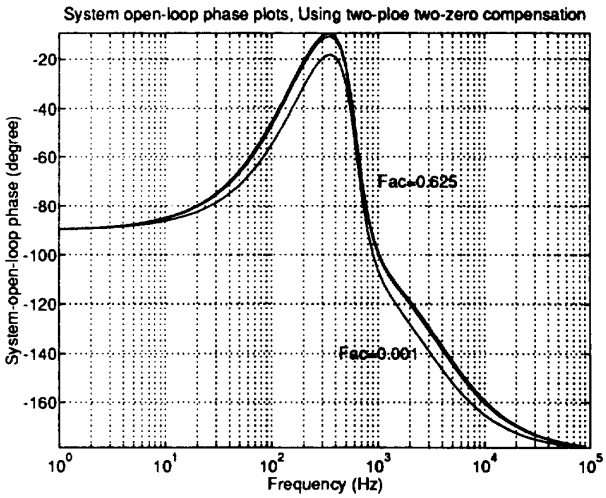

Figure 10: System open-loop phases

APPENDIX

List of input description statements for the circuit example in this paper:

A SWITCHING REGULATOR EXAMPLE

```
VI 20 0 23.0 1
Rc1 2 3 0.07 4
RL 2 0 1.69 6
X1 20 2 0 SCM
C01 3 0 330.0 5
Io 0 2 0.0 6
.SUBCKT SCM 1 2 3
Ron 1 20 1.0E-10 1
Roff 1 2 1.0E+20 3
Lps 0 1 1.0E-10 2
.ENDS SCM
.SWAN 6 4.0E-03 82.644E-06 22 10
+0.063 0.013 10500.0 210.0 4420.0
+0.1E-06 0.11E-06 0.35 53.6 300 2.0E-05
.END
```

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