Time Quantity One-Cycle Control for Power-Factor Correctors

Zheren Lai, Keyue M. Smedley, Member, IEEE, and Yunhong Ma

Abstract—Time quantity one-cycle control method is proposed in this paper for unity power-factor ac-dc converters. Converters controlled by this method operate at constant switching frequency, require no current sensing, have a simple control circuit, and exhibit resistive input impedance at the ac side. Feedback loop design method is provided to minimize the current distortion when the output voltage ripple is not negligible. Experimental results confirmed the theoretical prediction.

Index Terms— Switching converter, power factor correction, pulse width modulation.

I. INTRODUCTION

MOST RECTIFIERS are nonlinear loads to the utility line, therefore, they impose a reactive fundamental component and some higher order harmonics to the line. These components are undesirable because they: 1) produce electromagnetic interference and line voltage distortion and 2) do not contribute to load power, but increase the rms current in the transmission lines and, thus, additional losses. Ideally, the line current to the rectifier should be proportional to the line voltage so that maximum active power is delivered to the load and unity power factor is achieved.

By using dc–dc converters for active input current shaping, it is possible to achieve unity power factor. Numerous methods have been proposed in recent years [1]–[17]. Among them, the boost converter is the most frequently utilized topology due to its simplicity and high efficiency.

Automatic current shaping is obtained [1] when the boost converter operates at discontinuous conduction mode (DCM) with constant switching frequency and duty ratio. This method is very attractive because the control is very simple. The disadvantage is that the input current has distortion. The distortion is less severe when the boost converter operates at a high-voltage conversion ratio. Therefore, it is suitable for high-voltage applications.

A boost converter operating at the boundary of continuous conduction mode (CCM) and DCM [2] can theoretically eliminate the current distortion, but it requires variable switching frequency and a complex control circuit with a multiplier. It is undesirable in many applications that switching frequency varies over a wide range with load and line voltage. Some methods such as the second-order harmonic injection [3] need a very complex adaptive tune circuit and, sometimes, even have practical control difficulty.

ing, University of California, Irvine, CA 92717 USA.

It is also possible to make the input current proportional to the input voltage by including a current loop. The nonlinear carrier control for boost converters [4] is a good example. Current sensing is required for those control methods, so they are more suitable for high-power level applications and CCM operation.

This paper proposes a time quantity one-cycle control method for power-factor correction rectifiers with the follow-ing features:

- 1) purely resistive at the input port of a rectifier;
- 2) no requirement of high-voltage conversion ratio;
- 3) operating at constant switching frequency;
- 4) no need of current sensing;
- 5) no complex circuits such as the multiplier;
- 6) ease of integration.

A boost converter is used in this paper to illustrate the principle. First, the principle of the control method is introduced in Section II. Then, the effect of the output voltage ripple on the current distortion is discussed in Section III. Experimental verification is illustrated in Section IV. Finally, conclusions are given in Section V.

II. PRINCIPLE OF OPERATION

The boost converter is the most popular topology used as a power-factor corrector. The line current will have distortion when a boost converter operates at DCM, constant switching frequency, and constant duty ratio [6], [15]. This section will first review the cause of this distortion and its remedy and then present a new control method.

A. Cause and Remedy of Current Distortion

Fig. 1 shows a boost converter for active power-factor correction. When the boost converter operates at a constant switching frequency and constant duty ratio, the peak inductor current in each switching cycle is

$$i_{pk} = \frac{v_g}{L} \, dT_s \tag{1}$$

where T_s is the switching period

$$d = \frac{t_{on}}{T_s} \tag{2}$$

is the duty ratio and t_{on} is the on-time of the switch T. The time interval for the inductor current i_L to drop to zero is determined by

$$i_{pk} = \frac{v_o - v_g}{L} \, d_1 T_s. \tag{3}$$

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Fig. 1. Boost converter operating at DCM.

Therefore

$$d_1 = \frac{v_g}{v_o - v_g} d. \tag{4}$$

The average inductor current in each switching cycle (local average) \overline{i}_L is

$$\vec{i}_{L} = \frac{1}{2} (d + d_{1}) i_{pk} = \frac{1}{2L} \cdot \frac{v_{o} \cdot v_{g}}{v_{o} - v_{g}} \cdot d^{2} T_{s}.$$
(5)

When d is a constant, \overline{i}_L is proportional to $v_o \cdot v_g/(v_o - v_g)$ instead of v_g , hence, the input current to the rectifier has harmonic distortion.

As a remedy, one can eliminate the above distortion by modulating the duty ratio d in a line period such that

$$\bar{i}_L = \frac{v_g}{R_e} \tag{6}$$

where R_e is defined as the emulated input resistance of the rectifier. Substituting (6) into (5) yields

$$d(t) = \sqrt{\frac{2Lf_s}{R_e}} \frac{v_o - v_g}{v_o} \tag{7}$$

where $f_s = 1/T_s$ is the switching frequency. When the duty ratio d is controlled according to (7), the line current is proportional to the line voltage.

One can employ a multiplier/divider and a square-root operator to obtain (7) and compare with a sawtooth carrier to obtain the required duty ratio. In this paper, the one-cycle control technique [17] is adopted to modulate the pulse width, which is a time quantity, such that the duty ratio satisfies (7) in each cycle.

B. Time Quantity One-Cycle Control

The duty ratio is defined in (2). Rearranging (2) and (7) yields

$$\left(\frac{t_{on}}{T_s}\right)^2 = \frac{2Lf_s}{R_e} \frac{v_o - v_g}{v_o}.$$
(8)



Fig. 2. (a) The time quantity one-cycle control circuit and (b) its operation waveforms.

Since the output voltage v_o is unchanged at steady state, it can be assumed as a constant. The next key task is how to determine t_{on} for each switching cycle so that

$$\left(\frac{t_{on}}{T_s}\right)^2 = \frac{K(v_o - v_g)}{v_m} \tag{9}$$

where K is the gain of the voltage sensors for both v_g and v_o and

$$v_m = K v_o \frac{R_e}{2L f_s}.$$
 (10)

This task can be implemented by the circuit shown in Fig. 2.

The control circuit contains a clock generator, a flip-flop, a comparator, two integrators, and two reset switches for these two integrators. The switching frequency is determined by the constant-frequency clock. When a rising edge of a clock pulse arrives, the flip-flop is set, i.e., its positive output Q is logic "one." The active switch T in the power stage is turned on, and the two reset switches, S_1 and S_2 , are turned off. With a constant control voltage v_c , the first integrator outputs

$$v_1 = -\frac{v_c}{R_1 C_1} t, \qquad (0 \le t \le T_s)$$
 (11)

and the second integrator outputs

$$v_2 = \frac{v_c}{2R_1 C_1 R_2 C_2} t^2, \qquad (0 \le t \le T_s). \tag{12}$$

When v_2 reaches $K(v_o - v_g)$, the comparator outputs a high-voltage pulse that resets the flip-flop, i.e., Q becomes logic "zero." The active switch T is turned off, and the two reset switches are turned on. Both integration capacitors are discharged to $v_1 = v_2 = 0$, preparing for the operation in the



Fig. 3. The low-frequency and large-signal model.

next switching cycle. Comparing (9) and (12), one can see that if

$$\frac{v_c}{2R_1C_1R_2C_2} = \frac{v_m}{T_s^2} \tag{13}$$

(7) is satisfied for each cycle. A similar circuit was found for feedforward control of an *A*-quadratic converter [18].

Notice in (6) that v_g can be an arbitrary waveform, and \overline{i}_L is proportional to v_g . Thus, the input impedance of the rectifier is purely resistive, with an equivalent resistance R_e . Substituting (10) into (13) gives

$$R_e = K_e \frac{v_c}{v_o} \tag{14}$$

where

$$K_e = \frac{T_s^2}{R_1 C_1 R_2 C_2} \frac{\omega_s L}{2\pi} \frac{1}{K}$$
(15)

and $\omega_s = 2\pi f_s$. Thus, R_e is directly proportional to the control voltage v_c .

The input power to the rectifier can be controlled by varying the control voltage v_c so that the output dc voltage V_o is regulated. When the conversion efficiency η is taken into account, a low-frequency and large-signal model shown in Fig. 3 is obtained with a voltage feedback loop included [19], where $A_v(s)$ is the compensator. The notation in Fig. 3 is slightly different from that presented in [19]. The controlled output is a current source instead of a power source. The output voltage is determined by

$$V_o = v_{g,\,\rm rms} \sqrt{\frac{R}{R_e}} \,\eta \tag{16}$$

where R is the load resistance and $v_{g, rms}$ is the rms value of v_{q} .

III. EFFECT OF THE OUTPUT VOLTAGE RIPPLE

In the above description, the output voltage was considered as a constant, which is adequate under small-ripple assumption. With this assumption, the output filtering capacitance has to be very large. Therefore, the capacitor is bulky in size and expensive in price. Furthermore, large capacitance results in large inrush current at the start-up of the converter.

With smaller filtering capacitance, the output voltage is not a constant anymore. Instead, it is a dc voltage with some ripples, mainly a 120-Hz component

$$v_o(t) = V_o + \hat{v}_o(t) \tag{17}$$



Fig. 4. The control circuit to achieve variable gain.

where \hat{v}_o is the ripple voltage and V_o is the dc portion. These ripples will cause input current distortion.

According to (14), if v_c is proportional to v_o , the emulated resistance R_e will remain constant during one line period. Therefore, the input current has no distortion. The proportional coefficient K_e is dependent on R_e , which requires the gain from v_o to v_c to be variable in the feedback path. One can implement that with a multiplier, as shown in Fig. 4. The gain is controlled by the output of the control block $A_v(s)$, which is a slow-varying signal.

The following analysis shows that the effect of the output voltage ripple on the line current distortion can be minimized by proper feedback design without using a multiplier.

The following assumptions are made for the analysis.

- 1) The output voltage ripple is reasonably small; say its amplitude is 10% of the dc voltage V_o , i.e., its peak-to-peak value is 20% V_o .
- 2) The line voltage has no distortion, i.e., $v_g = V_g \sin(\omega_\ell t)$, where ω_ℓ is the line radian frequency.
- 3) At the output, all the dc current passes through the load resistor R, and all the ac current passes through the filtering capacitor C.

Under these assumptions, the current i shown in Fig. 3 can be approximated as

$$i = \frac{V_o}{R} \left(1 - \cos 2\omega_\ell t\right). \tag{18}$$

Thus, the ripple voltage is

$$\hat{v}_o(t) = -\frac{V_o}{2\omega_\ell RC} \sin\left(2\omega_\ell t\right) \tag{19a}$$

or

$$\hat{v}_o(t) = -\frac{P_o}{2\omega_\ell C V_o} \sin\left(2\omega_\ell t\right) \tag{19b}$$

where P_o is the output power. One can use (19) to estimate the filtering capacitance required for the maximum ripple amplitude.

A proportional-integral (PI) controller is used as an example for the control block $A_v(s)$ shown in Fig. 3:

$$A_v(s) = -\left(K_p + \frac{1}{\tau_I s}\right) \tag{20}$$

where K_p is the proportion constant and τ_I is the time constant of the integration.

At steady state, the dc portion of the output voltage should equal the control reference, i.e., $V_o = V_{ref}$. Thus, the output of the error amplifier is the ripple voltage, i.e.,

$$V_{ref} - v_o = -\hat{v}_o$$
$$= e(t) \tag{21}$$

where e(t) is the error voltage shown in Fig. 3.

At steady state, the output of the PI controller v_c satisfies

$$v_c = V_c + \hat{v}_c \tag{22}$$

where V_c stands for the dc portion and \hat{v}_c is the ac part. Due to using the PI controller, V_c will be obtained to keep V_o equal to the control reference by the integral part of the controller, i.e., $V_c = (R_{e,av}/K_e)V_o$. Here, $R_{e,av}$ is the average R_e in one line period since R_e is not constant anymore. If the zero of the PI controller is put well below the double-line frequency $2\omega_\ell$, \hat{v}_c satisfies

$$\hat{v}_c = K_p \hat{v}_o. \tag{23}$$

Thus

$$v_c = \frac{R_{e,av}}{K_e} V_o + K_p \hat{v}_o. \tag{24}$$

Selecting K_p to be

$$K_p = \frac{R_{e,av}}{K_e} \tag{25}$$

yields

$$v_c = K_p(V_o + \hat{v}_o)$$

= $K_p v_o.$ (26)

Thus, the line current will not have distortion due to the output voltage ripple.

However, $R_{e,av}$ varies with the output power while K_p keeps constant after the controller $A_v(s)$ is determined. Therefore, (26) is satisfied only for one particular load power level.

Reorganizing (24) gives

$$v_{c} = \frac{R_{e,av}}{K_{e}} \left(V_{o} + \hat{v}_{o} \right) + \left(K_{p} - \frac{R_{e,av}}{K_{e}} \right) \hat{v}_{o}$$
$$= \frac{R_{e,av}}{K_{e}} v_{o} \left[1 + \left(\frac{K_{e}K_{p}}{R_{e,av}} - 1 \right) \frac{\hat{v}_{o}}{v_{o}} \right]. \tag{27}$$

Combining (5), (14), and (27) yields

$$\overline{i}_L = \frac{v_g}{R_e} = \frac{v_g}{R_{e,av} \left[1 + \left(\frac{K_e K_p}{R_{e,av}} - 1\right) \frac{\hat{v}_o}{v_o} \right]}.$$
 (28)

Further assuming $|K_e K_p/R_{e,av}-1| \le 2$, one can approximate (28) as

$$\overline{i}_L \approx \frac{v_g}{R_{e,av}} \left[1 + \left(1 - \frac{K_e K_p}{R_{e,av}} \right) \frac{\hat{v}_o}{V_o} \right].$$
(29)

Substituting (16) and (19) into (29), with the assumption that the conversion efficiency $\eta = 1$, yields

$$\bar{i}_L \approx \frac{v_g}{R_{e,av}} \left[1 - \left(1 - \frac{K_e K_p}{R_{e,av}} \right) \cdot \frac{\sin\left(2\omega_\ell t\right)}{2\omega_\ell R_{e,av} C} \left(\frac{v_{g,\text{rms}}}{V_o} \right)^2 \right].$$
(30)



Fig. 5. THD's versus the emulated input resistance $R_{e, av}$ for different K_x .

At full load, $R_{e, av}$ is at its minimum value $R_{e, \min}$. Let

$$K_p = K_x \frac{R_{e,\min}}{K_e} \tag{31}$$

where K_x is an adjustable constant and utilize earlier assumptions (30) become

$$\overline{i}_{L} \approx \frac{V_{g} \sin(\omega_{\ell} t)}{R_{e,av}} \cdot \left[1 - \left(1 - \frac{K_{x}R_{e,\min}}{R_{e,av}} \right) \frac{\sin(2\omega_{\ell} t)}{2\omega_{\ell}R_{e,av}C} \left(\frac{v_{g,\mathrm{rms}}}{V_{o}} \right)^{2} \right].$$
(32)

The second item in the bracket of (32) is the cause of the current distortion.

As an example, the following parameters are assigned to (32): $V_{g, \text{rms}} = 115$ V, $V_o = 230$ V, $R_{e, \text{min}} = 60 \Omega$ for approximately 200 W of maximum output power, C = $100\,\mu\text{F}$ for about 20 V of peak-to-peak ripple, and 60 Hz for the line frequency. K_x is selected to range from 0.6 to 3 so that the assumptions for (29) are satisfied. The total harmonic distortion (THD) for different $R_{e,av}$ is calculated and shown in Fig. 5. The curves are the THD's for $K_x =$ 0.6, 0.8, 1.0, 1.2, 1.4, 1.6, 2, and 3, respectively. The horizontal axis is the normalized emulated resistance $R_{e, av}/R_{e, \min}$. Under earlier assumptions, the main harmonic is the third harmonic. Notice that when $K_x = 1.2$, the overall distortion in the entire load range is the smallest. Larger K_x will result in larger K_p , hence, larger bandwidth. When the line voltage varies, the curves shown in Fig. 5 will also change. The variation is a scale factor of $(v_{g, rms}/nominal v_{g, rms})^2$, as one can see from (32). Smaller $V_{g, rms}$ will result in small distortion and vice versa. Nevertheless, the theoretical, overall THD is smaller than 3%, at nominal line voltage, when K_x is less than 2. The current distortion is negligibly small when the feedback loop is properly designed.

IV. EXPERIMENTAL VERIFICATION

A 200-W experimental circuit was built to verify this control method. The circuit is shown in Fig. 6. The input to the rectifier is the 115-Vrms utility line, and the output dc voltage is 230



Fig. 6. The experimental circuit (L_f and C_f are filter components).



Fig. 7. Operation waveforms in each switching cycle. From top to bottom, the waveforms are v_T , v_1 , v_2 , and i_L , respectively.

V. The output is at full load when $R = 250 \Omega$. The switching frequency is 100 kHz. The gain for both voltage sensors is 1/50, determined by the resistor dividers. The feedback control block $A_v(s)$ is a PI controller, with $K_p = 0.3$ (corresponding to $K_x = 1.0$ so that the THD is minimized at full load) and $\tau_1 = 11s$. Thus, the zero of the PI controller is around 0.1 Hz to satisfy the condition for (23).

A. Experiment with Negligible Output Voltage Ripple

In order to verify the validity of the control method, the filtering capacitor was selected to be 1000 μ F in this experiment, so that the effect of the output voltage ripple can be neglected. Figs. 7 and 8 illustrate the experimental waveforms at full load. From top to bottom in Fig. 7, the waveforms are the switch voltages v_T , v_1 , v_2 , and i_L , respectively, as indicated in Fig. 6. In Fig. 8, the top waveform reflects the duty ratio, measured with a time-tovoltage converter Tektronix TVC501; the second one is the output of a differential amplifier representing $K(v_o - v_g)$; the third and forth ones are the line voltage and the input current to the rectifier, respectively. Notice that the current waveform is closely proportional to the line voltage, indicating



Fig. 8. Waveforms in a line period.



Fig. 9. Spectra of the normalized line voltage and current, measured at 115-Vrms line voltage, 230-Vdc output, and 250- Ω load: (a) the spectrum of the line voltage and (b) the spectrum of the line current.

that the input port of the rectifier is purely resistive. Fig. 9 shows the normalized spectra for the line voltage and current, respectively. Notice that they are very close. The THD for the voltage was measured to be 3.357%, and the THD for the current was 4.031%.

B. Experiment with Large Output Voltage Ripple

In order to observe the effect of the output voltage ripple on line current distortion, the filtering capacitance was reduced to 100 μ F. Fig. 10 shows the experimental waveforms at full



Ch1: 10V/div Ch2: 115Vms Ch3: 2A/div Horizontal scale: 6ms/div

Fig. 10. Waveforms of the output voltage ripple, line voltage, and line current at full load.



Fig. 11. Spectrum of the line current for Fig. 10.

load. From top to bottom, the waveforms are the output voltage ripple, line voltage, and current, respectively. The peak-topeak voltage of the ripple is about 10% of its dc portion. No obvious distortion can be seen from the waveforms. The spectrum of the current is shown in Fig. 11. The current THD was measured to be 3.974%, while the voltage THD was the same as the last experiment.

Fig. 12 shows the experimental results at 30% of the full load. From top to bottom, the waveforms are the corespondents to those in Fig. 10. Notice that the current wave has some small ringing. This is caused by the low-pass filter in the power stage. When the load resistance increases, the equivalent load impedance of the low-pass filter increases, resulting in higher quality factor, hence, more oscillation. Fig. 13 is the normalized spectrum of the line current. The THD was measured to be 5.092%.

C. Dynamic Response

Experiments about the dynamics were also carried out. The dynamic response due to a step load change was tested, and the transient is shown in Fig. 14. The upper curve is the output voltage, and the lower one is the line current. The output filtering capacitor was 100 μ F for this test. The load resistance changed from 500 to 250 Ω , i.e., from 50% to full load. This response speed is about 1/4 of that reported in [5]. One can increase the response speed by increasing K_p , with the trade-



Ch1: 10V/div Ch2: 115Vrms Ch3: 2A/div Horizontal scale: 5ms/div

Fig. 12. Waveforms of the output voltage ripple, line voltage, and line current at 30% of the full load.



Fig. 13. Spectrum of the line current for Fig. 12.



Fig. 14. Experimental transient response of the PFC.

off of larger harmonic distortion. Another way to increase the response speed is to adopt methods such as the one proposed in [20].

V. CONCLUSION

Power-factor correction and line-harmonic reduction have become an important issue in power electronics research. The time quality one-cycle control method proposed in this paper provides a simple, but effective solution for small-medium power applications. Owing to the one-cycle control concept, nonlinear components were not required for the control circuit, compared to the implementation presented in [6], which needs a square-root operator and a multiplier.

The proposed method controls the time duration of the switching pulse such that the average value of the input current follows the input voltage in each cycle. As a result, unity power factor and low distortion are achieved. Furthermore, feedback loop design method is presented to minimize the THD under a large output ripple condition. Therefore, the size of the filter capacitor can be reduced. The control bandwidth can be further increased with some sacrifice of current distortion.

A boost converter was used as an example for the implementation. As shown in the experimental results, this unity power-factor ac–dc converter operates at a constant switching frequency, requires no current sensing, has a simple control circuit, and exhibits *resistive* input impedance at the ac side.

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Zheren Lai received the B.S. and M.S. degrees in electrical engineering from Zhejiang University, Hangzhou, China, in 1989 and 1993, respectively. He is currently working toward the Ph.D. degree at the University of California (UCI), Irvine.

From 1989 to 1992, he worked on active power filters. He was employed as a Research Engineer at the Electrical and Electronic Engineering Company, Hangzhou, China, for a short period in 1993. Since he joined UCI in the fall of 1993, his research has been concentrated in the control of switching audio

power amplifiers. His research interests also include high-frequency power conversion and power-factor correction.



Keyue M. Smedley (S'87–M'90) received the B.S. and M.S. degrees in electrical engineering from Zhejiang University, Hangzhou, China, in 1982 and 1985, respectively, and the Ph.D. degree in electrical engineering from the California Institute of Technology, Pasadena, in 1991.

From 1990 to 1992, she was an Engineer at the Superconducting Super Collider, where she was responsible for determining the electrical characteristics of the superconducting magnet strings and designing the power conversion systems for the

Superconducting Collider. She joined the faculty of Electrical and Computer Engineering at the University of California, Irvine, in 1992, where she has established a state-of-the-art power electronics laboratory. Her research interests include nonlinear modeling and control of switching converters, class-D power amplifiers, soft-switching techniques for converters and inverters, power-factor correction methods, etc. She currently holds the U.S. patent for one-cycle control.

Dr. Smedley is the Chair of the Constitution and Bylaws Committee of the IEEE Power Electronics Society, a Faculty Member of Eta Kappa Nu, and the IEEE UCI Student Chapter Advisor.

Yunhong Ma received the B.S. and M.S. degrees in electrical engineering from Zhejiang University, Hangzhou, China, and the M.S. degree in computer engineering from Wayne State University, Detroit, MI, in 1982, 1987, and 1996, respectively.

From 1983 to 1992, she was a Lecturer (equivalent to an Assistant Professor) at Zhejiang University, where her research interests were power electronics, microprocessor applications, and embedded control systems. From 1994 to 1995, she was a Visiting Scholar at the University of California, Irvine, where her research interest was mainly in modeling methods for switching converters and power-factor correction. Since completing computer engineering studies, she has been interested in Software and Firmware design for real-time embedded systems.