

IR2108/IR21084

HIGH AND LOW SIDE DRIVER

Features

- Floating channel designed for bootstrap operation
Fully operational to +600V
Tolerant to negative transient voltage
dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for both channels
- 5V Schmitt triggered input logic
- Cross-conduction prevention logic
- Matched propagation delay for both channels
- High side output in phase with HIN input
- Low side output out of phase with LIN input
- Logic and power ground +/- 5V offset.
- Internal 500ns dead-time, and programmable up to 5us with one external R_{DT} resistor (IR21084)
- Lower di/dt gate driver for better noise immunity

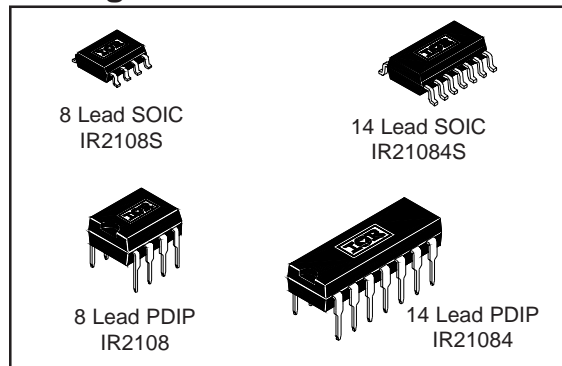
Description

The IR2108/IR21084 are high voltage, high speed power MOSFET and IGBT drivers with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 volts.

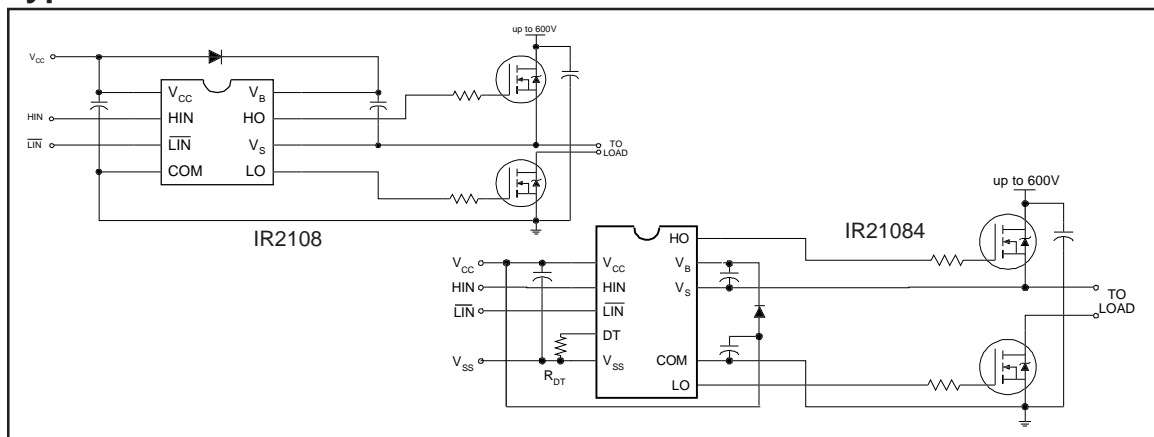
Product Summary

V _{OFFSET}	600V max.
I _{O+/-}	120 mA / 250 mA
V _{OUT}	10 - 20V
t _{on/off} (typ.)	180 ns
Deadtime (typ.) (programmable up to 5uS for IR21084)	500 ns

Packages



Typical Connection



IR2108/IR21084

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units	
V _B	High side floating absolute voltage	-0.3	625	V	
V _S	High side floating supply offset voltage	V _B - 25	V _B + 0.3		
V _{HO}	High side floating output voltage	V _S - 0.3	V _B + 0.3		
V _{CC}	Low side and logic fixed supply voltage	-0.3	25		
V _{LO}	Low side output voltage	-0.3	V _{CC} + 0.3		
DT	Programmable dead-time (IR21084 only)	V _{SS} - 0.3	V _{CC} + 0.3		
V _{IN}	Logic input voltage (HIN & LIN)	V _{SS} - 0.3	V _{CC} + 0.3		
V _{SS}	Logic ground (IR21084 only)	V _{CC} - 25	V _{CC} + 0.3		
dV _S /dt	Allowable offset supply voltage transient	—	50	V/ns	
P _D	Package power dissipation @ T _A ≤ +25°C	(8 lead PDIP)	—	1.0	W
		(8 lead SOIC)	—	0.625	
		(14 lead PDIP)	—	1.6	
		(14 lead SOIC)	—	1.0	
R _{thJA}	Thermal resistance, junction to ambient	(8 lead PDIP)	—	125	°C/W
		(8 lead SOIC)	—	200	
		(14 lead PDIP)	—	75	
		(14 lead SOIC)	—	120	
T _J	Junction temperature	—	150	°C	
T _S	Storage temperature	-50	150		
T _L	Lead temperature (soldering, 10 seconds)	—	300		

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The V_S and V_{SS} offset rating are tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
V _B	High side floating supply absolute voltage	V _S + 10	V _S + 20	V
V _S	High side floating supply offset voltage	Note 1	600	
V _{HO}	High side floating output voltage	V _S	V _B	
V _{CC}	Low side and logic fixed supply voltage	10	20	
V _{LO}	Low side output voltage	0	V _{CC}	
V _{IN}	Logic input voltage (HIN & LIN)	V _{SS}	V _{CC}	
DT	Programmable dead-time (IR21084 only)	V _{SS}	V _{CC}	
V _{SS}	Logic ground (IR21084 only)	-5	5	
T _A	Ambient temperature	-40	125	°C

Note 1: Logic operational for V_S of -5 to +600V. Logic state held for V_S of -5V to -V_{BS}.

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC} , V_{BS}) = 15V, V_{SS} = COM, C_L = 1000 pF, T_A = 25°C, DT = V_{SS} unless otherwise specified.

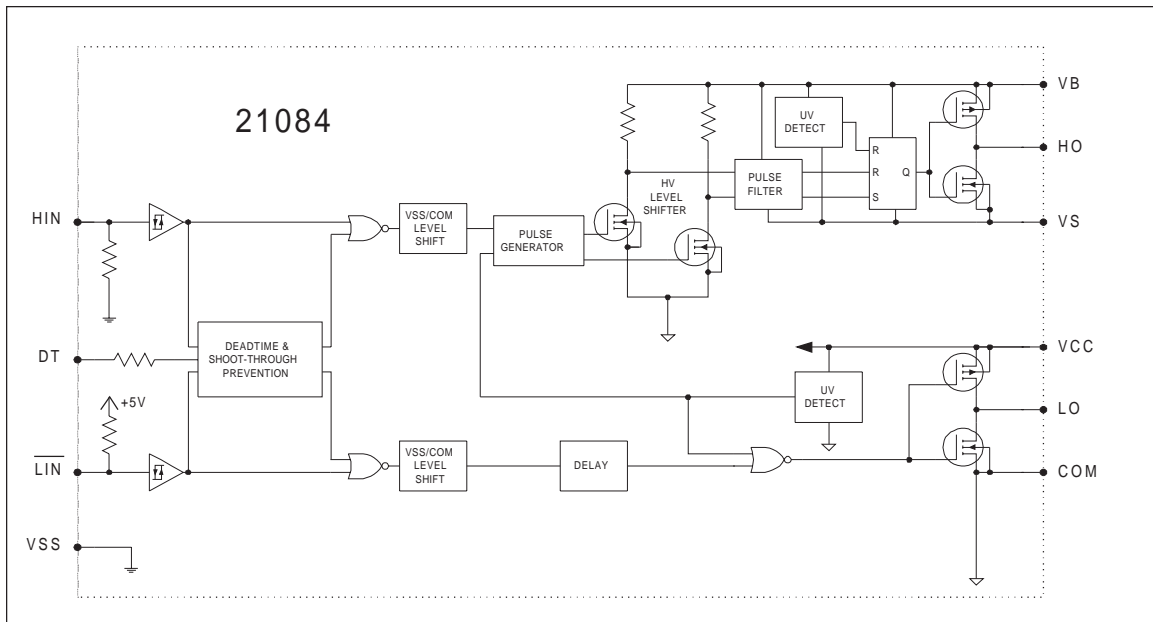
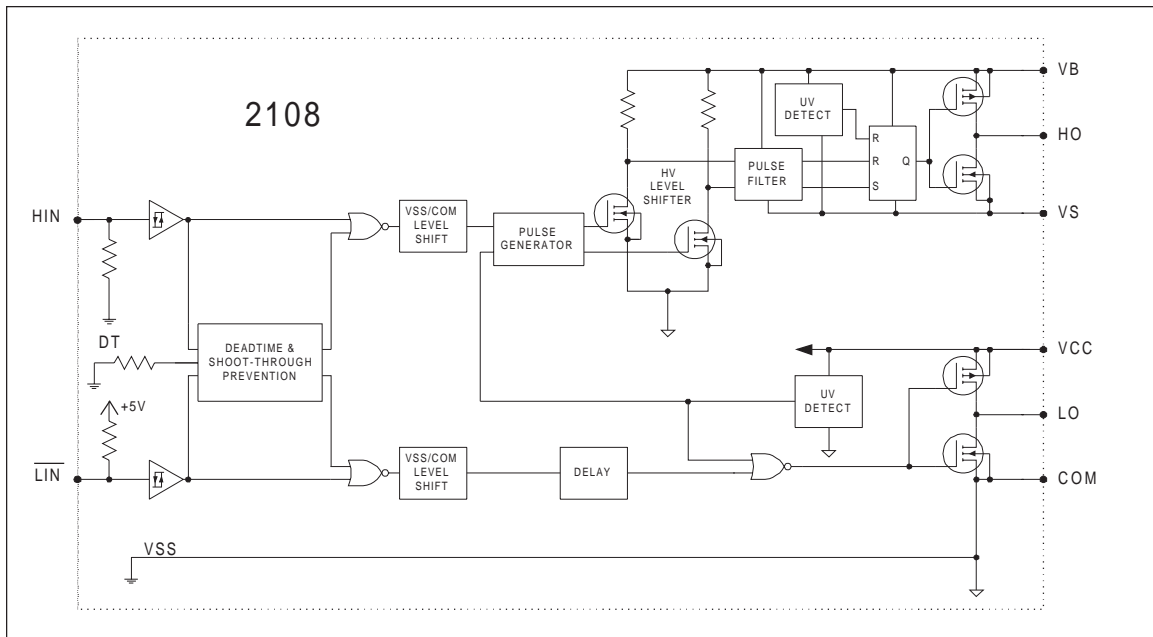
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	—	180	270	nS	$V_S = 0V$
t_{off}	Turn-off propagation delay	—	170	250		$V_S = 0V$ or 600V
MT	Delay matching, HS & LS turn-on/off	—	0	50		
t_r	Turn-on rise time	—	150	220		$V_S = 0V$
t_f	Turn-off fall time	—	50	80		$V_S = 0V$
DT	Deadtime: LO turn-off to HO turn-on(DT _{LO-HO}) HO turn-off to LO turn-on (DT _{HO-LO})	380	500	620	uS	RDT= 0
		4	5	6		RDT = 200k (IR21084)
MDT	Deadtime matching = DT _{LO-HO} - DT _{HO-LO}	—	0	60	nS	RDT=0
		—	0	600		RDT = 200k (IR21084)

Static Electrical Characteristics

V_{BIAS} (V_{CC} , V_{BS}) = 15V, V_{SS} = COM, DT= V_{SS} and T_A = 25°C unless otherwise specified. The V_{IL} , V_{IH} and I_{IN} parameters are referenced to V_{SS}/COM and are applicable to the respective input leads: \overline{HIN} and \overline{LIN} . The V_O , I_O and R_{on} parameters are referenced to COM and are applicable to the respective output leads: HO and LO.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "1" input voltage for \overline{HIN} & logic "0" for \overline{LIN}	2.7	—	—	V	$V_{CC} = 10V$ to 20V
V_{IL}	Logic "0" input voltage for \overline{HIN} & logic "1" for \overline{LIN}	—	—	0.8		$V_{CC} = 10V$ to 20V
V_{OH}	High level output voltage, $V_{BIAS} - V_O$	—	0.8	1.4		$I_O = 20$ mA
V_{OL}	Low level output voltage, V_O	—	0.3	0.6		$I_O = 20$ mA
I_{LK}	Offset supply leakage current	—	—	50	μA	$V_B = V_S = 600V$
I_{QBS}	Quiescent V_{BS} supply current	20	60	150	μA	$V_{IN} = 0V$ or 5V
I_{QCC}	Quiescent V_{CC} supply current	0.4	1.0	1.6	mA	$V_{IN} = 0V$ or 5V
I_{IN+}	Logic "1" input bias current	—	5	20	μA	$\overline{HIN} = 5V$, $\overline{LIN} = 0V$
I_{IN-}	Logic "0" input bias current	—	1	2		$\overline{HIN} = 0V$, $\overline{LIN} = 5V$
V_{CCUV+} V_{BSUV+}	V_{CC} and V_{BS} supply undervoltage positive going threshold	8.0	8.9	9.8	V	
V_{CCUV-} V_{BSUV-}	V_{CC} and V_{BS} supply undervoltage negative going threshold	7.4	8.2	9.0		
V_{CCUVH} V_{BSUVH}	Hysteresis	0.3	0.7	—		
I_{O+}	Output high short circuit pulsed current	120	200	—	mA	$V_O = 0V$, $PW \leq 10 \mu s$
I_{O-}	Output low short circuit pulsed current	250	350	—		$V_O = 15V$, $PW \leq 10 \mu s$

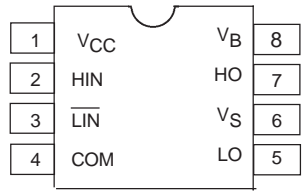
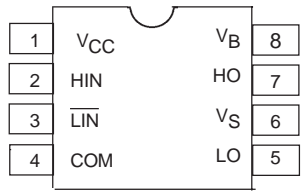
Functional Block Diagram

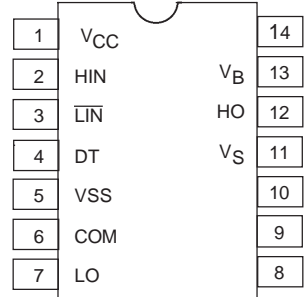
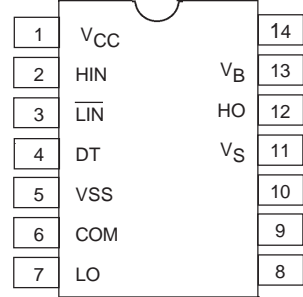


Lead Definitions

Symbol	Description
HIN	Logic input for high side gate driver output (HO), in phase (referenced to COM for IR2108 and VSS for IR21084)
$\overline{\text{LIN}}$	Logic input for low side gate driver output (LO), out of phase (referenced to COM for IR2108 and VSS for IR21084)
DT	Programmable dead-time lead, referenced to VSS. (IR21084 only)
VSS	Logic Ground (21084 only)
V _B	High side floating supply
HO	High side gate driver output
V _S	High side floating supply return
V _{CC}	Low side and logic fixed supply
LO	Low side gate driver output
COM	Low side return

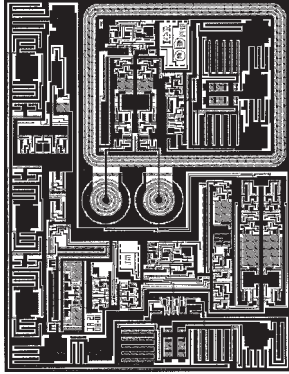
Lead Assignments

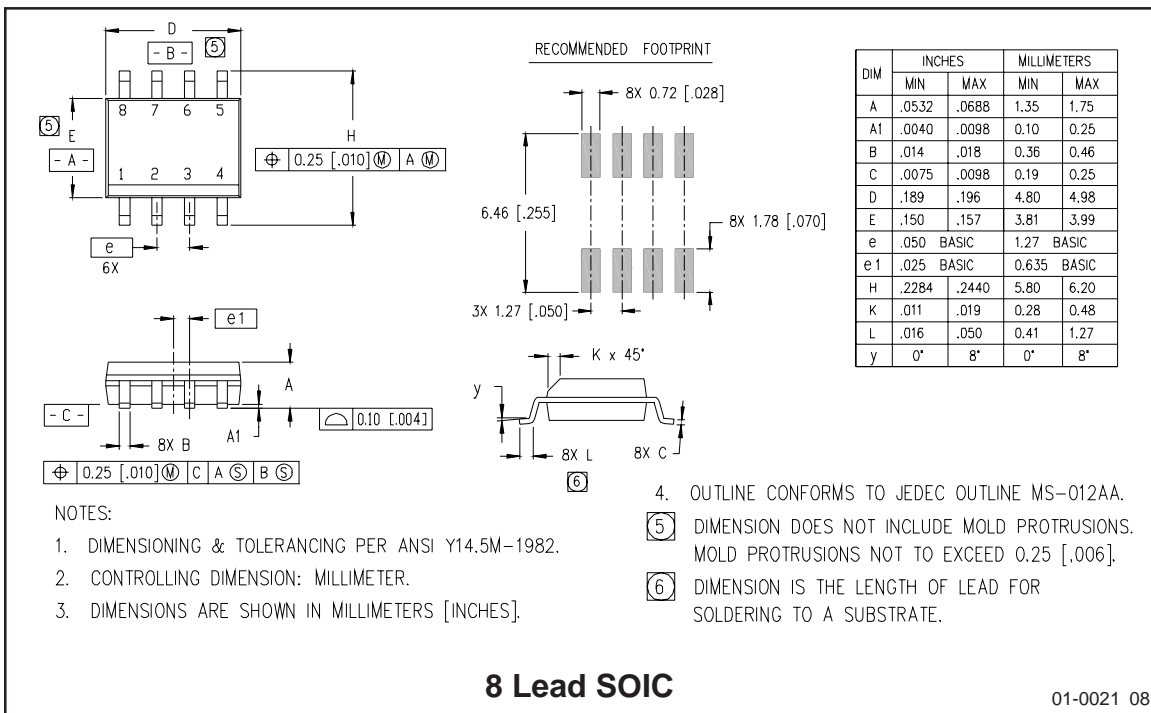
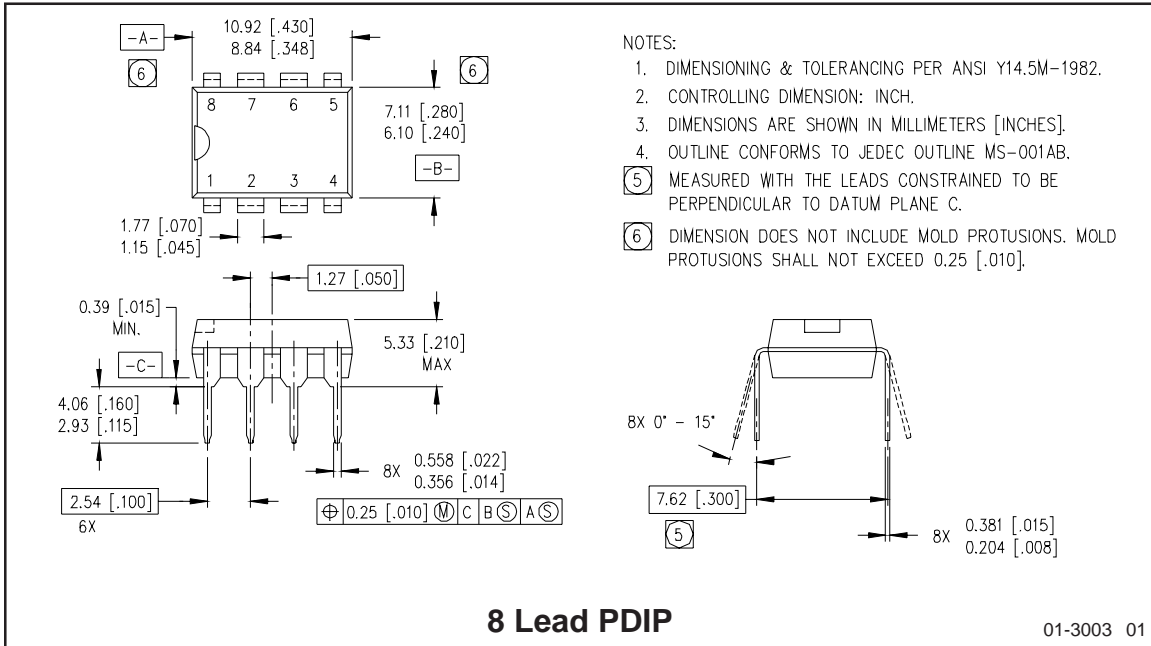
 <p>8 Lead PDIP</p>	 <p>8 Lead SOIC</p>
IR2108	IR2108S

 <p>14 Lead PDIP</p>	 <p>14 Lead SOIC</p>
IR21084	IR21084S

IR2108/IR21084

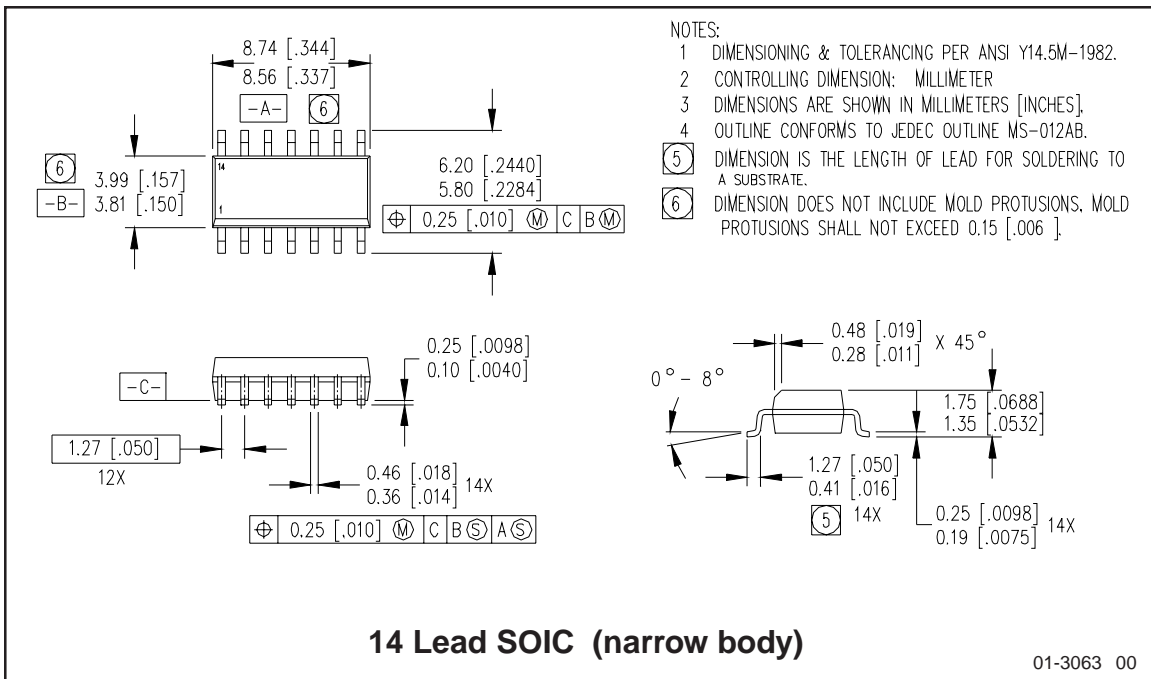
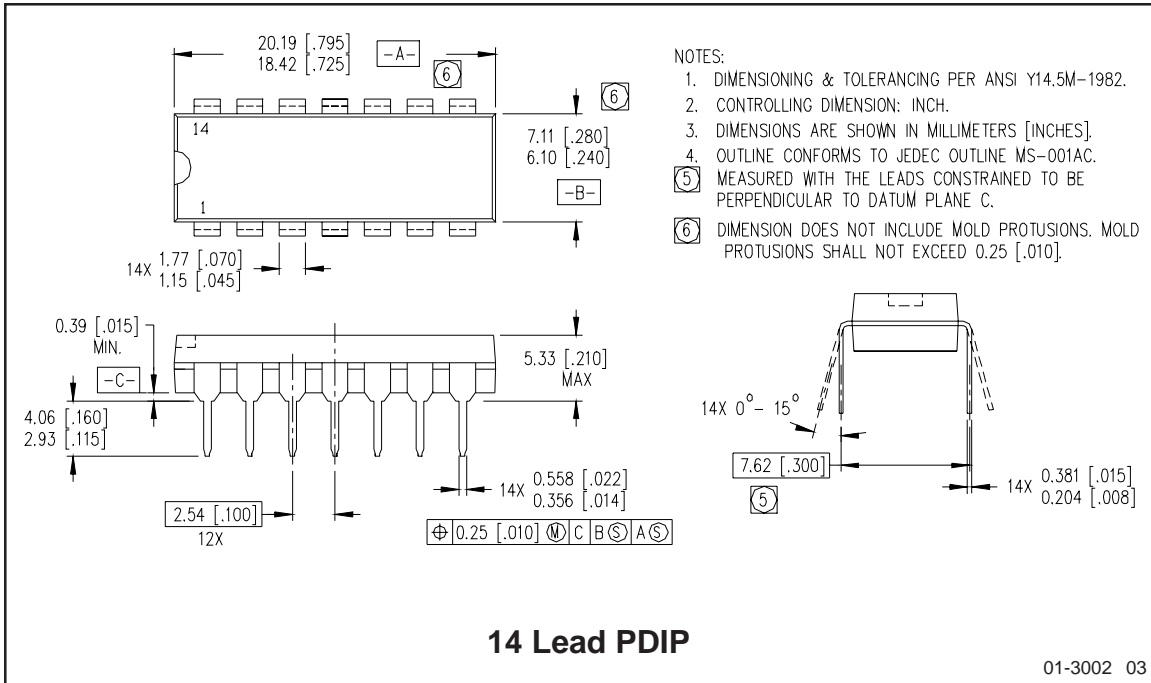
Device Information

Process & Design Rule		HVDCMOS 3.0 μm
Transistor Count		168
Die Size		66 X 88 X 26 (mil)
Die Outline		
Thickness of Gate Oxide		800 \AA
Connections	Material	Poly Silicon
	First Layer	Width Spacing Thickness
Second Layer	Material	Al - Si (Si: 1.0% \pm 0.1%)
	Width Spacing Thickness	3 μm 5 μm 10,000 \AA
	Contact Hole Dimension	3 μm X 3 μm
Insulation Layer	Material	PSG (SiO_2)
	Thickness	1.0 μm
Passivation	Material	PSG (SiO_2)
	Thickness	1.5 μm
Method of Saw		Full Cut
Method of Die Bond		Ablebond 84 - 1
Wire Bond	Method	Thermo Sonic
	Material	Au (1.0 mil / 1.3 mil)
Leadframe	Material	Cu
	Die Area	Ag
	Lead Plating	Pb : Sn (37 : 63)
Package	Types	8 & 14 Lead PDIP / 8 & 14 Lead SOIC
	Materials	EME6300 / MP150 / MP190
Remarks:		



IR2108/IR21084

International
IR Rectifier



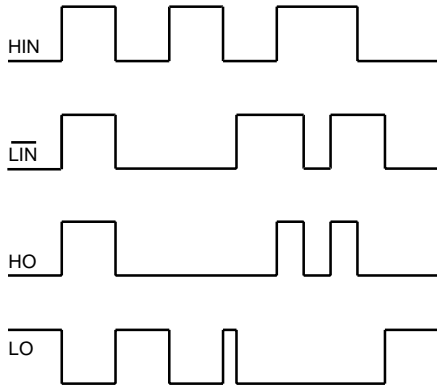


Figure 1. Input/Output Timing Diagram

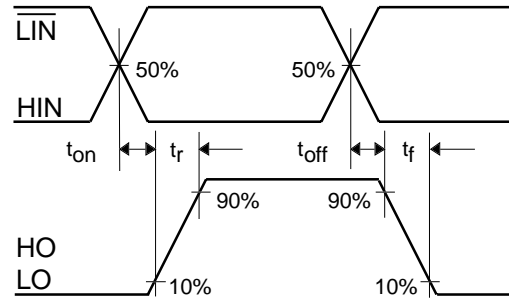


Figure 2. Switching Time Waveform Definitions

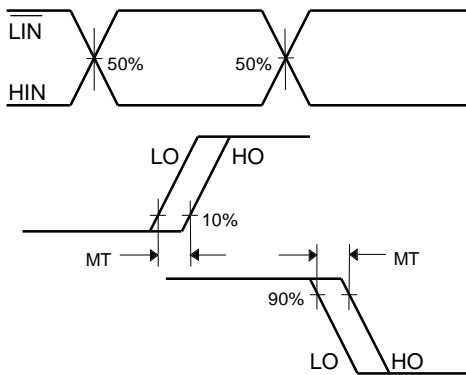


Figure 3. Delay Matching Waveform Definitions

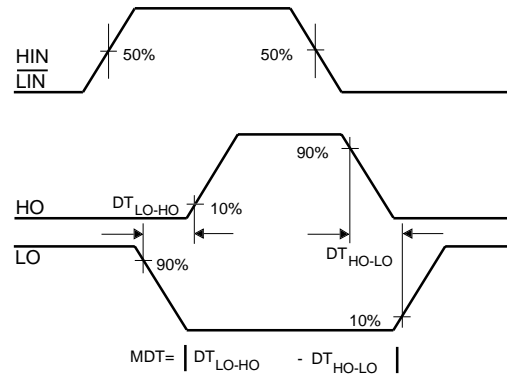


Figure 4. Deadtime Waveform Definitions