Using PWM Output as a Digital-to-Analog Converter on a TMS320C240 DSP

APPLICATION REPORT: SPRA490

David M. Alter
Technical Staff - DSP Applications
November 1998

TEXAS INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain application using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

TRADEMARKS

TI is a trademark of Texas Instruments Incorporated.

Other brands and names are the property of their respective owners.

Contents

Figures

Tables

Using PWM Output as a Digital-to-Analog Converter on a TMS320C240 DSP

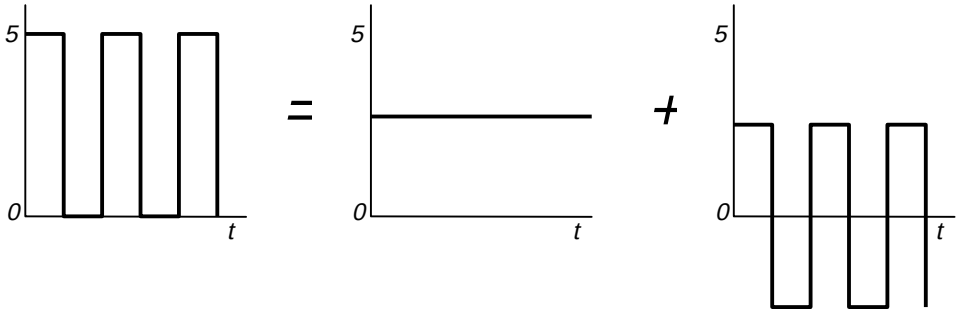
Abstract

This paper presents a method for utilizing the on-chip PWM generators on a TMS320C240 DSP for digital-to-analog (D/A) conversion. The method involves analog low-pass filtering the PWM signal to remove high frequency components, leaving only the low-frequency content. Theoretical and experimental results are presented to quantify the achievable bit resolution. In addition, analog low-pass filter design is discussed and an example 3rd order filter design is given. The achievable D/A bandwidth is on the order of 500 to 1000 Hz. Such bandwidth is useful for real-time system debug purposes, and also suitable in less demanding applications such as low performance servo control or man-machine interfacing.

Introduction

The pulse width modulated (PWM) signal outputs on a TMS320C240 DSP are variable duty cycle square-waves with 5 volt amplitude. These signals can each be decomposed into a D.C. component plus a new square-wave of identical duty-cycle but with a time-average amplitude of zero. Figure 1 depicts this graphically. It will be shown that the amplitude of the D.C. component is directly proportional to the PWM duty cycle.

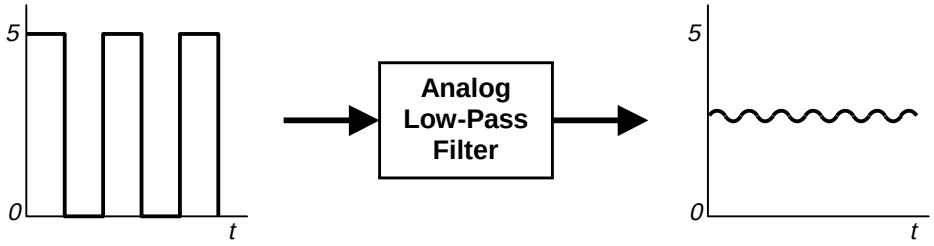
Figure 1. Decomposition of PWM Signal (shown for 50% duty cycle)



Original PWM signal D.C. Component Zero average square wave

The idea behind realizing D/A output from the PWM signal is to analog low-pass filter the PWM output to remove most of the high frequency components, thereby leaving only the low frequency (D.C.) components. This is depicted in Figure 2. The bandwidth of the low-pass filter will essentially determine the bandwidth of the D/A. A frequency analysis of the PWM signal is given in the next section in order to provide a theoretical basis for the filtering strategy.

Figure 2. Analog Filtering of PWM Signal

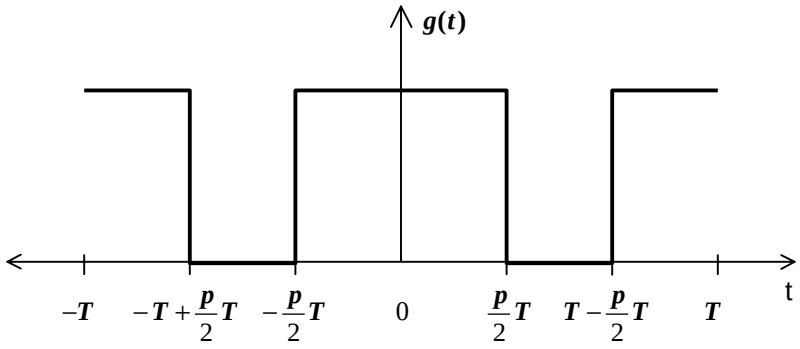


Original PWM Signal Desired Analog Output

Frequency Analysis of the PWM Signal

Fourier theory states that any periodic waveform can be decomposed into an infinite sum of harmonics at frequencies which are integer multiples of the base periodic frequency. Without loss of generality, the Fourier series representation of the PWM signal can be simplified by judiciously placing the time origin so that the signal becomes an even mathematical function, as shown in Figure 3.

Figure 3. PWM Signal Time-Shifted for Even Symmetry



In Figure 3, p denotes the PWM duty cycle ($0 \le p \le 1$), and T denotes the carrier period in seconds. Recall that a TMS320C240 DSP is capable of generating both asymmetric and symmetric PWM. This should not be confused with even symmetry, which is a mathematical property of a function. The signal depicted in Figure 3 applies equally well to either type of PWM.

The Fourier series representation of an even periodic function f(t) may be computed as follows [1]:

$$f(t) = A_0 + \sum_{n=1}^{\infty}\left[A_n \cos\left(\frac{2n\pi t}{T}\right) + B_n \sin\left(\frac{2n\pi t}{T}\right)\right] \quad (1)$$

where

$$A_0 = \frac{1}{2T}\int_{-T}^{T} f(t)dt \quad (2)$$

$$A_n = \frac{1}{T}\int_{-T}^{T} f(t)\cos\left(\frac{2n\pi t}{T}\right)dt \quad (3)$$

$$B_n = \frac{1}{T}\int_{-T}^{T} f(t)\sin\left(\frac{2n\pi t}{T}\right)dt \quad (4)$$

With a 5 volt amplitude for g(t) in Figure 3, one obtains the following results after performing the integrals (2) - (4):

$$A_0 = 5\cdot p \qquad A_n = 5\cdot\frac{1}{n\pi}\left[\sin(n\pi p) - \sin(2n\pi(1-p/2))\right] \qquad B_n = 0 \quad (5)$$

The zero result for B_n is expected for an even function, and will not be discussed further here. The D.C. component A_0 is seen equal to the PWM amplitude multiplied by the PWM duty cycle. This is the desired D/A output. By selecting the proper duty cycle, any D/A output voltage can be obtained within the range 0 to 5 volts. The A_n terms represent the amplitudes of the high frequency harmonic components of the PWM signal, which are seen to exist at integer multiples of the PWM carrier frequency $2\pi/T$ (Hz). For example when using 20 kHz PWM, the harmonics will occur at 20 kHz, 40 kHz, 60 kHz, and so on. An ideal brick wall filter with a cut-off at any frequency below 20 kHz would completely remove the high frequency harmonics, leaving only the low frequency D.C. component. Additionally, it would allow the PWM duty cycle to be varied at frequencies up to the cut-off frequency and reflect this variation with a corresponding voltage level change in the D.C. output. Of course, one cannot build an ideal filter, and a real filter will always allow some portion of the harmonics to pass. This will produce ripple in the desired output, as was shown in Figure 2. Filter design trade-offs will be discussed in a later section.

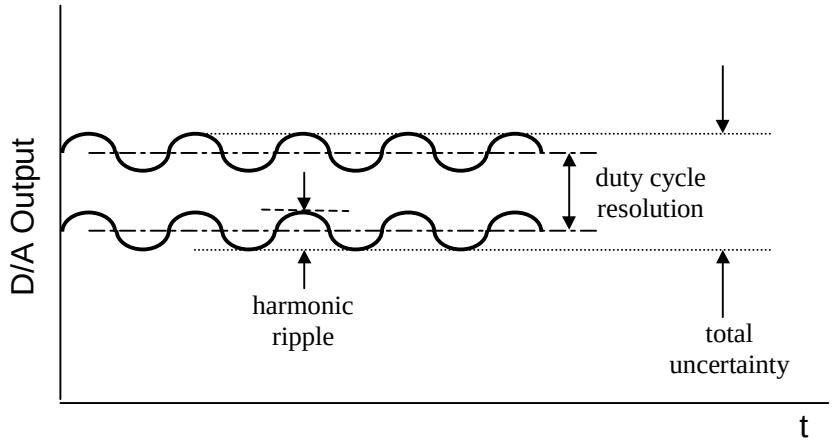
D/A Resolution Issues

Two main sources of error affect the desired D/A output. First, the PWM duty cycle can only be specified with finite resolution. On the TMS320C240, this resolution is directly related to the PWM carrier frequency used. For example, suppose 20 kHz PWM is desired with the DSP driven by a 20 MHz CPU clock. This gives 1000 clock counts per cycle of PWM, or just less than 10-bit resolution when specifying the timer compare value and hence the duty cycle. In other words, the desired D.C. output can only be

specified in steps of 5 mV (i.e. 5V/1000 counts). The second source of error is the peak-to-peak ripple produced by the unfiltered harmonics. These two sources of error sum together in equation (6) to yield the total uncertainty. This is graphically depicted in Figure 4.

$$\text{total uncertainty} = \text{harmonic ripple} + \text{duty cycle resolution} \quad (6)$$

Figure 4. Total Uncertainty in the D/A Output



One approach for improving the duty cycle resolution is to decrease the carrier frequency of the PWM. In the previous example, reducing the carrier frequency to 10 kHz from 20 kHz cuts the step size in half to 2.5 mV (i.e. ~11 bits resolution). However, the lower carrier frequency also decreases the base frequency of the unwanted harmonics in (1). In particular, the first harmonic will now appear at 10 kHz rather than 20 kHz, and more of it will pass through the analog low-pass filter, thereby increasing the harmonic ripple. A trade-off thus exists when selecting PWM frequency.

While the duty cycle resolution is easy to compute for a given carrier frequency, analytically quantifying the harmonic ripple is considerably more difficult (if not impossible) due to the infinite summation in (1). Instead, simulation can be used to study the steady-state ripple allowed by various low-pass filters. It is easy to show that a 50% duty cycle will maximize the energy contained in the first harmonic (i.e. n=1). This harmonic is arguably the most troublesome, since the energy in higher harmonics decreases as a function of $1/n^2$ regardless of the duty cycle. The value p = 0.5 will therefore be used for worst-case simulation studies.

Table 1 shows a simulation performance comparison of three different analog low-pass filters. While the simple 1st order RC filter provides the most cost-effective solution, its performance would clearly be lacking in most applications. The 2nd and 3rd order filters offer significantly better performance. With the 3rd order filter, the harmonic ripple is seen to be roughly on the same order as the duty cycle resolution. This illustrates well the aforementioned trade-off between duty-cycle resolution and harmonic ripple, as both PWM frequencies are seen to give similar total resolution, approximately 9 bits. Note that the table reflects theoretically achievable results. The performance of a real system will also be affected by noise.

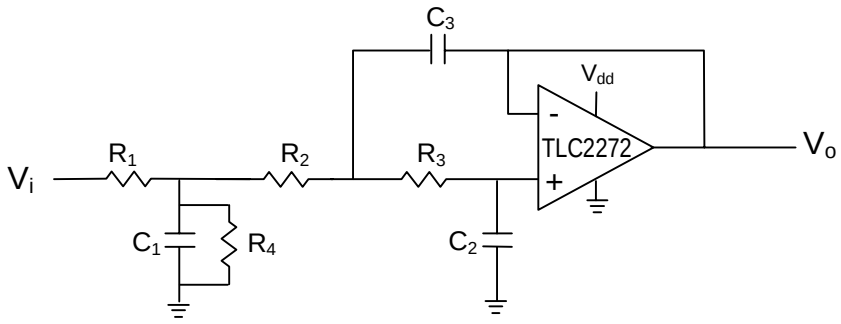
Table 1. Analog Low-Pass Filter Performance (simulation, 0-5V, 50% duty cycle PWM input)

Filter Order	Transfer Function	Parameters	-3dB Bandwidth (Hz)	PWM Freq. (kHz)	Harmonic Ripple (Vpp)	Duty Cycle Resolution (V)	Total Resolution (bits)
1st	$\frac{1}{RCs+1}$	RC = 1.6e-4 s/rad	1000	10	0.78	0.0025	2.7
				20	0.39	0.0050	3.7
2nd	$\frac{\omega_n^2}{s^2+2\zeta\omega_n s+\omega_n^2}$	ζ = 0.707 ω_n = 6283 rad/s	1000	10	0.062	0.0025	6.3
				20	0.016	0.0050	7.9
3rd	$\frac{1}{a_3s^3+a_2s^2+a_1s+a_0}$	a_3 = 1.35e-12 a_2 = 2.99e-8 a_1 = 2.75e-4 a_0 = 1	1000	10	0.0064	0.0025	9.1
				20	0.00081	0.0050	9.7

Analog Low-Pass Filter Design Example

Figure 5 shows one possible implementation of a 3rd order low-pass filter.

Figure 5. Circuit Diagram for 3rd Order Low-Pass Filter



The input-output transfer function for this filter is given by

$$\frac{V_0}{V_i} = \frac{1}{a_3 s^3 + a_2 s^2 + a_1 s + a_0} \tag{7}$$

where

$$a_0 = 1 + \frac{R_1}{R_4}$$

$$a_1 = R_1(C_1 + C_2) + (R_2 + R_3)C_2 + \frac{R_1}{R_4} C_2 (R_2 + R_3)$$

$$a_2 = R_3 C_2 C_3 (R_1 + R_2) + R_2 R_3 C_2 C_3 + \frac{R_1}{R_4} R_2 R_3 C_2 C_3$$

$$a_3 = R_1 R_2 R_3 C_1 C_2 C_3$$

A variety of commercial software package exist that can readily determine the coefficients a_0 through a_3 that give a particular filter bandwidth. However, finding the resistor and capacitor values that produce these coefficients requires one to solve the nonlinear set of equations given in (7). The nonlinearity of the equations makes finding a solution difficult enough, but in addition, there are only 4 equations with 7 unknowns, and hence a unique solution probably does not exist. Instead, a heuristic solution will be

provided [2]. The specific 3rd order filter listed in Table 1 may be constructed with the following nominal valued components:

R_1=1.6K R_2=2.4K R_3=7.5K R_4=∞ (not present) (8)
C_1=0.1µF C_2=0.01µF C_3=0.047µF

These components give a -3dB bandwidth of 1000 Hz. To obtain bandwidths different from 1000 Hz, one can leave all the above capacitor values and also R_4 unchanged, but scale the other resistor values as:

$$R_i^{new} = R_i \cdot \frac{1000\ Hz}{\text{new bandwidth}}, \quad i = 1, 2, 3. \tag{9}$$

The component R_4 allows for adjustment of the D.C. filter gain, the need for which will now be motivated. The TLC2272 operational amplifier is an Advanced LinCMOS™ rail-to-rail device from Texas Instruments that is fully specified for single-supply operation. It therefore can be powered from the same +5V supply that runs the TMS320C240 DSP. This eliminates the need for separate power circuitry, and hence reduces system cost. However, while the TLC2272 output is able to essentially swing rail-to-rail (e.g. 0.01 to 4.99 volts at 25° C with Vdd=+5V), the input voltage is limited to approximately 4 volts, which is incompatible with the +5V PWM outputs of the C240 (for complete device specifications on the TLC2272, see [3]). Two solutions to this problem are possible. First, one can use a dual sided power supply, but this adds system cost since additional power circuitry will be needed. Alternately, one can make the D.C. gain of the low-pass filter less than unity. The following provides a step-by-step approach to utilize resistor R_4 for this purpose:

1) Select component values according to (9) for the desired filter bandwidth.
2) Choose a desired full-scale D/A output range that is less than the op-amp input voltage limit (e.g. ~4 volts for the TLC227x)
3) Determine new R_1 and R_4 values by simultaneously solving the following:

™ Advanced LinCMOS is a trademark of Texas Instruments Incorporated.

$$\frac{\boldsymbol{R}_4}{\boldsymbol{R}_1 + \boldsymbol{R}_4} = \frac{\text{full scale range from step \#2}}{\text{PWM voltage}} \quad (10a)$$

$$\frac{\boldsymbol{R}_1 \boldsymbol{R}_4}{\boldsymbol{R}_1 + \boldsymbol{R}_4} = \boldsymbol{R}_1 \text{ from step \#1} \quad (10b)$$

Equation (10a) specifies the filter D.C. gain, while (10b) keeps the parallel D.C. impedance of R_1 and R_4 the same as the original R_1 from step #1. The PWM voltage is 5V for the TMS320C240. Note that this method is not mathematically exact. Performance of all filter designs should always be checked via simulation or experimentation.

The following represent equations (10a) and (10b) for a 1000 Hz bandwidth, 3 volt full-scale range design:

$$\frac{\boldsymbol{R}_4}{\boldsymbol{R}_1 + \boldsymbol{R}_4} = \frac{3\text{V}}{5\text{V}} \quad (11a)$$

$$\frac{\boldsymbol{R}_1 \boldsymbol{R}_4}{\boldsymbol{R}_1 + \boldsymbol{R}_4} = 1600\Omega \quad (11b)$$

The following component values result:

R_1=2.67K R_2=2.4K R_3=7.5K R_4=4.0K (12)
C_1=0.1µF C_2=0.01µF C_3=0.047µF

The filter represented by equation (12) will hereafter be referred to as the *modified 3rd order filter*. Simulation shows that the above component values actually yield a 1010 Hz bandwidth. Replacing resistors R_1 and R_4 with the nearest respective standard values of 2.7K and 3.9K results in a slight change in filter bandwidth to 1013 Hz. Considering significant figures and component tolerance, both bandwidths are 1000 Hz.

Figure 6 shows theoretical magnitude responses for three of the filters presented in this section. As expected, the modified 3rd order filter is seen to have a D.C. gain of approximately 0.6, whereas the other two filters have unity D.C. gains. Also, it is no surprise that the 3rd order filters have superior attenuation behavior after the 1000 Hz cutoff frequency. Figure 7 shows the phase characteristics of the filters. Phase should be considered in addition to magnitude when designing a closed-loop system or

when otherwise analyzing the filter outputs (i.e. the D/A output) since the frequency components of the output signal will each be phase delayed by a different amount, and hence distortion of the signal will occur. As would be expected, the 3rd order filters suffer from greater phase delay than the 1st order filter.

Figure 6. Magnitude Response of Analog Low-Pass Filters (Theoretical)

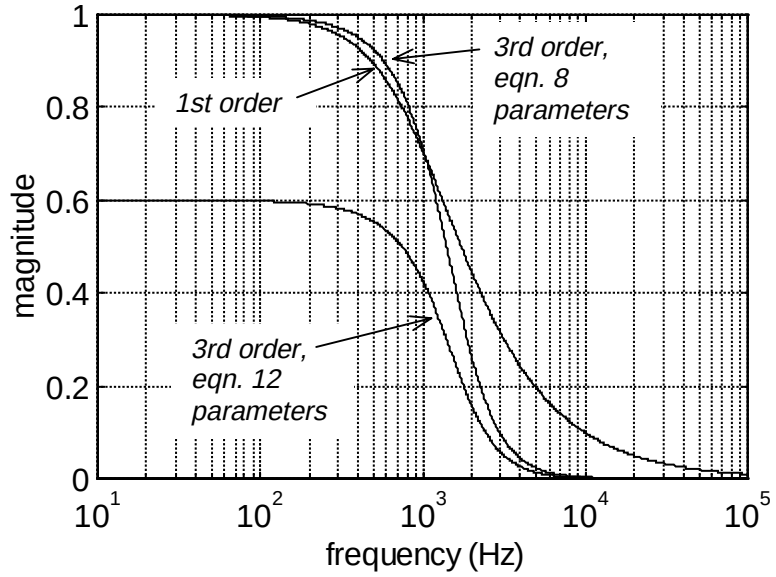
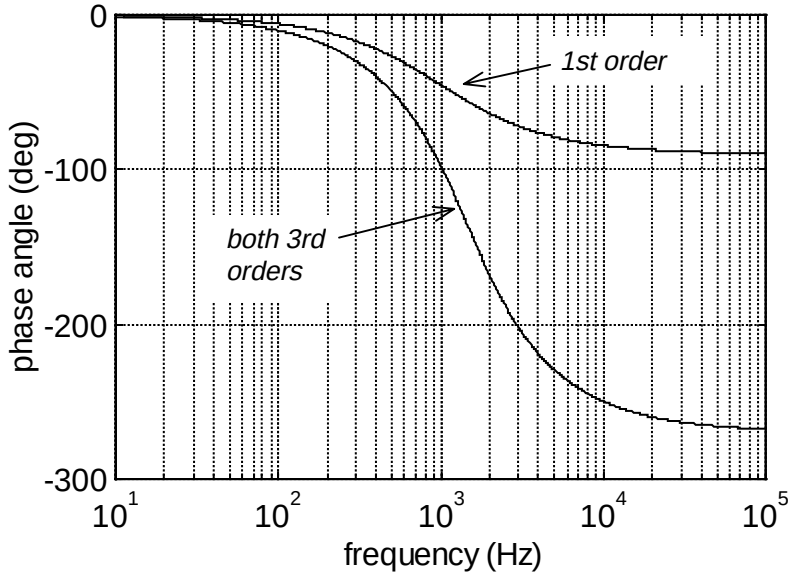


Figure 7.Phase Response of Analog Low-Pass Filters (Theoretical)



Experimental Setup and Results

Static and dynamic experimentation was performed to evaluate the performance of the 1st order filter (using R=1.6K Ω, and C=0.1 μF) and the modified 3rd order filter defined by equation (12). The TMS320F240 evaluation module (EVM) was utilized as the DSP platform for these tests. The F240 provided 20 kHz PWM input to the filters and simultaneously performed the data acquisition function (for downloading and plotting of the filter outputs) using its on-chip 10-bit analog-to-digital converter. The 10-bit A/D has a 4.9 mV resolution per bit, and a total accuracy of ±1.5 bits.

For the static test, the filters were driven with a constant 50% duty cycle PWM signal. Data acquisition was performed at a 125 kHz sample rate, and results are shown in Figure 8 and Figure 9. The expected outputs are constant voltage levels equal to half the full-scale ranges (e.g. 2.5 volts and 1.5 volts respectively for the 1st and modified 3rd order filters). The results show that the average value of each waveform matches the expected voltage level (although the modified 3rd order filter shows a slight discrepancy due to analog component tolerances). In addition, the 1st order filter shows the expected dominant oscillation at the fundamental 20 kHz frequency of the PWM. The amplitude of this oscillation is roughly 0.3 to 0.4 Vpp, which matches well the simulated results for harmonic ripple given in Table 1. The modified 3rd order filter shows no detectable ripple at 20 kHz since its amplitude is below the data acquisition resolution of 4.9 mV. It does however display some external circuit noise of roughly 20 mV peak-to-peak. Note that the resolution of the 10-bit A/D is quite evident in Figure 9.

For the dynamic tests, the filters were driven by a varying duty cycle PWM signal to produce full-scale output range amplitude sinewaves at frequencies of 10 Hz, 100 Hz, and 1000 Hz. Duty cycle variation was accomplished using a 100 point look-up table. The table entries represented one period of a sinewave, and were used to specify the compare register value for the PWM output. The frequency of the sinewave can be varied by changing the periodic update rate of the PWM compare register (i.e. there are 100 evenly spaced updates per desired sinewave period). Data acquisition was performed at a 20 kHz sample rate. Figures 10 through 12 shows the results. Of interest here is the amplitude attenuation suffered by the sinewave as frequency is increased. In Figure 10, the peak-to-peak amplitudes at 10 Hz are seen roughly equal to the expected full-scale ranges (i.e. 5 and 3 volts respectively for the 1st and 3rd order filters). However, at 1000 Hz, Figure 12 shows peak-to-peak amplitudes of only 3.4 volts for the 1st order filter and 2.0 volts for the 3rd order filter. These amplitudes represent an approximate 30% attenuation from zero frequency filter output (i.e. -3dB), and are to be expected from theory due to the 1000 Hz cutoff frequencies of both filters.

Figure 8. 1st Order Filter Output from 50% Duty Cycle PWM input (Experimental)

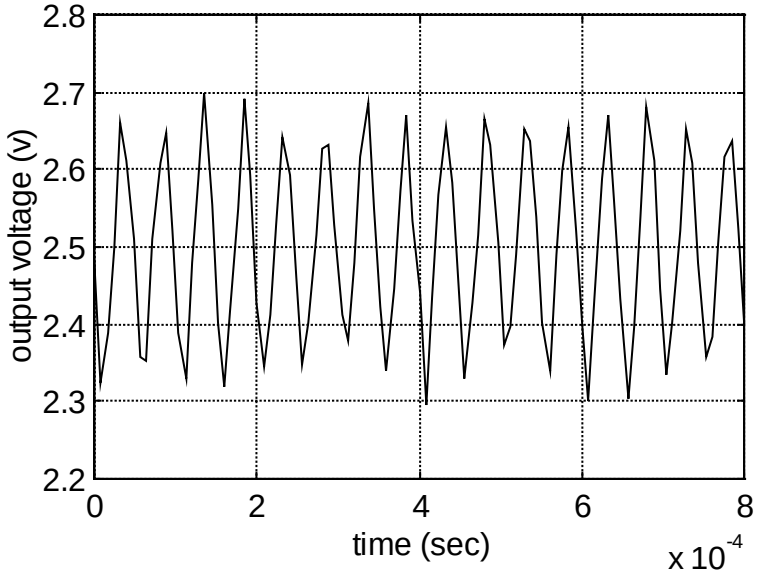


Figure 9. Modified 3rd Order Filter Output from 50% Duty Cycle PWM input (Experimental)

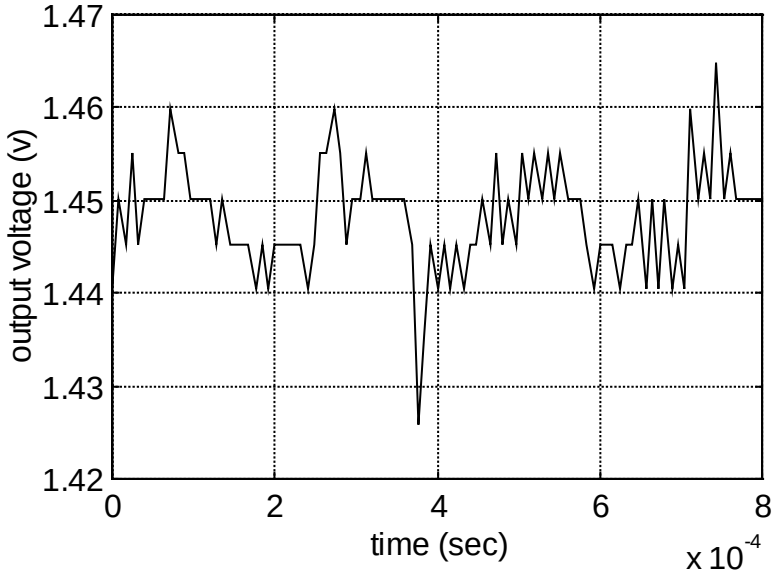


Figure 10. 10 Hz Sinewave Output from Low-Pass Filters (Experimental)

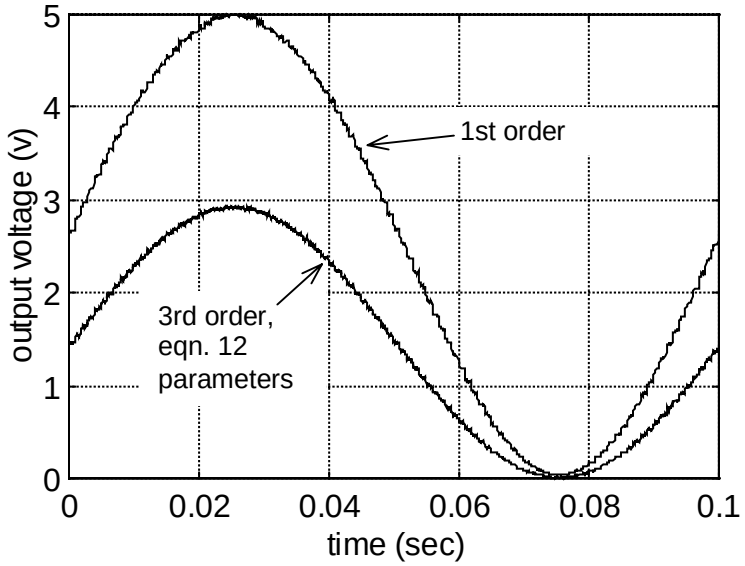


Figure 11. 100 Hz Sinewave Output from Low-Pass Filters (Experimental)

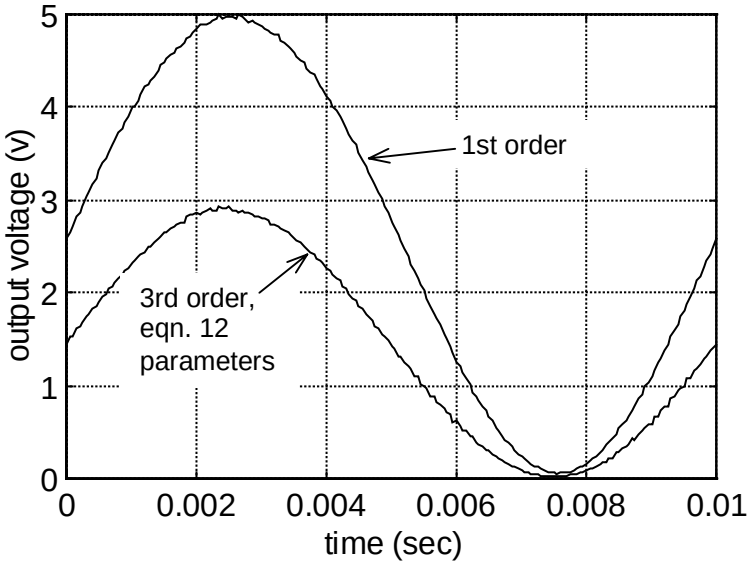
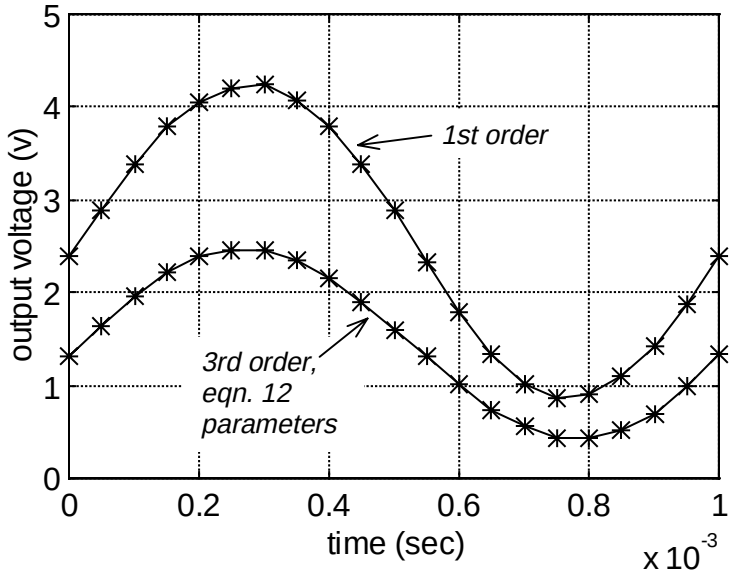


Figure 12. 1000 Hz Sinewave Output from Low-Pass Filters (Experimental)



Application Issues

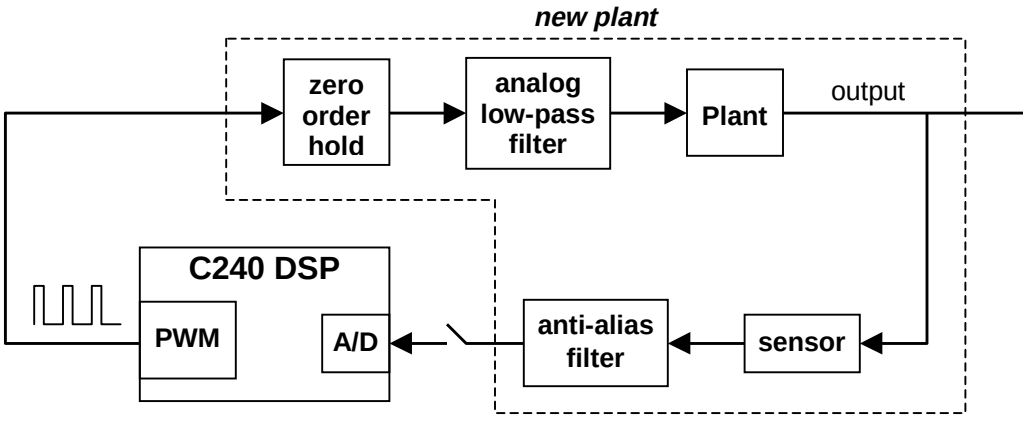
The D/A conversion bandwidth achievable with this approach is in the range of 500Hz to 1kHz, or perhaps even a bit higher depending on the analog low-pass filter bandwidth and the carrier frequency of the PWM. This is relatively low when compared to dedicated DAC chips, some of which can achieve bandwidths in the MHz range. However, such low D/A bandwidths are still applicable for a variety of applications The advantages of the PWM approach to D/A described in this paper are its low-cost (e.g. the cost of the analog low-pass filter) and its on-chip integration. No address decoding needs to be performed, as would be the case with a parallel DAC chip, nor are any of the serial interfaces used on the DSP (e.g. SCI or SPI serial ports on the TMS320C240) as would be the case with a serial DAC chip. Some example applications will be discussed next.

Man-machine interfacing: In this application, the D/A is used to provide feedback to a human system operator. For example, the D/A may drive a speaker used to generate different tones. Required bandwidths and resolution in these applications are generally quite low, and using the PWM as D/A should present few problems.

Real-time debug tool: During system design, it is often desired to monitor various software variables in real-time. By using D/A, quantities of interest can be used to specify the PWM compare register value, and hence control the PWM duty cycle. After analog filtering, the signals corresponding to these values can be observed on a display device, such as an oscilloscope. Examples of commonly monitored quantities include digital sensor inputs such as the quadrature encoder count, state-variables such as position or velocity, or specially calculated debug variables such as RMS current. The D/A resolution required for this application is typically low enough that a simple 1st order RC filter can be used as the analog low-pass filter, thereby providing a quick and cheap method for performing system debug.

Closed-loop control: A 1000 Hz D/A bandwidth is often sufficient in less demanding closed-loop control systems. For example, sample rates in conventional PID servo control are typically on the order of 100 to 500 Hz, and hence higher frequency signals will not need to be passed to the plant. One approach to handling the D/A analog low-pass filter is to consider it part of the plant (i.e. the system to be controlled) during controller design. This will help ensure a stable closed-loop system since the controller design will incorporate the dynamic response of the filter. Figure 13 shows a block diagram for a typical closed-loop system. When designing the controller, the new plant might be defined as the series connection of the D/A analog low-pass filter, the original plant, the output sensor, and the anti-alias filter on the A/D. When performing discrete-domain controller design, one would also include the zero-order hold block.

Figure 13. Closed-Loop Control Block Diagram



General: A final application issue concerns the peak-to-peak voltage level of the PWM outputs on the TMS320C240 DSP family. The D/A method presented in this paper relies on a 0-5 volt peak-to-peak PWM output in order to relate the D/A output voltage to each particular PWM duty cycle. Deviation from 0-5 volts will change the duty-cycle to D/A output mapping. It should be realized that all PWM outputs on the C240 DSP are specified only as TTL in the data sheet [4]. In reality however, the PWM outputs do essentially swing from ground to the supply voltage (V_{dd}). The exact PWM voltage level is a function of current draw on the PWM pin, which will be determined by the analog low-pass filter used. Depending on the application, this may not be a concern. The C240 data sheet [4] contains some information on output voltage levels versus current draw. In situations where it is desired to know the exact duty-cycle to output voltage mapping, one could experimentally determine the PWM output voltage for the particular low-pass filter circuitry employed. In particularly problematic situations, one remedy is to insert an analog voltage comparator between the PWM pin and the analog low-pass filter. The PWM signal provides one input to the comparator, and a logic-high voltage level that is lower than the high-level swing of the PWM provides the other input. The comparator output will essentially reproduce the original PWM signal but with more precisely known amplitude.

Summary

Digital-to-analog conversion can be achieved on the TMS320C240 DSP by analog low-pass filtering a PWM output signal. The D.C. amplitude of the D/A output has been shown to be directly proportional to the PWM duty cycle. This is the fundamental enabler for this D/A method on the C240 DSP. The achievable D/A bandwidth of this method is arguably low, on the order of 500 Hz to 1 kHz. However, such low bandwidths are still useful for real-time system debug, and also in applications not demanding high-performance, such as low-speed servo control, or man-machine interfacing. When compared to a dedicated DAC chip, the presented method for D/A offers low cost and ease of interfacing with the DSP.

References

[1] Hildebrand, F.B., “Advanced Calculus for Applications,” Prentice-Hall Inc., Englewood Cliffs, New Jersey, 2nd edition, 1976, pp. 214-223.

[2] Horwitz, P., and Hill, W., “The Art of Electronics,” Cambridge University Press, New York, NY, 2nd edition, ISBN 0-521-37095-7, pp.306.

[3] "TLC227x, TLC227xA, TLC227xY Data Sheet," Texas Instruments Literature #SLOS190, February, 1997.

[4] "TMS320C240, TMS320F240 DSP Controllers Data Sheet," Texas Instruments Literature #SPRS042B, May 1998.