International
IOR Rectifier

ADVANCE DATA

Data Sheet No. PD60213

IR2214/IR22141

HALF-BRIDGE GATE DRIVER IC

Features

- Floating channel up to +1200V
- Soft overcurrent shutdown
- Synchronization signal to synchronize shut down with the other phases
- Integrated desaturation detection circuit
- Two stage turn on output for di/dt control
- Separate pull-up/pull-down output drive pins
- Matched delay outputs
- Under voltage lockout with hysteresis band

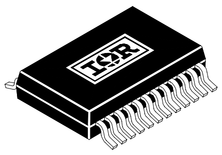
Product Summary

V_{OFFSET}	1200V max.
I_O+/- (typ.)	2.0 A / 3.0A
V_{OUT}	10.4V - 20V
Deadtime matching (max)	75nsec
Deadtime (typ)	330nsec
Desat blanking time (typ)	3µsec
DSH,DSL input voltage threshold (typ)	8.0V
Soft shutdown time (typ)	9.6µsec

Description

The IR2214/IR22141 is a gate driver suited to drive a single half bridge in power switching applications. The high gate driving capability (2A source, 3A sink) and the low quiescent current enable bootstrap supply techniques in medium power systems. The IR2214/IR22141 driver features full short circuit protection by means of the power transistor desaturation detection. The IR2214/IR22141 manages all the half-bridge faults by turning off smoothly the desaturated transistor through the dedicated soft shut down pin, therefore preventing over-voltages and reducing EM emissions. In multi-phase system IR2214/IR22141 drivers communicate using a dedicated local network (SY_FLT and FAULT/SD signals) to properly manage phase-to-phase short circuits. The system controller may force shutdown or read device fault state through the 3.3 V compatible CMOS I/O pin (FAULT/SD). To improve the signal immunity from DC-bus noise, the control and power ground use dedicated pins enabling low-side emitter current sensing as well. Under voltage conditions in floating and low voltage circuits are managed independently.

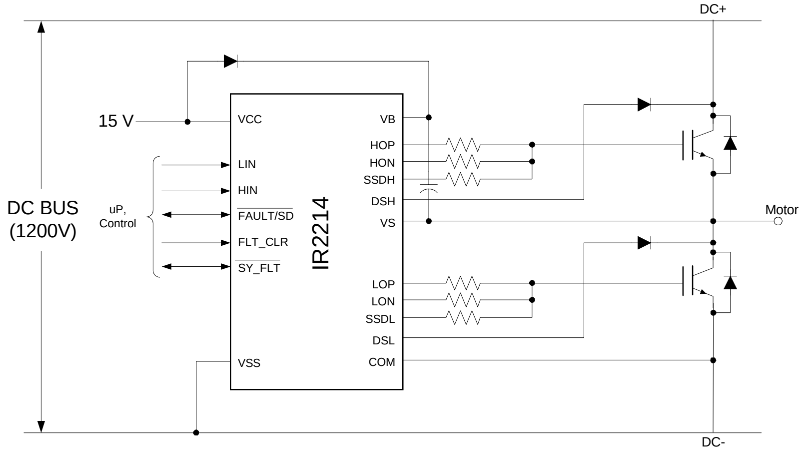
Package



24-Lead SSOP

Typical Connection

(Refer to Lead Assignments for correct pin configuration). This/These diagram(s) show electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.



Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to $V_{SS,}$ all currents are defined positive into any lead The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
V_S	High side offset voltage	V_B - 25	V_B + 0.3	V
V_B	High side floating supply voltage	-0.3	1225	
V_{HO}	High side floating output voltage (HOP, HON and SSDH)	V_S - 0.3	V_B + 0.3	
V_{CC}	Low side and logic fixed supply voltage	-0.3	25	
COM	Power ground	V_{CC} - 25	V_{CC} + 0.3	
V_{LO}	Low side output voltage (LOP, LON and SSDL)	V_{COM} -0.3	V_{CC} + 0.3	
V_{IN}	Logic input voltage (HIN, LIN and FLT_CLR)	-0.3	V_{CC} + 0.3	
V_{FLT}	FAULT input/output voltage (FAULT/SD and SY_FLT)	-0.3	V_{CC} + 0.3	
V_{DSH}	High side DS input voltage	V_B -25	V_B + 0.3	
V_{DSL}	Low side DS input voltage	V_{CC} - 25	V_{CC} + 0.3	
dV_S/dt	Allowable offset voltage slew rate	—	50	V/ns
P_D	Package power dissipation @ $T_A \le$ +25°C	—	1.5	W
Rth_{JA}	Thermal resistance, junction to ambient	—	65	°C/W
T_J	Junction temperature	—	150	°C
T_S	Storage temperature	-55	150	
T_L	Lead temperature (soldering, 10 seconds)	—	300	

Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions. All voltage parameters are absoute voltages referenced to $V_{SS.}$ The V_S offset rating is tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
V_B	High side floating supply voltage (Note 1)	V_S + 11.5	V_S + 20	V
V_S	High side floating supply offset voltage	Note 2	1200	
V_{HO}	High side output voltage (HOP, HON and SSDH)	V_S	V_S + 20	
V_{LO}	Low side output voltage (LOP, LON and SSDL)	V_{COM}	V_{CC}	
V_{CC}	Low side and logic fixed supply voltage (Note 1)	11.5	20	
COM	Power ground	- 5	5	
V_{IN}	Logic input voltage (HIN, LIN and FLT_CLR)	0	V_{CC}	
V_{FLT}	Fault input/output voltage (FAULT/SD and SY_FLT)	0	V_{CC}	
V_{DSH}	High side DS pin input voltage	V_B - 20	V_B	
V_{DSL}	Low side DS pin input voltage	V_{CC} - 20	V_{CC}	
T_A	Ambient temperature	-40	125	°C

Note 1: While internal circuitry is operational below the indicated supply voltages, the UV lockout disables the output drivers if the UV thresholds are not reached.

Note 2: Logic operational for VS from VSS-5 to VSS+1200V. Logic state held for VS from VSS-5V to VSS-VBS. (Please refer to the Design Tip DT97-3 for more details).

Static Electrical Characteristics

V_{CC} = 15 V, V_{SS} = COM = 0 V, V_S = 0 ÷ 1200 V and T_A = 25 °C unless otherwise specified.

Pin: V_{CC}, V_{SS}, V_B, V_S

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
V_{CCUV+}	Vcc supply undervoltage positive going threshold	9.3	10.2	11.4	V	
V_{CCUV-}	Vcc supply undervoltage negative going threshold	8.7	9.3	10.3		
V_{CCUVH}	Vcc supply undervoltage lockout hysteresis	-	0.9	-		
V_{BSUV+}	(V_B-V_S) supply undervoltage positive going threshold	9.3	10.2	11.4		V_S=0V, V_S=1200V
V_{BSUV-}	(V_B-V_S) supply undervoltage negative going threshold	8.7	9.3	10.3		V_S=0V, V_S=1200V
V_{BSUVH}	(V_B-V_S) supply undervoltage lockout hysteresis	-	0.9	-		
I_{LK}	Offset supply leakage current	-	-	50	µA	V_B = V_S = 1200V
I_{QBS}	Quiescent V_{BS} supply current	-	400	800		V_{IN} = 0V or 3.3V
I_{QCC}	Quiescent Vcc supply current	-	0.7	2.5	mA	(No load)

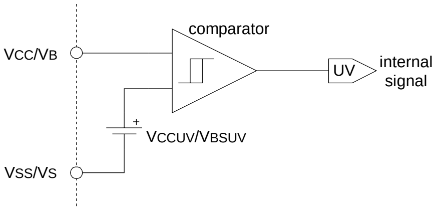


Figure 1: Undervoltage diagram

Pin: HIN, LIN, FLTCLR, $\overline{\text{FAULT/SD}}$, $\overline{\text{SY\_FLT}}$

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
V_{IH}	Logic "1" input voltage	2.0	-	-	V	V_{CC} = V_{CCUV-} to 20V
V_{IL}	Logic "0" input voltage	-	-	0.8		
V_{IHSS}	Logic input hysteresis	0.2	0.4	-		
I_{IN+}	Logic "1" input bias current	-	370	-	µA	V_{IN} = 3.3V
I_{IN-}	Logic "0" input bias current	-1	-	0	µA	V_{IN} = 0V
$R_{ON,FLT}$	FAULT/SD open drain resistance	-	60	-	Ω	
$R_{ON,SY}$	SY_FLT open drain resistance	-	60	-		P ≤7 µs

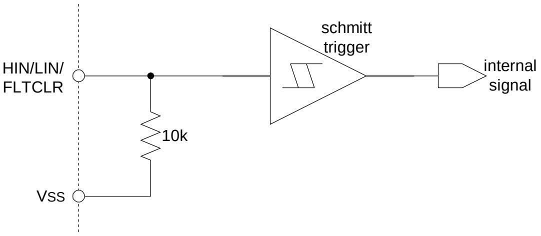


Figure 2: HIN, LIN and FLTCLR diagram

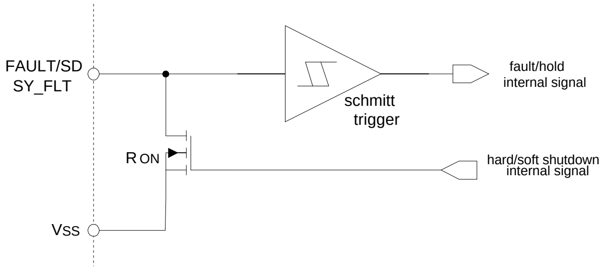


Figure 3: FAULT/SD and SY_FLT diagram

Pin: DSL, DSH

The active bias is present only in IR22141. V_{DESAT}, I_{DS} and I_{DSB} parameters are referenced to COM and V_S respectively for DSL and DSH.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
V_{DESAT+}	High desat input threshold voltage	7.2	8.0	8.8	V	See Fig. 16, 4
V_{DESAT-}	Low desat input threshold voltage	6.3	7.0	7.7		
V_{DSTH}	Desat input voltage hysteresis	-	1.0	-		
I_{DS+}	High DSH or DSL input bias current	-	21	-	µA	$V_{DESAT} = V_{CC}$ or V_{BS}
I_{DS-}	Low DSH or DSL input bias current	-	-160	-		$V_{DESAT} = 0V$
I_{DSB}	DSH or DSL input bias current (IR22141 only)	-	-20	-	mA	$V_{DESAT} = (V_{CC}$ or $V_{BS}) - 2V$

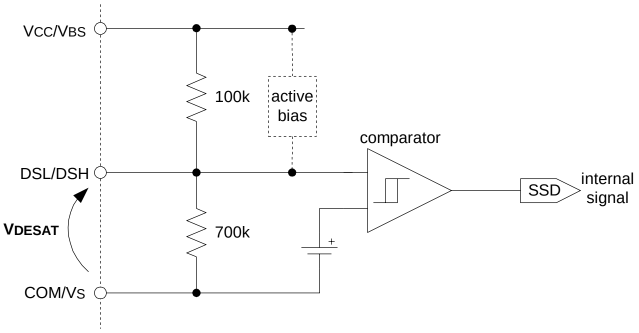


Figure 4: DSH and DSL diagram

Pin: HOP, LOP

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
V_{OH}	High level output voltage, V_B – V_{HOP} or V_{CC} –V_{LOP}	-	20	100	mV	I_O = 1mA
I_{O1+}	Output high first stage short circuit pulsed current	-	2	-	A	$V_{HOP/LOP}$=0V, H_{IN} or L_{IN}= 1, PW≤200ns, resistive load, see Fig. 8
I_{O2+}	Output high second stage short circuit pulsed current	-	1	-		$V_{HOP/LOP}$=0V, H_{IN} or L_{IN} = 1, 400ns≤PW≤10µs, resistive load, see Fig. 8

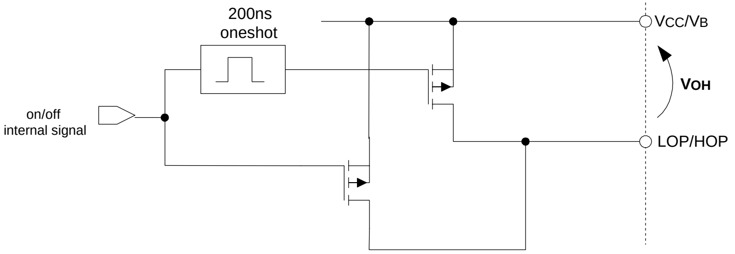


Figure 5: HOP and LOP diagram

Pin: HON, LON, SSDH, SSDL

V_{OL}	Low level output voltage, V_{HON} or V_{LON}	-	2.3	15	mV	I_O = 1mA
$R_{ON,SSD}$	Soft Shutdown on resistance (Note 1)	-	90	-	Ω	PW ≤ 7 µs
I_{O-}	Output low short circuit pulsed current	-	3	-	A	$V_{HOP/LOP}$=15V, H_{IN} or L_{IN} = 0, PW≤10µs

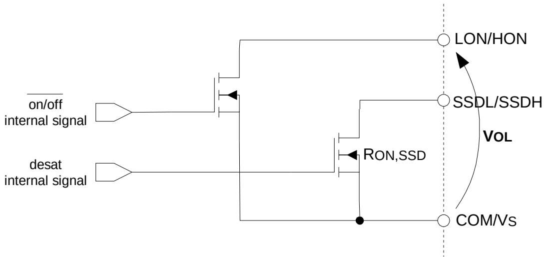


Figure 6: HON, LON, SSDH and SSDL diagram

AC Electrical Characteristics

$V_{CC} = V_{BS} = 15V$, $V_S = V_{SS}$ and $T_A = 25°C$ unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn on propagation delay	220	440	660	ns	V_{IN} = 0 & 1 V_S = 0 to 1200V HOP shorted to HON, LOP shorted to LON, Figure 7, 10
t_{off}	Turn off propagation delay	220	440	660		
t_r	Turn on rise time (C_{LOAD}=1nF)	—	24	—		
t_f	Turn off fall time (C_{LOAD}=1nF)	—	7	—		
t_{on1}	Turn on first stage duration time	120	200	280		Figure 8
t_{DESAT1}	DSH to HO soft shutdown propagation delay at HO turn on	2000	3300	4600		V_{HIN}= 1 V_{DESAT} = 15V,Fig.10
t_{DESAT2}	DSH to HO soft shutdown propagation delay after Blanking	1050	—	—		
t_{DESAT3}	DSL to LO soft shutdown propagation delay at LO turn on	2000	3300	4600		V_{LIN} = 1 V_{DESAT} = 15V,Fig.10
t_{DESAT4}	DSL to LO soft shutdown propagation delay after Blanking	1050	—	—		
t_{DS}	Soft shutdown minimum pulse width of desat	1000	—	—		Figure 9
t_{SS}	Soft shutdown duration period	5700	9600	13500		C_L=TBD µF, V_{DS}=15V,Fig. 9
$t_{SY\_FLT,DESAT1}$	DSH to SY_FLT propagation delay at HO turn on	—	3600	—		V_{HIN} = 1 V_{DS} = 15V, Fig. 10
$t_{SY\_FLT,DESAT2}$	DSH to SY_FLT propagation delay after blanking	1300	—	—		
$t_{SY\_FLT,DESAT3}$	DSL to SY_FLT propagation delay at LO turn on	—	3050	—		V_{LIN} = 1 V_{DESAT}=15V,Fig.10
$t_{SY\_FLT,DESAT4}$	DSL to SY_FLT propagation delay after blanking	1050	—	—		
t_{BL}	DS blanking time at turn on	—	3000	—		V_{HIN} = V_{LIN} = 1 V_{DESAT}=15V,Fig.10
	Dead-time/Delay Matching Characteristics					
DT	Dead-time	—	330	—		Figure 11
MDT	Dead-time matching, MDT=DTH-DTL	—	—	75		External DT=0nsec Figure 11
PDM	Propagation delay matching, Max(t_{on}, t_{off}) - Min(t_{on}, t_{off})	—	—	75		External DT> 500nsec, Fig.7

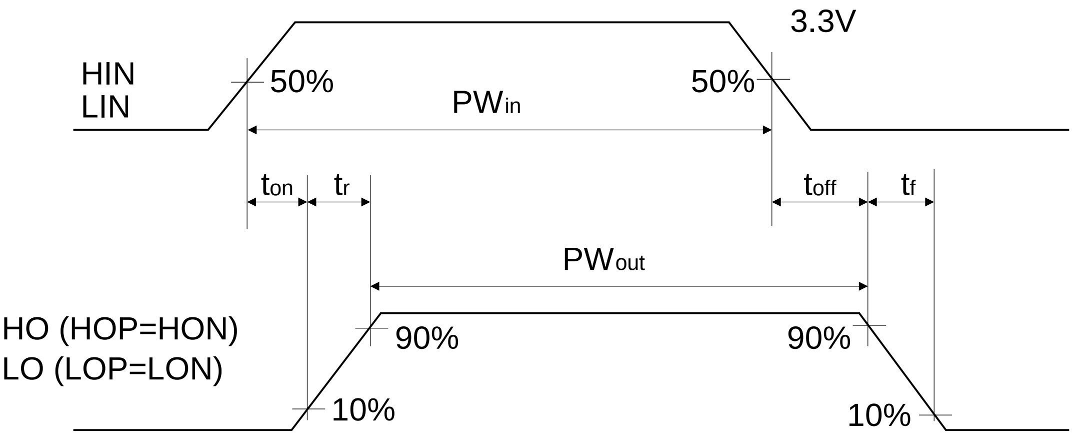


Figure 7: Switching Time Waveforms

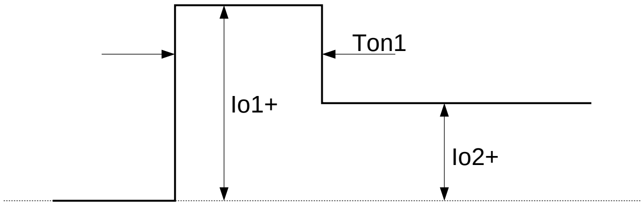


Figure 8: Output Source Current

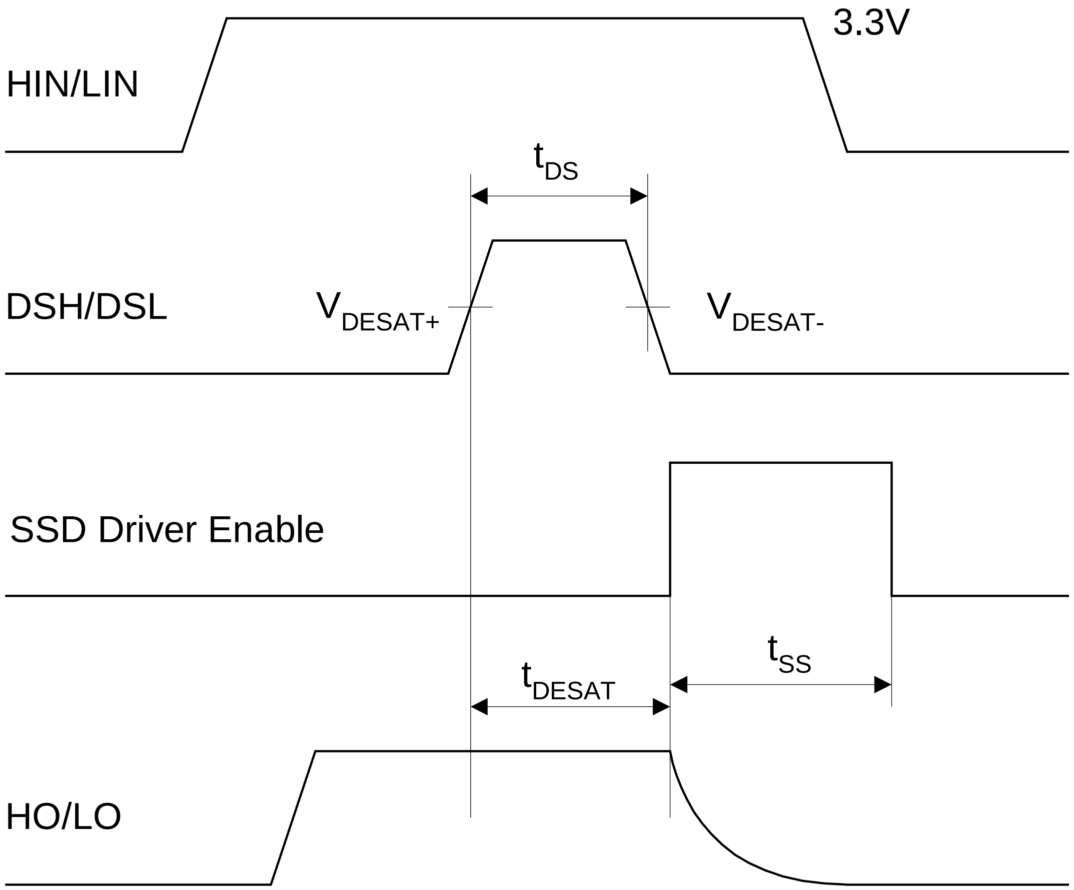


Figure 9: Soft Shutdown Timing Waveform

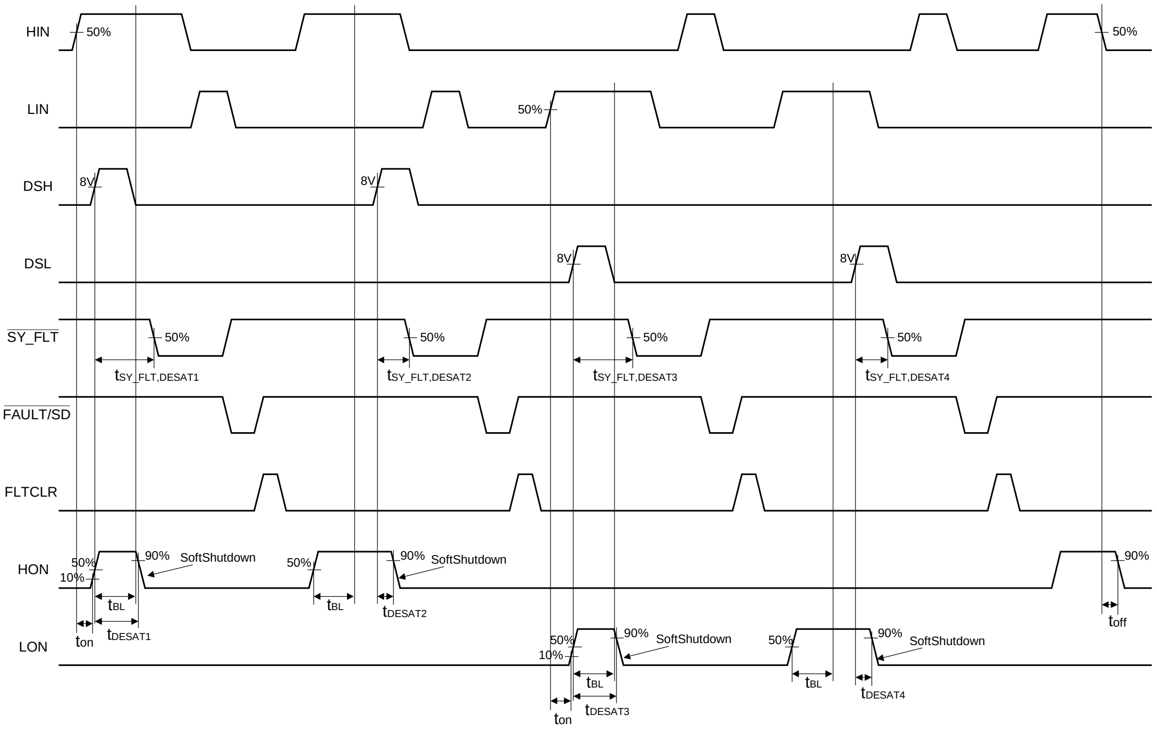
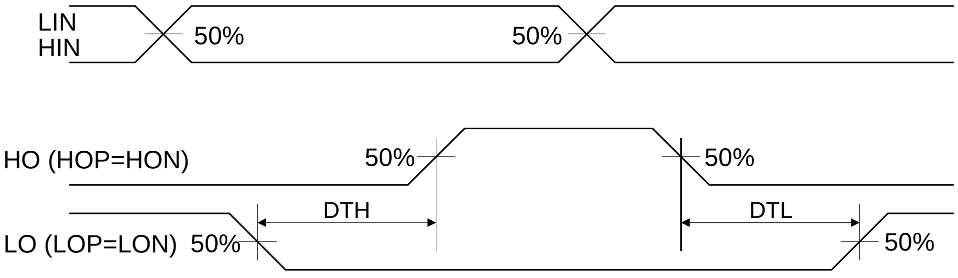


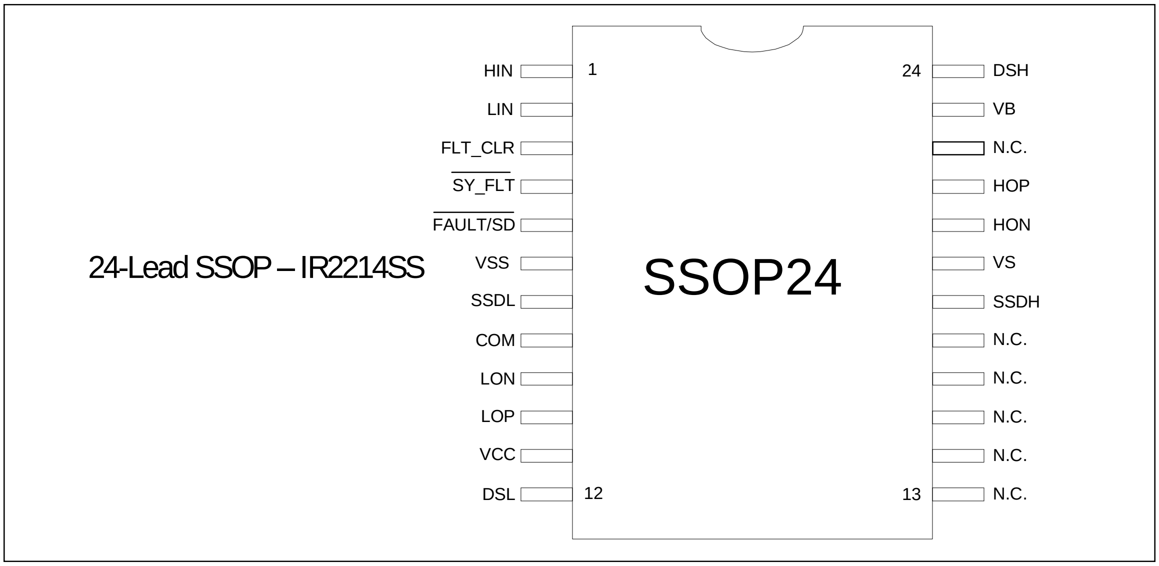
Figure 10: Desat Timing



MDT=DTH-DTL

Figure 11: Internal Dead-Time Timing

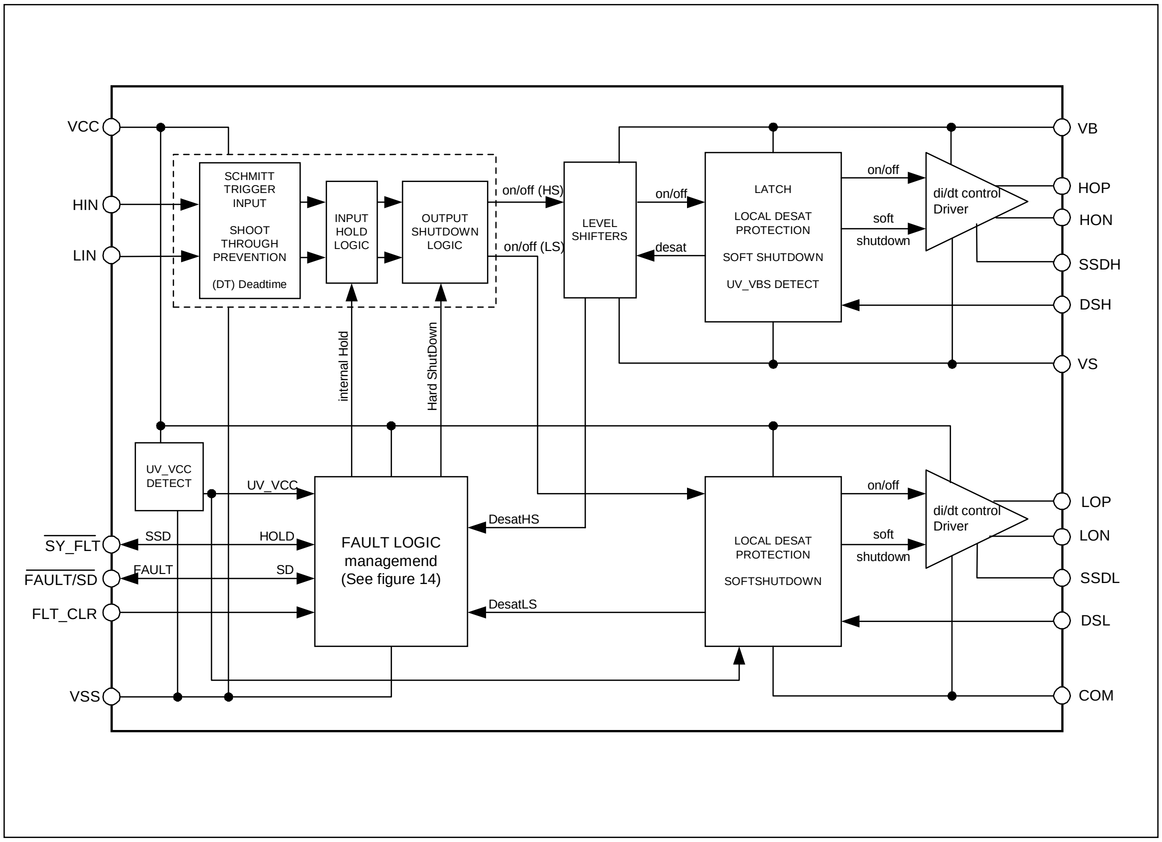
Lead Assignments



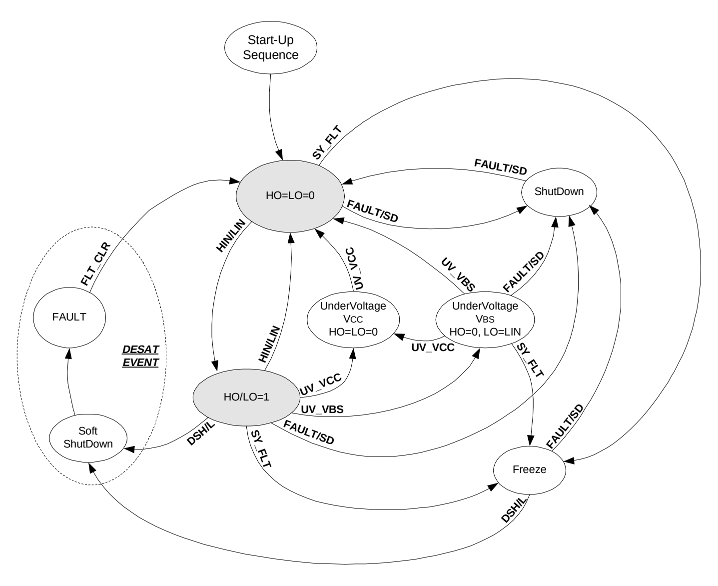
Lead Definitions

Symbol	Description
VCC	Low side gate driver supply
VSS	Logic Ground
HIN	Logic input for high side gate driver outputs (HOP/HON)
LIN	Logic input for low side gate driver outputs (LOP/LON)
$\overline{\text{FAULT/SD}}$	Dual function (in/out) active low pin. Refer to figures 17, 18 and 15. As an output, indicates fault condition. As an input, shuts down the outputs of the gate driver regardless H_{IN}/L_{IN} status.
$\overline{\text{SY\_FLT}}$	Dual function (in/out) active low pin. Refer to figures 17, 18 and 15. As an output, indicates SSD sequence is occurring. As an input, an active low signal freezes both output status.
FLT_CLR	Fault clear active high input. Clears latched fault condition (See figure 17)
LOP	Low side driver sourcing output
LON	Low side driver sinking output
DSL	Low side IGBT desaturation protection input
SSDL	Low side soft shutdown
COM	Low side driver return
VB	High side gate driver floating supply
HOP	High side driver sourcing output
HON	High side driver sinking output
DSH	High side IGBT desaturation protection input
SSDH	High side soft shutdown
VS	High side floating supply return

Functional Block Diagram



State Diagram



Stable State
- FAULT
- HO=LO=0 (Normal operation)
- HO/LO=1 (Normal operation)
- UNDERVOLTAGE V_{CC}
- SHUTDOWN (SD)
- UNDERVOLTAGE V_{BS}
- FREEZE

Temporary State
- SOFT SHUTDOWN
- START UP SEQUENCE

System Variable
- FLT_CLR
- HIN/LIN
- UV_VCC
- UV_VBS
- DSH/L
- SY_FLT
- FAULT/SD

NOTE1: a change of logic value of the signal labeled on lines (system variable) generates a state transition.
NOTE2: Exiting from UNDERVOLTAGE V_{BS} state, the HO goes high only if a rising edge event happens in H_{IN}.

IR2214 Logic Table

Output drivers status description

HO/LO status	HOP/LOP	HON/LON	SSDH/SSDL
0	HiZ	0	HiZ
1	1	HiZ	HiZ
SSD	HiZ	HiZ	0
LO/HO	Output follows inputs (in=1->out=1, in=0->out=0)		
LO_{n-1}/HO_{n-1}	Output keeps previous status		

	INPUTS			**INPUT/OUTPUT**		**Under Voltage** Yes: V< UV threshold No : V> UV threshold X : don't care		**OUTPUTS**	
Operation	**Hin**	**Lin**	**FLT_CLR**	**SY_FLT** SSD: desat (out) HOLD: freezing (in)	**FAULT/SD** SD: shutdown (in) FAULT: diagnostic (out)	**V_{CC}**	**V_{BS}**	**HO**	**LO**
Shut Down	X	X	X	X	0 (SD)	X	X	0	0
Fault Clear	H_{IN}	L_{IN}	↑	NOTE1	↑ (FAULT)	No	No	HO	LO
Normal Operation	1	0	0	1	1	No	No	1	0
	0	1	0	1	1	No	No	0	1
	0	0	0	1	1	No	No	0	0
Anti Shoot Through	1	1	0	1	1	No	No	0	0
Soft Shut Down (entering)	1	0	0	↓ (SSD)	1	No	No	SSD	0
	0	1	0	↓ (SSD)	1	No	No	0	SSD
Soft Shut Down (finishing)	X	X	0	↑ (SSD)	↓ (FAULT)	No	No	0	0
	X	X	0	↑ (SSD)	↓ (FAULT)	No	No	0	0
Freeze	X	X	X	0 (HOLD)	1	No	No	HO_{n-1}	LO_{n-1}
Under Voltage	X	L_{IN}	X	1	1	No	Yes	0	LO
	X	X	X	1	0 (FAULT)	Yes	X	0	0

NOTE1: SY_FLT automatically resets after SSD event is over and FLT_CLR is not required. In order to avoid FLT_CLR to conflict with the SSD procedure, FLT_CLR should not be operated while SY_FLT is active.

FEATURES DESCRIPTION

1. Start-up sequence

At power supply start-up it is recommended to keep FLT_CLR pin active until supply voltages are properly established. This prevents spurious diagnostic signals being generated. All protection functions are operating independently from FLT_CLR status and output driver status reflects the input commands.

When bootstrap supply topology is used for supplying the floating high side stage, the following start-up sequence is recommended (see also figure 12):

1. Set Vcc
2. Set FLT_CLR pin to HIGH level
3. Set LIN pin to HIGH level and let the bootstrap capacitor be charged
4. Release LIN pin to LOW level
5. Release FLT_CLR pin to LOW level

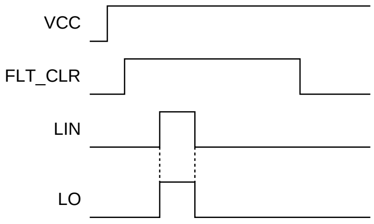


Figure 12 Start-up sequence

A minimum 15μs LIN and FLT-CLR pulse is required.

2. Normal operation mode

After start-up sequence has been terminated, the device becomes fully operative (see grey blocks in the State Diagram).

HIN and LIN produce driver outputs to switch accordingly, while the input logic checks the input signals preventing shoot-through events and including DeadTime (DT).

3. Shut down

The system controller can asynchronously command the Hard ShutDown (HSD) through the 3.3 V compatible CMOS I/O FAULT/SD pin. This event is not latched.

In a multi-phase system, FAULT/SD signals are or-wired so the controller or one of the gate drivers can force simultaneous shutdown to the other gate drivers through the same pin.

4. Fault management

IR2214 is able to manage both the supply failure (undervoltage lock out on both low and high side circuits) and the desaturation of both power transistors.

4.1 Undervoltage (UV)

The Undervoltage protection function disables the driver's output stage preventing the power device being driven with too low voltages.

Both the low side (V_{CC} supplied) and the floating side (V_{BS} supplied) are controlled by a dedicate undervoltage function.

Undervoltage event on the V_{CC} (when $V_{CC} < UV_{VCC-}$) generates a diagnostic signal by forcing FAULT/SD pin low (see FAULT/SD section and figure 14). This event disables both low side and floating drivers and the diagnostic signal holds until the under voltage condition is over. Fault condition is not latched and the FAULT/SD pin is released once V_{CC} becomes higher than UV_{VCC+}.

The undervoltage on the V_{BS} works disabling only the floating driver. Undervoltage on V_{BS} does not prevent the low side driver to activate its output nor generate diagnostic signals. V_{BS} undervoltage condition ($V_{BS} < UV_{VBS-}$) latches the high side output stage in the low state. V_{BS} must be reestablished higher than UV_{VBS+} to return in normal operating mode. To turn on the floating driver H_{IN} must be re-asserted high (rising edge event on H_{IN} is required).

4.2 Power devices desaturation

Different causes can generate a power inverter failure: phase and/or rail supply short-circuit, overload conditions induced by the load, etc… In all these fault conditions a large current increase is produced in the IGBT.
The IR2214 fault detection circuit monitors the IGBT emitter to collector voltage (V_{CE}) by means of an external high voltage diode. High current in the IGBT may cause the transistor to desaturate, i.e. V_{CE} to increase.
Once in desaturation, the current in power transistor can be as high as 10 times the nominal current. Whenever the transistor is switched off, this high current generates relevant voltage transients in the power stage that need to be smoothed out in order to avoid destruction (by over-voltages). The IR2214 gate driver accomplish the transients control by smoothly turning off the desaturated transistor by means of the SSD pin activating a so called *Soft ShutDown* sequence (SSD).

4.2.1 Desaturation detection: DSH/L function

Figure 13 shows the structure of the desaturation sensing and soft shutdown block. This configuration is the same for both high and low side output stages.

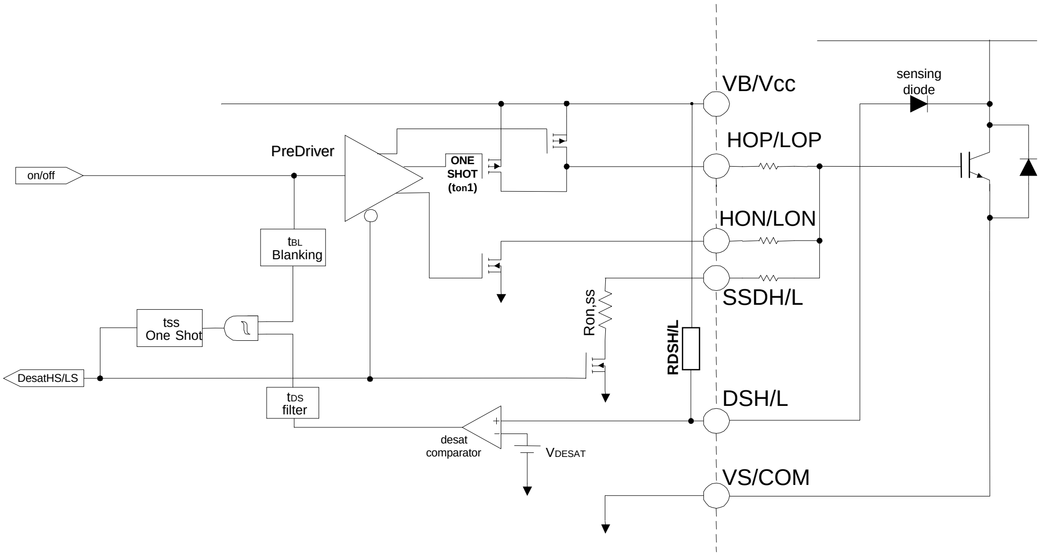


Figure 13: high and low side output stage

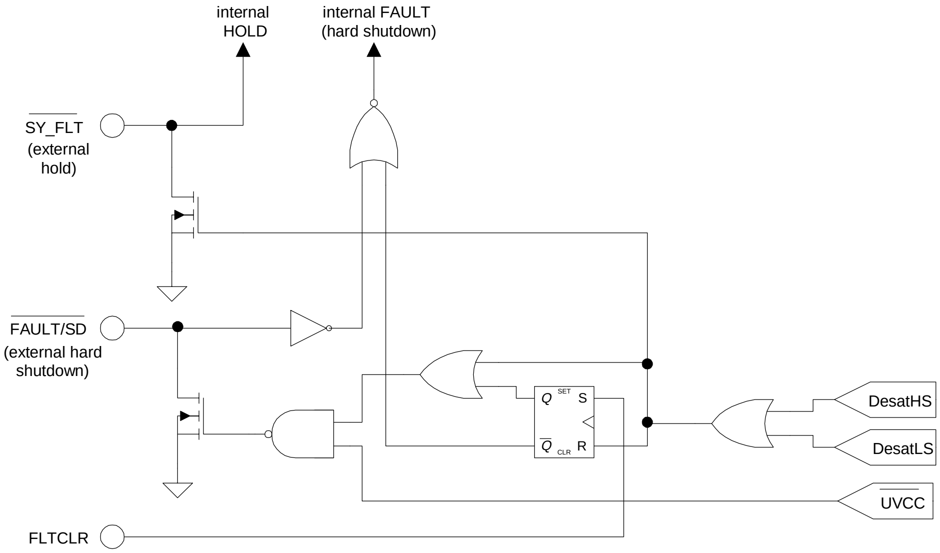


Figure 14: fault management diagram

The external sensing diode should have BV>1200V and low stray capacitance (in order to minimize noise coupling and switching delays). The diode is biased by an internal pull-up resistor $R_{DSH/L}$ (equal to V_{CC}/I_{DS-} or V_{BS}/I_{DS-} for IR2214) or by a dedicated circuit (see the active-bias section for the IR22141). When V_{CE} increases, the voltage at DSH/L pin increases too. Being internally biased to the local supply, DSH/L voltage is automatically clamped. When DSH/L exceeds the V_{DESAT+} threshold the comparator triggers (see figure 13). Comparator output is filtered in order to avoid false desaturation detection by externally induced noise; pulses shorter than t_{DS} are filtered out. To avoid detecting a false desaturation during IGBT turn on, the desaturation circuit is disabled by a Blanking signal (T_{BL}, see Blanking block in figure 13). This time is the estimated maximum IGBT turn on time and must be not exceeded by proper gate resistance sizing. When the IGBT is not completely saturated after T_{BL}, desaturation is detected and the driver will turn off.

Eligible desaturation signals initiate the Soft Shutdown sequence (SSD). While in SSD, the output driver goes in high impedance and the SSD pull-down is activated to turn off the IGBT through SSDH/L pin. The SY_FLT output pin (active low, see figure 14) reports the IR2214 status all the way long SSD sequence lasts (t_{SS}). Once finished SSD, SYS_FLT releases, and IR2214 generates a FAULT signal (see the FAULT/SD section) by activating FAULT/SD pin. This generates a hard shut down for both high and low output stages (HO=LO=low). Each driver is latched low until the fault is cleared (see FLT_CLR).

Figure 14 shows the fault management circuit. In this diagram DesatHS and DesatLS are two internal signals that come from the output stages (see figure 13).

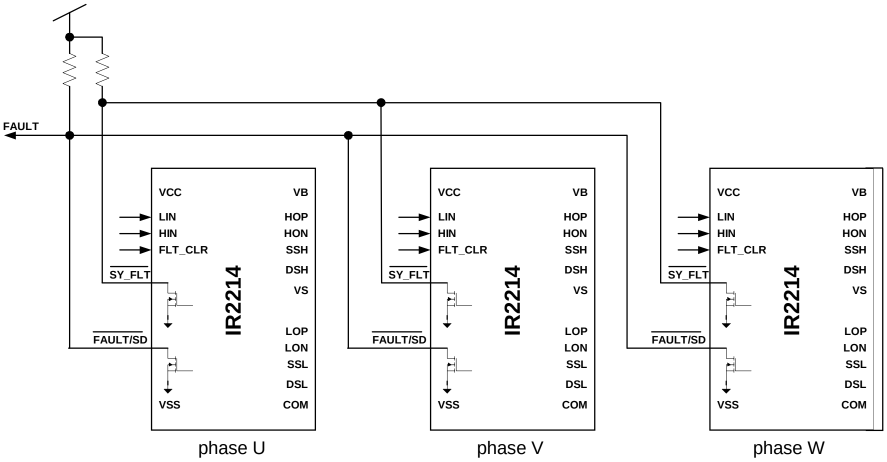


Figure 15: IR2214 application in 3ph system.

It must be noted that while in Soft Shut Down, both Under Voltage fault and external Shut Down (SD) are masked until the end of SSD. Desaturation protection is working independently by the other entire control pin and it is disabled only when the output status is off.

4.2.2 Fault management in multi-phase systems

In a system with two or more gate drivers the IR2214 devices must be connected as in figure 15.

SY_FLT.

The bi-directional SY_FLT pins communicate each other in the local network. The logic signal is active low.

The device that detects the IGBT desaturation activates the SY_FLT, which is then read by the other gate drivers. When SYS_FLT is active all the drivers hold their output state regardless the input signals (H_{IN}, L_{IN}) they receive from the controller (freeze state).

This feature is particularly important in phase-to-phase short circuit where two IGBTs are involved; in fact, while one is softly shutting-down, the other must be prevented from hard shutdown to avoid vanishing SSD.

In the Freeze state the frozen drivers are not completely inactive because desaturation detection still takes the highest priority.

SY_FLT communication has been designed for creating a local network between the drivers. There is no need to wire SY_FLT to the controller.

FAULT/SD

The bi-directional FAULT/SD pins communicates each other and with the system controller. The logic signal is active low.

When low, the FAULT/SD signal commands the outputs to go off by hard shutdown. There are three events that can force FAULT/SD low:

1. Desaturation detection event: the FAULT\SD pin is *latched* low when SSD is over, and only a FLT_CLR signal can reset it.

2. Undervoltage on V_{CC}: the FAULT\SD pin is forced low and held until the undervoltage is active (*not latched*).
3. FAULT/SD is externally driven low either from the controller or from another IR2214 device. This event is *not latched*; therefore the FLT_CLR cannot disable it. Only when FAULT/SD becomes high the device returns in normal operating mode.

5. Active bias

For the purpose of sensing the power transistor desaturation the collector voltage is read by an external HV diode. The diode is normally biased by an internal pull up resistor connected to the local supply line (V_B or V_{CC}). When the transistor is “on” the diode is conducting and the amount of current flowing in the circuit is determined by the internal pull up resistor value.

In the high side circuit, the desaturation biasing current may become relevant for dimensioning the bootstrap capacitor (see figure 19). In fact, too low pull up resistor value may result in high current discharging significantly the bootstrap capacitor. For that reason typical pull up resistor are in the range of 100 kΩ. This is the value of the internal pull up.

While the impedance of DSH/DSL pins is very low when the transistor is on (low impedance path through the external diode down to the power transistor), the impedance is only controlled by the pull up resistor when the transistor is off. In that case relevant dV/dt applied by the power transistor during the commutation at the output results in a considerable current injected through the stray capacitance of the diode into the desaturation detection pin (DSH/L). This coupled noise may be easily reduced using an active bias for the sensing diode.

An Active Bias structure is available only for IR22141 version for DSH/L pin. The DSH/L pins present an active pull-up respectively to VB/VCC, and a pull-down respectively to VS/COM.

The dedicated biasing circuit reduces the impedance on the DSH/L pin when the voltage exceeds the V_{DESAT} threshold (see figure 16). This low impedance helps in rejecting the noise providing the current inject by the parasitic capacitance. When the power transistor is fully on, the sensing diode gets forward biased and the voltage at the DSH/L pin decreases. At this point the biasing circuit deactivates, in order to reduce the bias current of the diode as shown in figure 16.

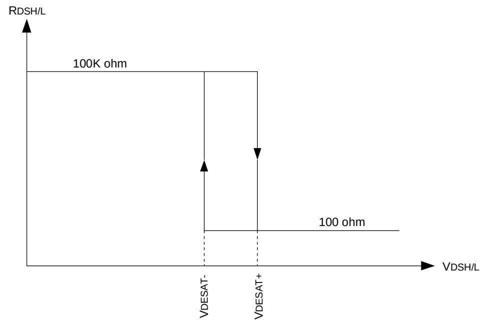


Figure 16: $R_{DSH/L}$ Active Biasing

6. Output stage

The structure is shown in figure 13 and consists of two turns on stages and one turn off stage.

When the driver turns on the IGBT (see figure 8), a first stage is constantly activated while an additional stage is maintained active only for a limited time (ton1). This feature boost the total driving capability in order to accommodate both fast gate charge to the plateau voltage and dV/dt control in switching.

At turn off, a single n-channel sinks up to 3A (I_{O-}) and offers a low impedance path to prevent the self-turn on due to the parasitic Miller capacitance in the power switch.

7. Timing and logic state diagrams description

The following figures show the input/output logic diagram.
Figure 17 shows the SY_FLT and FAULT/SD signals as output, whereas figure 18 shows them as input.

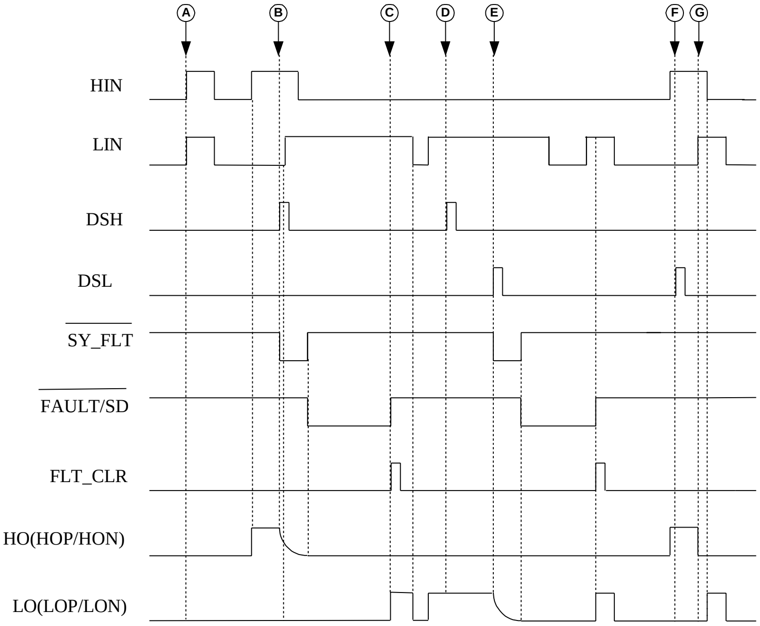


Figure 17: I/O timing diagram with SY_FLT and FAULT/SD as output

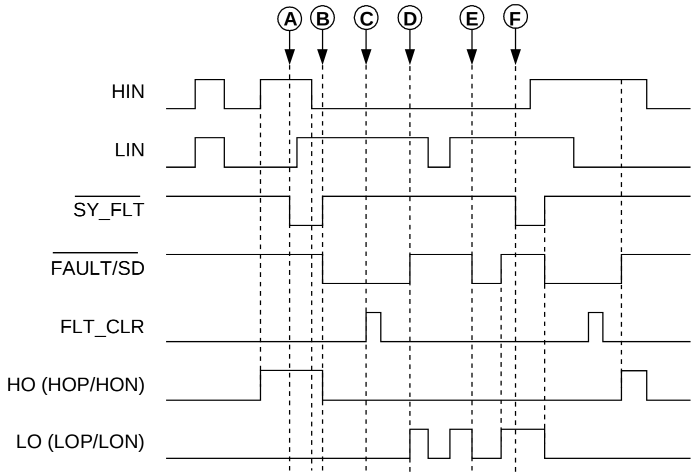


Figure 18: I/O logic diagram with SY_FLT and FAULT/SD as input

Referred to timing diagram of figure 17:

A. When the input signals are on together the outputs go off (anti-shoot through).

B. The HO signal is on and the high side IGBT desaturates, the HO turn off softly while the SY_FLT stays low. When SY_FLT goes high the FAULT/SD goes low. While in SSD, if LIN goes up, LO does not change (freeze).

C. When FAULT/SD is latched low (see FAULT/SD section) FLT_CLR can disable it and the outputs go back to follow the inputs.

D. The DSH goes high but this is not read because HO is off.

E. The LO signal is on and the low side IGBT desaturates, the low side behaviour is the same as described in point B.

F. The DSL goes high but this is not read because LO is off.

G. As point A (anti-shoot through).

Referred to logic diagram figure 18:

A. The device is in hold state, regardless of input variations. Hold state is forced by SY_FLT forced low externally

B. The device outputs goes off by hard shutdown, externally commanded. A through B is the same sequence adopted by another IR2214 device in SSD procedure.

C. Externally driven low FAULT/SD (shutdown state) cannot be disabled by forcing FLT_CLR (see FAULT/SD section).

D. The FAULT/SD is released and the outputs go back to follow the inputs.

E. Externally driven low FAULT/SD: outputs go off by hard shutdown (like point B).

F. As point A and B but for the low side output.

Sizing tips

Bootstrap supply

The V_{BS} voltage provides the supply to the high side driver circuitry of the IR2214. This supply sits on top of the V_S voltage and so it must be floating.
The bootstrap method to generate V_{BS} supply can be used with IR2214. The bootstrap supply is formed by a diode and a capacitor connected as in figure 19.

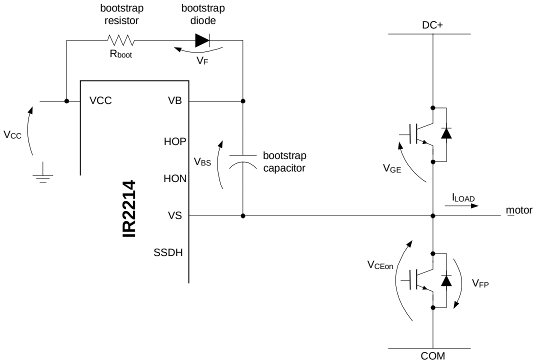


Figure 19: bootstrap supply schematic

This method has the advantage of being simple and low cost but may force some limitations on duty-cycle and on-time since they are limited by the requirement to refresh the charge in the bootstrap capacitor.
Proper capacitor choice can reduce drastically these limitations.

Bootstrap capacitor sizing

To size the bootstrap capacitor, the first step is to establish the minimum voltage drop (ΔV_{BS}) that we have to guarantee when the high side IGBT is on.

If V_{GEmin} is the minimum gate emitter voltage we want to maintain, the voltage drop must be:

$$\Delta V_{BS} \le V_{CC} - V_F - V_{GE\,\min} - V_{CEon}$$

under the condition:

$$V_{GE\,\min} > V_{BSUV-}$$

where V_{CC} is the IC voltage supply, V_F is bootstrap diode forward voltage, V_{CEon} is emitter-collector voltage of low side IGBT and V_{BSUV-} is the high-side supply undervoltage negative going threshold.

Now we must consider the influencing factors contributing V_{BS} to decrease:

- IGBT turn on required Gate charge (Q_G);
- IGBT gate-source leakage current (I_{LK_GE});
- Floating section quiescent current (I_{QBS});
- Floating section leakage current (I_{LK})
- Bootstrap diode leakage current (I_{LK_DIODE});
- Desat diode bias when on (I_{DS-})
- Charge required by the internal level shifters (Q_{LS}); typical 20nC
- Bootstrap capacitor leakage current (I_{LK_CAP});
- High side on time (T_{HON}).

I_{LK_CAP} is only relevant when using an electrolytic capacitor and can be ignored if other types of capacitors are used. It is strongly recommend using at least one low ESR ceramic capacitor (paralleling electrolytic and low ESR ceramic may result in an efficient solution).

Then we have:

$$Q_{TOT} = Q_G + Q_{LS} + (I_{LK\_GE} + I_{QBS} + \\ + I_{LK} + I_{LK\_DIODE} + I_{LK\_CAP} + I_{DS-}) \cdot T_{HON}$$

The minimum size of bootstrap capacitor is:

$$C_{BOOT\,\min} = \frac{Q_{TOT}}{\Delta V_{BS}}$$

An example follows:

a) using a 25A @ 125C IGBT (IRGP30B120KD):

- I_{QBS} = 800 µA (See Static Electrical Charact.);
- I_{LK} = 50 µA (See Static Electrical Charact.);
- Q_{LS} = 20 nC;
- Q_G = 160 nC (Datasheet IRGP30B120KD);
- I_{LK_GE} = 100 nA (Datasheet IRGP30B120KD);
- I_{LK_DIODE} = 100 µA (with reverse recovery time <100 ns);
- I_{LK_CAP} = 0 (neglected for ceramic capacitor);
- I_{DS-} = *150* µA (see Static Electrical Charact.);
- T_{HON} = 100 µs.

And:

- V_{CC} = 15 V
- V_F = 1 V
- $V_{CEonmax}$ = 3.1 V
- V_{GEmin} = 10.5 V

the maximum voltage drop ΔV_{BS} becomes

$$\Delta V_{BS} \le V_{CC} - V_F - V_{GE\min} - V_{CEon} =$$
$$= 15V - 1V - 10.5V - 3.1V = 0.4V$$

and the boodstrap capacitor is:

$$C_{BOOT} \ge \frac{290\ nC}{0.4\,V} = 725\ nF$$

NOTICE: Here above V_{CC} has been chosen to be 15V. Some IGBTs may require higher supply to work correctly with the bootstrap technique. Also Vcc variations must be accounted in the above formulas.

Some important considerations

a. Voltage ripple

There are three different cases making the bootstrap circuit gets conductive (see figure 19):

- I_{LOAD} < 0; the load current flows in the low side IGBT displaying relevant V_{CEon}

$$V_{BS} = V_{CC} - V_F - V_{CEon}$$

In this case we have the lowest value for V_{BS}. This represents the worst case for the bootstrap capacitor sizing. When the IGBT is turned off the Vs node is pushed up by the load current until the high side freewheeling diode get forwarded biased

- I_{LOAD} = 0; the IGBT is not loaded while being on and V_{CE} can be neglected

$$V_{BS} = V_{CC} - V_F$$

- I_{LOAD} > 0; the load current flows through the freewheeling diode

$$V_{BS} = V_{CC} - V_F + V_{FP}$$

In this case we have the highest value for V_{BS}. Turning on the high side IGBT, I_{LOAD} flows into it and V_S is pulled up.

To minimize the risk of undervoltage, bootstrap capacitor should be sized according to the I_{LOAD}<0 case.

b. Bootstrap Resistor

A resistor (R_{boot}) is placed in series with bootstrap diode (see figure 19) so to limit the current when the bootstrap capacitor is initially charged. We suggest not exceeding some Ohms (typically 5, maximum 10 Ohm) to avoid increasing the V_{BS} time-constant. The minimum on time for charging the bootstrap capacitor or for refreshing its charge must be verified against this time-constant.

c. Bootstrap Capacitor

For high T_{HON} designs where is used an electrolytic tank capacitor, its ESR must be considered. This parasitic resistance forms a voltage divider with R_{boot} generating a voltage step on V_{BS} at the first charge of bootstrap capacitor. The voltage step and the related speed (dV_{BS}/dt) should be limited. As a general rule, ESR should meet the following constraint:

$$\frac{ESR}{ESR + R_{BOOT}} \cdot V_{CC} \leq 3V$$

Parallel combination of small ceramic and large electrolytic capacitors is normally the best compromise, the first acting as fast charge thank for the gate charge only and limiting the dV_{BS}/dt by reducing the equivalent resistance while the second keeps the V_{BS} voltage drop inside the desired ΔV_{BS}.

d. Bootstrap Diode

The diode must have a BV> 1200V and a fast recovery time (trr < 100 ns) to minimize the amount of charge fed back from the bootstrap capacitor to V_{CC} supply

Gate resistances

The switching speed of the output transistor can be controlled by properly size the resistors controlling the turn-on and turn-off gate current. The following section provides some basic rules for sizing the resistors to obtain the desired switching time and speed by introducing the equivalent output resistance of the gate driver (R_{DRp} and R_{DRn}).

The examples always use IGBT power transistor. Figure 20 shows the nomenclature used in the following paragraphs. In addition, V_{ge}^* indicates the plateau voltage, Q_{gc} and Q_{ge} indicate the gate to collector and gate to emitter charge respectively.

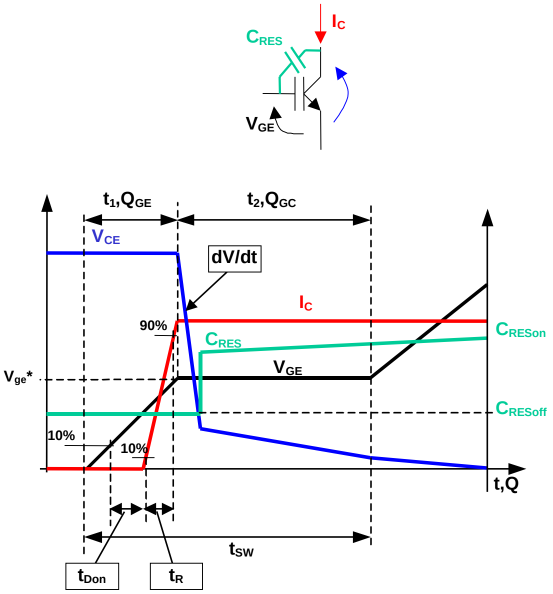


Figure 20: Nomenclature

Sizing the turn-on gate resistor

- Switching-time

For the matters of the calculation included hereafter, the switching time t_{sw} is defined as the time spent to reach the end of the plateau voltage (a total $Q_{gc}+Q_{ge}$ has been provided to the IGBT gate). To obtain the desired switching time the gate resistance can be sized starting from Q_{ge} and Q_{gc}, Vcc, V_{ge}^* (see figure 21):

$$I_{avg} = \frac{Q_{gc} + Q_{ge}}{t_{sw}}$$

and

$$R_{TOT} = \frac{Vcc - V_{ge}^*}{I_{avg}}$$

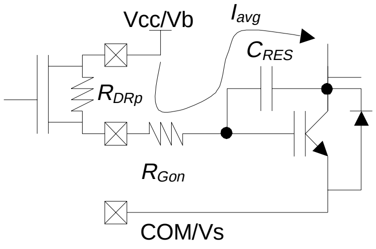


Figure 21: R_{Gon} sizing

where $R_{TOT} = R_{DRp} + R_{Gon}$

R_{Gon} = gate on-resistor
R_{DRp} = driver equivalent on-resistance

When R_{Gon} > 7 Ohm, R_{DRp} is defined by

$$R_{DRp} = \begin{cases} \dfrac{t_{on1}}{t_{SW}} \cdot \left[\dfrac{Vcc}{I_{o1+}} + \dfrac{Vcc}{I_{o2+}} \left(\dfrac{t_{SW}}{t_{on1}} - 1 \right) \right] & when\ t_{SW} > t_{on1} \\ \dfrac{Vcc}{I_{o1+}} & when\ t_{SW} \le t_{on1} \end{cases}$$

(I_{O1+}, I_{O2+} and t_{on1} from the IR2214 datasheet).

Table 1 reports the gate resistance size for two commonly used IGBTs (calculation made using typical datasheet values and assuming Vcc=15V).

- Output voltage slope

Turn-on gate resistor R_{Gon} can be sized to control output slope (dV_{OUT}/dt).
While the output voltage has a non-linear behaviour, the maximum output slope can be approximated by:

$$\frac{dV_{out}}{dt} = \frac{I_{avg}}{C_{RESoff}}$$

inserting the expression yielding I_{avg} and rearranging:

$$R_{TOT} = \frac{Vcc - V_{ge}^*}{C_{RESoff} \cdot \dfrac{dV_{out}}{dt}}$$

As an example, table 2 shows the sizing of gate resistance to get $dV_{out}/dt=5V/ns$ when using two popular IGBTs, typical datasheet values and assuming $Vcc=15V$.

NOTICE: Turn on time must be lower than T_{BL} to avoid improper desaturation detection and SSD triggering.

Sizing the turn-off gate resistor

The worst case in sizing the turn-off resistor R_{Goff} is when the collector of the IGBT in off state is forced to commutate by external events (i.e. the turn-on of the companion IGBT).
In this case the dV/dt of the output node induces a parasitic current through C_{RESoff} flowing in R_{Goff} and R_{DRn} (see figure 22).
If the voltage drop at the gate exceeds the threshold voltage of the IGBT, the device may self turn on causing large oscillation and relevant cross conduction.

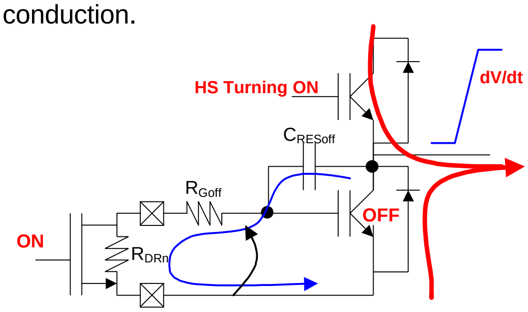


Figure 22: R_{Goff} sizing: current path when Low Side is off and High Side turns on

Translated into equations::

$$V_{th} \ge \left(R_{Goff} + R_{DRn}\right) \cdot I = \left(R_{Goff} + R_{DRn}\right) \cdot C_{RESoff} \frac{dV_{out}}{dt}$$

Rearranging the equation yields:

$$R_{Goff} \le \frac{V_{th}}{C_{RESoff} \cdot \frac{dV}{dt}} - R_{DRn}$$

When R_{Goff} > 4 Ohm, R_{DRn} is well defined by Vcc/I_{O-} (I_{O-} from IR2214 datasheet).
As an example, table 3 reports R_{Goff} for two popular IGBT to withstand $dV_{out}/dt = 5V/ns$.

NOTICE: the above-described equations are intended being an approximated way for the gate resistances sizing. More accurate sizing may account more precise device modelling and parasitic component dependent on the PCB and power section layout and related connections.

Table 1: t_{sw} driven R_{Gon} sizing

IGBT	Qge	Qgc	Vge*	tsw	Iavg	Rtot	RGon → std commercial value	Tsw
IRGP30B120K(D)	19nC	82nC	9V	400ns	0.25A	24Ω	RTOT - RDRp = 12.7 Ω → 10 Ω	→420ns
IRG4PH30K(D)	10nC	20nC	9V	200ns	0.15A	40Ω	RTOT - RDRp = 32.5 Ω → 33 Ω	→202ns

Table 2: dV_{OUT}/dt driven R_{Gon} sizing

IGBT	Qge	Qgc	Vge*	CRESoff	Rtot	RGon → std commercial value	dVout/dt
IRGP30B120K(D)	19nC	82nC	9V	85pF	14Ω	RTOT - RDRp = 6.5 Ω → 8.2 Ω	→4.5V/ns
IRG4PH30K(D)	10nc	20nC	9V	14pF	85Ω	RTOT - RDRp = 78 Ω → 82 Ω	→5V/ns

Table 3: R_{Goff} sizing

IGBT	Vth(min)	CRESoff	RGoff
IRGP30B120K(D)	4	85pF	RGoff ≤ 4 Ω
IRG4PH30K(D)	3	14pF	RGoff ≤ 35 Ω

PCB LAYOUT TIPS

Distance from H to L voltage:

The IR2214 pin out maximizes the distance between floating (from DC- to DC+) and low voltage pins. It's strongly recommended to place components tied to floating voltage in the high voltage side of device (V_B, V_S side) while the other components in the opposite side.

Ground plane:

Ground plane must not be placed under or nearby the high voltage floating side to minimize noise coupling.

Gate drive loops:

Current loops behave like an antenna able to receive and transmit EM noise. In order to reduce EM coupling and improve the power switch turn on/off performances, gate drive loops must be reduced as much as possible. Figure 23 shows the high and low side gate loops.

Moreover, current can be injected inside the gate drive loop via the IGBT collector-to-gate parasitic capacitance. The parasitic auto-inductance of the gate loop contributes to develop a voltage across the gate-emitter increasing the possibility of self turn-on effect. For this reason is strongly recommended to place the three gate resistances close together and to minimize the loop area (see figure 23).

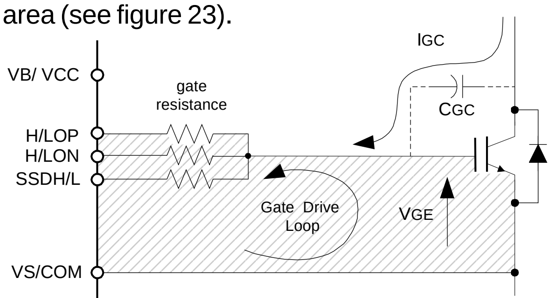


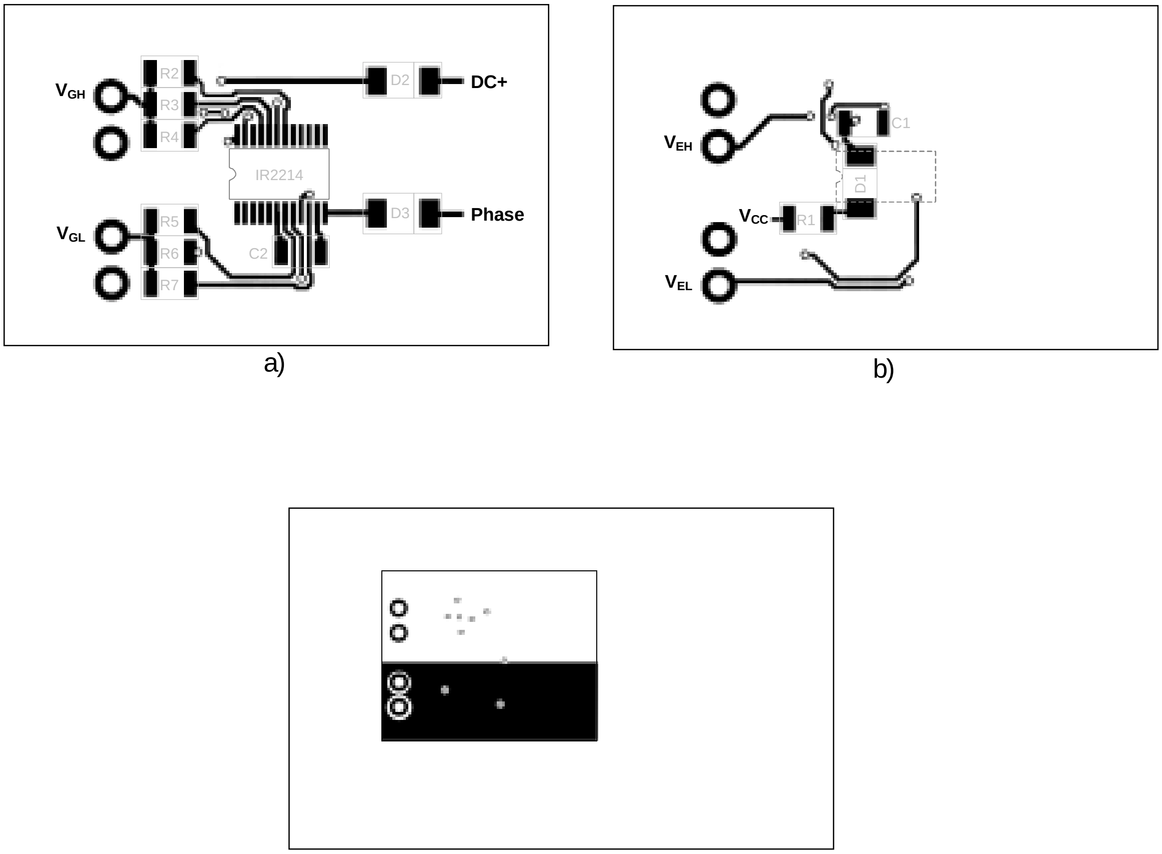
Figure 23: gate drive loop

Supply capacitors:

IR2214 output stages are able to quickly turn on IGBT with up to 2 A of output current. The supply capacitors must be placed as close as possible to the device pins (V_{CC} and V_{SS} for the ground tied supply, V_B and V_S for the floating supply) in order to minimize parasitic inductance/ resistance.

Routing and placement example:

Figure 24 shows one of the possible layout solutions using a 3 layer PCB. This example takes into account all the previous considerations. Placement and routing for supply capacitors and gate resistances in the high and low voltage side minimize respectively supply path and gate drive loop. The bootstrap diode is placed under the device to have the cathode as close as possible to bootstrap capacitor and the anode far from high voltage and close to V_{CC}.



a)

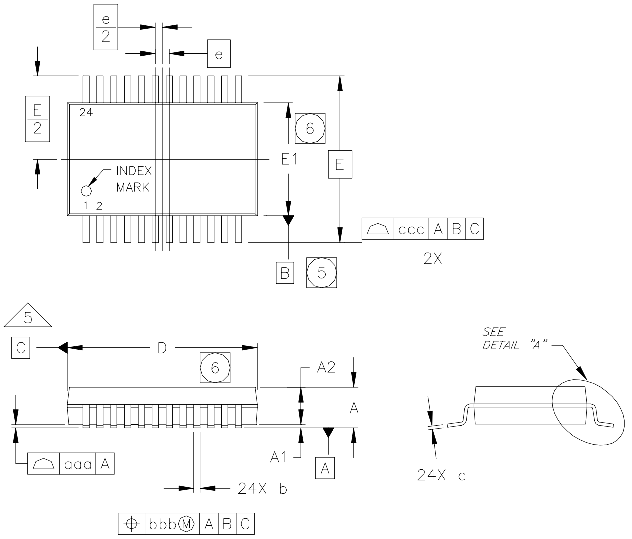
b)

c)

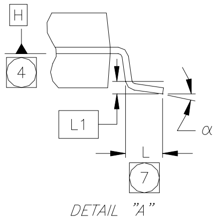
Figure 24: layout example: top (a), bottom (b) and ground plane (c) layer

Referred to figure 24:
Bootstrap section: R1, C1, D1
High side gate: R2, R3, R4
High side Desat: D2
Low side supply: C2
Low side gate: R5, R6, R7
Low side Desat: D3

Case outline

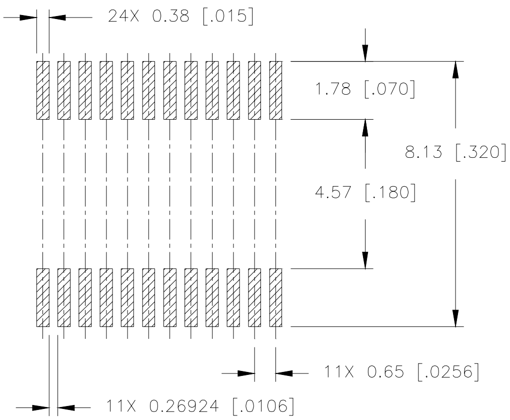


SYMBOL	DIMENSIONS					
	MILLIMETERS			INCHES		
	MO-150AH			*MO-150AH*		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.73	1.86	2.00	.068	.073	.078
A1	0.05	0.13	0.20	.002	.005	.008
A2	1.65	1.75	1.85	.065	.069	.073
b	0.22	0.30	0.38	.009	.012	.015
c	0.09	0.15	0.25	.004	.006	.010
D	7.90	8.20	8.50	.311	.323	.334
E	7.80 BSC			.307		
E1	5.00	5.30	5.60	.197	.209	.221
e	0.65 BSC			.026 BSC		
L	0.55	0.75	0.95	.022	.030	.037
L1	0.25 BSC			.010 BSC		
α	0°	4°	8°	0°	4°	8°
aaa	0.10			.004		
bbb	0.15			.006		
ccc	0.20			.008		



DETAIL "A"

MINIMUM RECOMMENDED FOOTPRINT



NOTES
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. DIMENSIONS ARE SHOWN IN MILLIMETERS AND INCHES.
3. CONTROLLING DIMENSION: MILLIMETER.

④ DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.

⑤ DATUM B AND C TO BE DETERMINED AT DATUM PLANE H.

⑥ DIMENSIONS D AND E1 ARE DETERMINED AT DATUM PLANE H.

⑦ L IS THE LEAD LENGTH FOR SOLDERING TO A SUBSTRATE.

8. OUTLINE CONFORMS TO JEDEC OUTLINE MO-150AH.

24-Lead SSOP

01 6076 01
01 5537 01 MO-150AH

International
IOR Rectifier

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Data and specifications subject to change without notice. 8/6/2003