Chapter Five

MINIMIZATION OF CONDUCTED EMI

The sizes of the energy storage elements (transformers, inductors, and capacitors) in a switch-mode power supply decrease approximately linearly with the increase of the switching frequency. Therefore, high-density power supplies generally demand high switching frequency and fast semiconductor devices. However, the increased switching frequency, together with the increased current and voltage slew rates, di/dt and dv/dt, have detrimental effects on the electromagnetic compatibility (EMC) performance of the power supplies. At the same time, EMI filters typically have degraded attenuation due to parasitic elements at high frequencies, and will be less effective in filtering out the high frequency electro-magnetic interference (EMI) noises generated from the power circuits. Commercial power supplies cannot be put on the market until certain EMC regulations are met. In recent years, both U.S. and Europe have imposed more stringent EMI regulation specifications on power supplies [D15, D16]. As a result, EMI has become a very important design aspect of the high-density power supplies.

In the past, EMC design remained a myth to the power electronics field. EMI practices usually take last-minute, trial-and-error experimental methods without careful planning and design. Furthermore, this last-minute patch-on solution sometimes cannot even meet the regulation requirement and calls for redesign of the entire converter, which inevitably delays the time to the market. Recently a number of attempts have been reported to address the theoretical analysis of EMI noises for power supplies, and to perform an early-phase EMI design. However, they are limited to specific, simplified converter switching cells and are difficult to apply to general complete power converters.

This chapter develops a systematic approach to the conducted EMC design aspect of high-density power supplies. Converter components are accurately modeled, with the parasitic elements extracted to reveal their impacts on the EMI noises. Circuit simulations are used to analyze and minimize the EMI noises. As an example, the same 36-W flyback adapter analyzed in Chapter 4 is used to demonstrate the design procedures of this approach.

5.1. Parasitic Parameter Extraction - Example: Flyback Adapter

Conducted EMI noises are generated from power supplies due to the switching actions of the semiconductor devices. Although the EMI regulation specifications target the total EMI emission, the noises can be divided into differential-mode and common-mode noises in order to more effectively minimize each noise for an overall emission suppression. Generally, the differential-mode noise is predominantly caused by the magnetic coupling $L \cdot di/dt$, where L is the

parasitic loop inductance which experiences high switching current slew rate di/dt. On the other hand, the common-mode noise is mainly related to the electrical coupling $C \cdot dv/dt$, where C is the parasitic common-mode capacitance which sees high voltage slew rate dv/dt. Therefore, it is essential to model the parasitic elements in the circuit accurately for the analysis of the EMI noises.

5.1.1. Layout Inductance Calculation

Conventionally, the parasitic inductance is extracted using finite-element-analysis (FEA) by solving the Maxwell's differential field equations. For a complex structure, this method requires extensive computation, and sometimes shows poor convergence. In addition, it requires the predetermination of the current loop for calculation. This presents a difficulty for power converters because current loops vary in different sub-topologies, which are determined by the switching combinations of semiconductor devices.

The partial element equivalent circuit (PEEC) method overcomes all the above obstacles [D17-D21]. The principles of this method are explained in detail in Appendix III. The PEEC method uses Maxwell's integral equations instead of differential equations, and calculates inductance analytically, based on the geometry information only, which only involves matrix manipulations. It also breaks the loop inductance into partial inductance associated with each trace, and relates these partial inductances with mutual inductances, so that the overall loop inductance can be easily computed for any arbitrary combination of traces. Therefore, it can be easily applied to nonlinear switching circuits.

A software package, *Inductance Calculation* (*InCa*), is developed based on the PEEC method and performs the partial inductance and resistance calculations [E11]. It is used to extract the parasitic parameters associated with the power-stage PCB layout of the flyback adapter, shown in Fig. 5.1. The calculated parasitic inductance, L_p, and the trace resistance, R_p, using PEEC method are expressed in the following matrix forms:

$$L_p = \begin{bmatrix} 45.9 & -4.6 & -3.4 & -1.3 & -0.4 & -0.4 & -2.6 & -0.3 & 1.0 \\ & 16.3 & 1.0 & 2.3 & 0.9 & 0.6 & 0.7 & 0.3 & -0.3 \\ & & 10.9 & 0 & 0 & 0 & 1.4 & 0 & -0.6 \\ & & & 20.0 & 2.4 & 3.6 & 0 & 0.9 & 0 \\ & & & & 5.8 & 0.7 & 0 & 0.2 & 0 \\ & & & & & 8.0 & 0 & 0.4 & 0 \\ & & & & & & 31.6 & 0 & -8.7 \\ & & & & & & & 5.1 & 0 \\ & & & & & & & & 10.2 \end{bmatrix} nH, \quad R_p = \begin{bmatrix} 22.4 \\ 10.2 \\ 6.2 \\ 6.2 \\ 3.9 \\ 5.0 \\ 8.9 \\ 2.0 \\ 3.7 \end{bmatrix} mW, \quad \text{(5-1)}$$

where the diagonal terms of the L_p matrix are the self inductances, and the off-diagonal terms are the mutual inductances.

An equivalent circuit of the parasitic elements is shown in Fig. 5.2, where all the parasitic inductors are shown in the light color. As can be clearly seen from Fig. 5.2, there is no predetermined loop parasitic inductance, and L_{p1}-L_{p9} form the loop inductance according to the switching topologies.

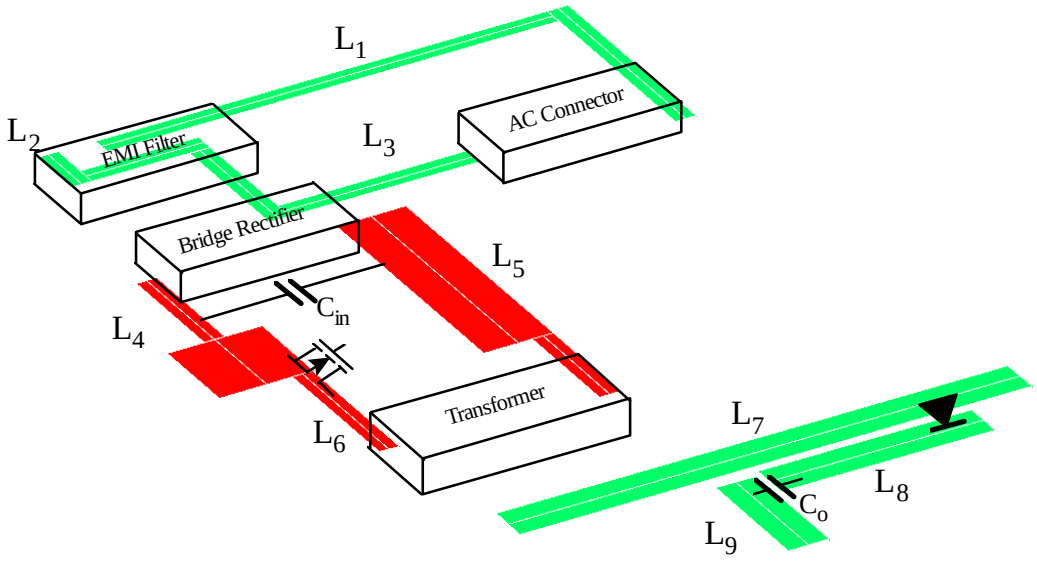


Figure 5.1. PCB layout of flyback converter (the ▬ traces are the crucial traces). The labeled inductances corresponds to the parasitic inductances shown in Fig. 5.2.

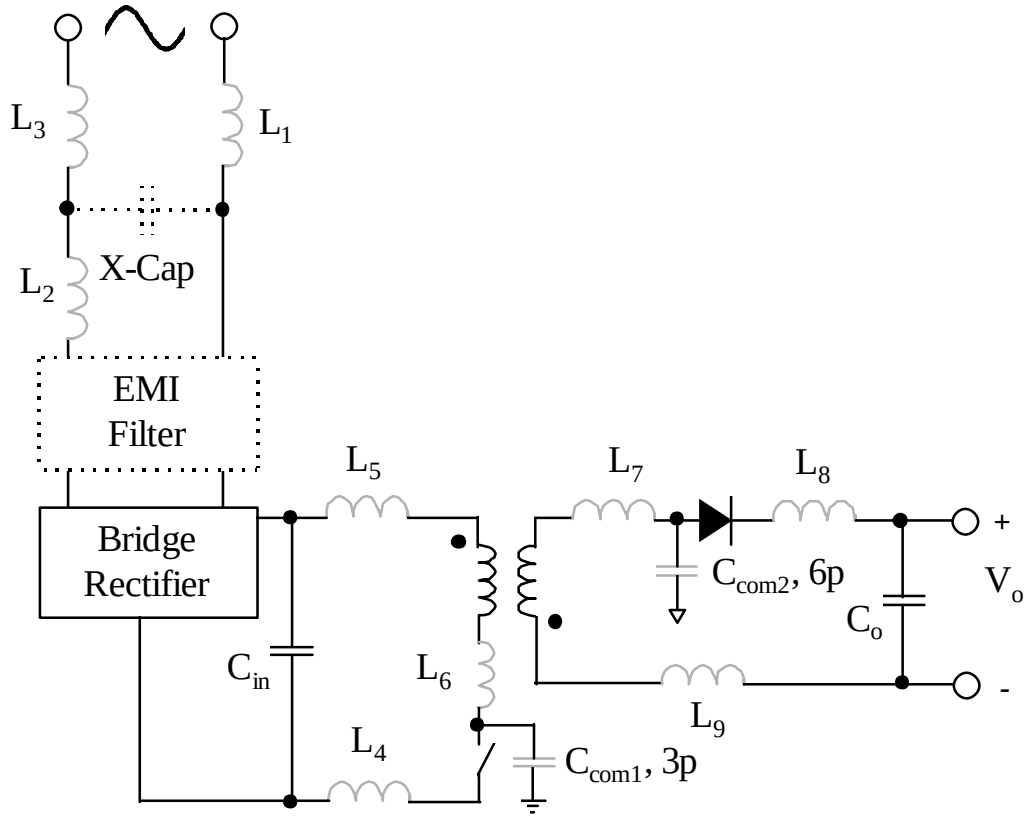


Figure 5.2. Equivalent circuit of parasitic elements in layout and packaging (shown in light color). Note: the mutual inductance and the parasitic trace resistance are not shown explicitly, and the dotted portion of the circuit is the EMI filter.

5.1.2. Packaging Capacitance Calculation

The common-mode capacitance, C_{com}, consists of the capacitances between the chassis ground and the electrical nodes which experience voltage changes ($dv/dt \neq 0$). In order to reduce the junction temperatures, the semiconductor devices are usually mounted on heatsinks, which are connected to chassis ground for safety. Therefore, C_{com} is mainly determined by semiconductor devices because of the relatively large parasitic common-mode capacitances between the heatsinks and the cases of the semiconductors, which are electrically connected either to the fast-switching MOSFET drains or to diode anodes.

To calculate the common-mode capacitance between the device case and the heatsink (which usually are separated only by a thin layer of isolation material), the analytical Wheeler/Schneider formula can be used (a modified parallel-plate formula), i.e.,

$$C = \frac{p e_o e_{eff}}{\ln\left[1+\frac{1}{2}\left(\frac{8h}{w_{eff}}\right)\left(\frac{8h}{w_{eff}}+\sqrt{\left(\frac{8h}{w_{eff}}\right)^2+p^2}\right)\right]}\cdot l\,;$$

$$e_{eff} = \frac{e-1}{2}+\frac{e-1}{2}\left(1+\frac{10h}{w}\right)^{-\frac{1}{2}};\quad w_{eff} = w+\frac{t}{p}\ln\frac{4e}{\sqrt{(\frac{t}{h})^2+[\frac{1}{p(\frac{w}{t}+1.1)}]^2}}\} \qquad (5\text{-}2)$$

where w, l, t are the width, length, and thickness of the case, respectively, h is the spacing between the case and the heatsink, and e is the dielectric constant [D22]. The parasitic common-mode capacitance associated with the primary switch and the secondary rectifier for the example adapter is calculated for the flyback converter packaging using Eq. (5-2), and shown in Fig. 5.2.

5.2. Circuit Modeling and EMI Analysis - Example: Flyback Adapter

In addition to the layout and packaging parasitics, to predict the EMI performance accurately, the high-frequency characteristics of the components in a converter need to be appropriately modeled so that the high frequency circuit behavior and the EMI coupling mechanism can be correctly determined.

5.2.1. Power Transformer Modeling

Other than the power switches (their models are usually available from semiconductor manufacturers, and are beyond the scope of this work), which generate the high-frequency di/dt and dv/dt slew rates, the power transformer is the most critical and complex component in terms of the EMI performance of the isolated power converters.

For an accurate analysis, FEA is usually used to determine the electromagnetic characteristics of a transformer, which requires extensive utilization of electromagnetic field analysis and simulation time. In addition, the results are difficult to apply directly to EMI analysis. In contrast, the two-winding transformer method models the high-frequency characteristics of a transformer using equivalent circuit based on transformer impedance measurement [D23]. The transformer open-circuit impedance, Z_o, and short-circuit impedance, Z_{sc}, are measured, and consequently can be used to characterize the transformer behavior using a corresponding equivalent circuit.

The power transformer used in the flyback adapter is modeled using this method. Figure 5.3 shows the derived equivalent circuit of the power transformer. The magnetizing and leakage inductances, winding capacitances, winding resistances, and core loss resistances are modeled. The measured and simulated open-circuit impedances, Z_o, and short-circuit impedances, Z_{sc}, are compared and shown in Figs. 5.4(b) and 5.4(c). It can be seen that the modeled impedance characteristics (on the right) agree very well with the measurements (on the left). It should be noted that in the short-circuit measurement, where only the leakage inductance of the transformer is present, lead inductance introduced by the test setup and the equipment causes artificial high frequency resonances at 20 MHz and 30 MHz. The equivalent circuit in Fig. 5.3 predicts a capacitive 20 dB/dec rolloff after the leakage inductance and the winding capacitance resonance around 10 MHz. Therefore, the impedance model shown in Fig. 5.4(b) is modified to account for the effects of the introduced lead inductance in the measurement. However, this artificial resonance is not present in the actual converter.

5.2.2. Modeling of LISN

The conducted EMI measurement procedure requires a 50 Ω/ 50 μH line impedance stabilization network (LISN) to be inserted between the equipment under test (EUT) and the ac utility line to provide a specified measuring impedance for noise voltage measurement, and to isolate the EUT and the measuring equipment from the utility at radio frequencies. A circuit model of the LISN, which is required in the EMI simulation, is shown in Fig. 5.5. The simulated and measured conducted EMI noise voltages are taken across the 50-Ω resistor, and compared with experimental measurements.

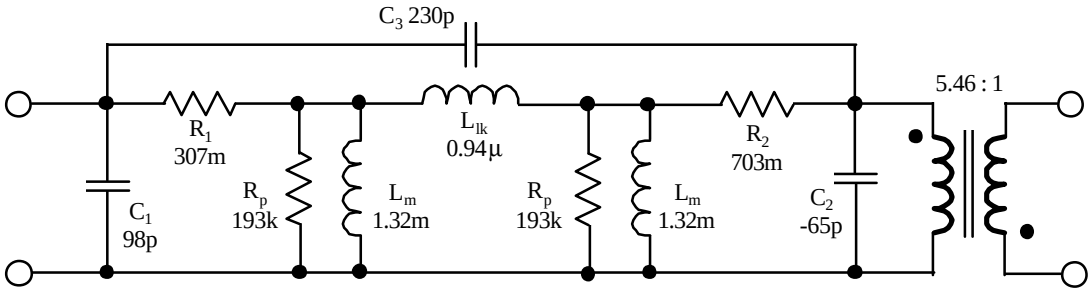
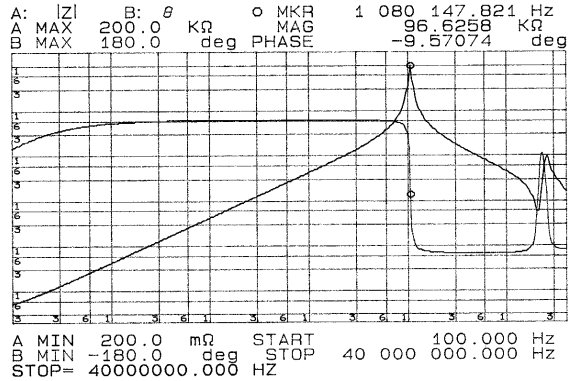
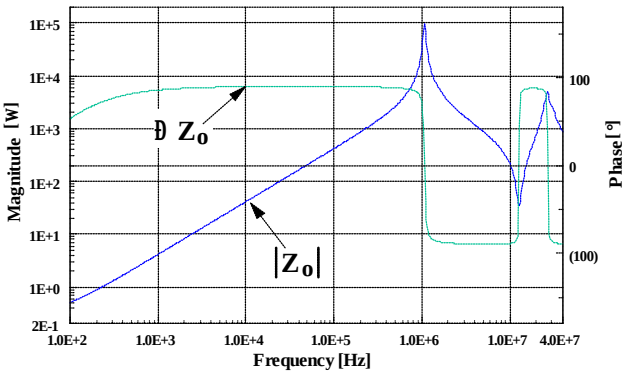


Figure 5.3. Reduced equivalent circuit of power transformer: L_m: magnetizing inductance; L_{lk}: leakage inductance; C_1-C_3: winding capacitances; R_1, R_2: winding resistances; R_p: core-loss resistance.
Note that C_2 is negative due to the energy balance. However, all the measurable capacitances, formed by the combinations of C_1-C_3, are positive.

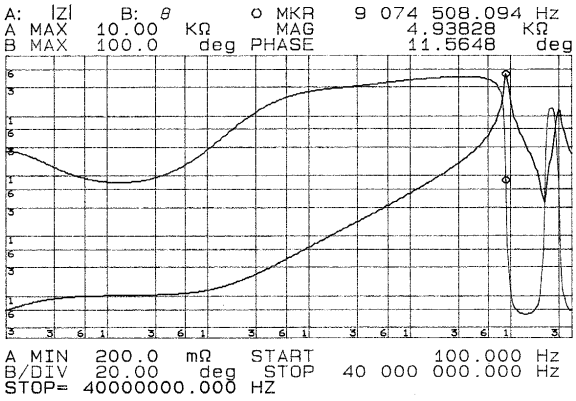
Measurement

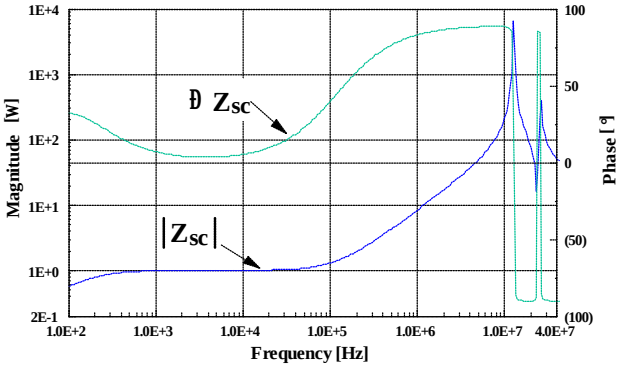


Model



(a)





(b)

Figure 5.4. Comparison of power transformer impedance measurement and modeling: (a) open-circuit Z_o; (b) short-circuit Z_{sc}.

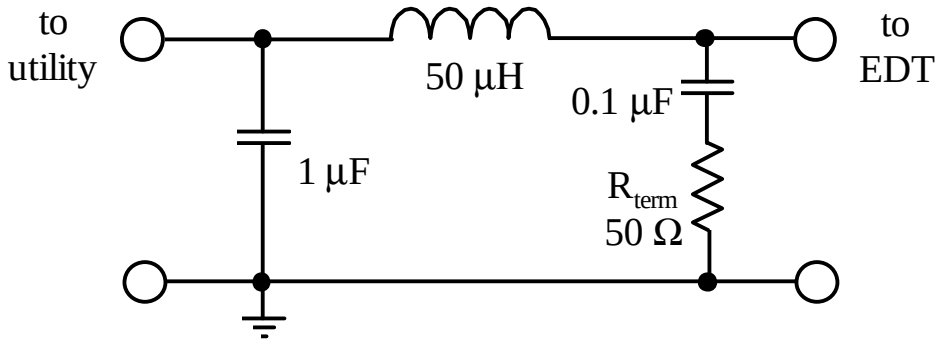


Figure 5.5. Circuit diagram of LISN.

5.2.3. EMI Analysis

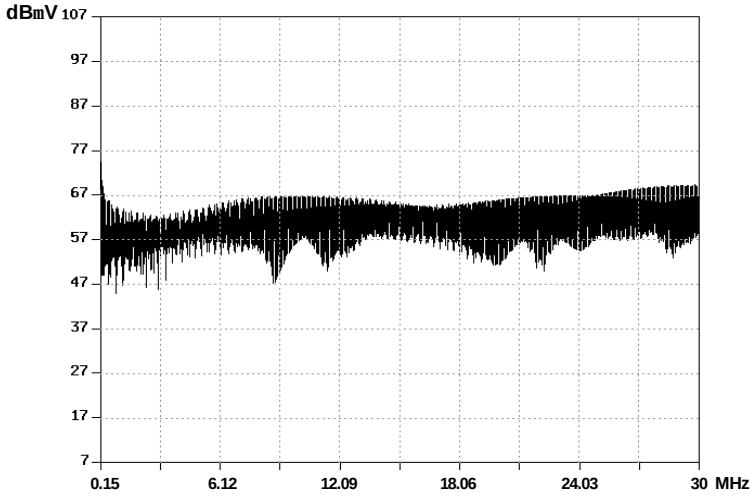
Taking the circuit models shown in Figs. 5.2, 5.3, and 5.5, a complete circuit model can be formed. Using an electrical circuit simulator, e.g., Saber, the conducted EMI performance of the studied power supply can be examined. Figure 5.6 shows the simulated EMI noises for the flyback adapter at high line input voltage (265 Vac). The conducted EMI noises can be divided into common-mode and differential-mode noises, by performing the following calculation:

$$\begin{cases} V_{com} = \dfrac{V_{R_{term1}} + V_{R_{term2}}}{2}, \\ V_{diff} = \dfrac{V_{R_{term1}} - V_{R_{term2}}}{2} \end{cases} \tag{5-3}$$

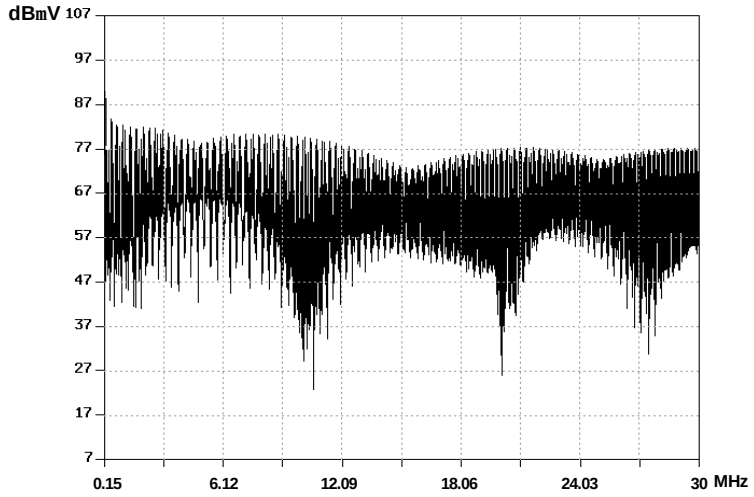
where V_{Rterm1} and V_{Rterm2} are the noise voltages across the termination resistors in Fig. 5.5, respectively. As can be seen 5.6, the conducted EMI noise in this particular adapter is common-mode-dominant. Namely, the common-mode noise is about 10 dB higher than the differential-mode noise throughout the regulation frequency band (150 kHz - 30 MHz). Figure 5.6(c) plots the total conducted EMI noise, which is the sum of common-mode and differential-mode noises:

$$V_{total} = V_{com} + V_{diff} \,. \tag{5-4}$$

Figure 5.6(c) also shows the FCC Class-B conducted emission limit. It is clear that the emission from the flyback adapter does not meet the regulatory requirement.



(a)



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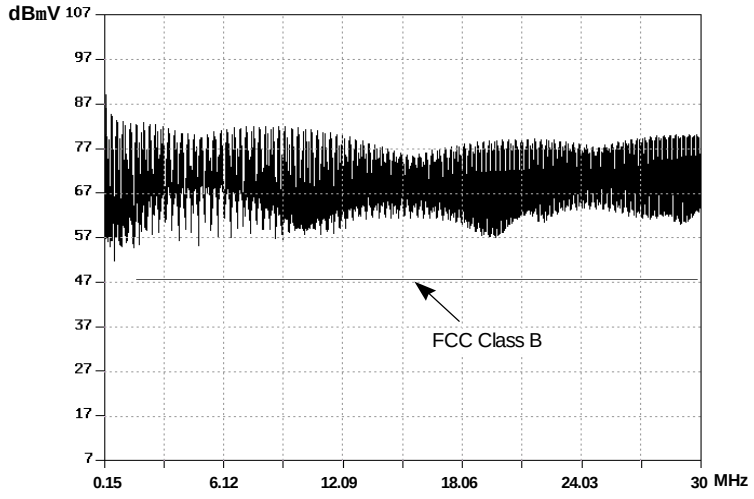


(c)

Figure 5.6. Simulated conducted EMI noises at V_{in} = 265 Vac: (a) differential-mode noise; (b) common-mode noise; (b) total noise.

5.3. EMI Noise Suppression - Example: Flyback Adapter

The methods of reducing the conducted EMI noises in a switching converter can involve either suppressing generated EMI noise sources by careful layout planning and packaging designs, or attenuating the generated noises by using EMI filters. The first approach focuses on reducing the inherent noise within the converter. The attenuation approach is widely used because it does not require modification of power converter design, and EMI filters can be external add-on modules. Using the filter attenuation alone to meet the EMI regulation, filter size may become a hurdle to achieving high power density. Therefore, for high-density power supplies, EMI filter should be designed based on an optimized layout and packaging of the converter, to minimize the size and the weight of the EMI filter.

5.3.1. Layout Improvement

As can be seen from the equivalent circuit of the flyback adapter (Fig. 5.2), the fast-switching currents exist in the primary loop (L_4 - L_5 - L_6) and the secondary loop (L_7 - L_8 - L_9). Figure 5.1 shows that the secondary loop area is already minimized, while the primary loop (traces shown in the dark color) has relatively large loop area. Therefore, an improved circuit layout can be designed by reducing the primary loop area, as shown in Fig. 5.7, so that its loop inductance is reduced, and the $L \cdot di/dt$ effect consequently decreases. Furthermore, a ground-referenced metal layer for radiated EMI shielding is added, which acts as a ground plane and effectively reducing the parasitic inductance to L_p', as

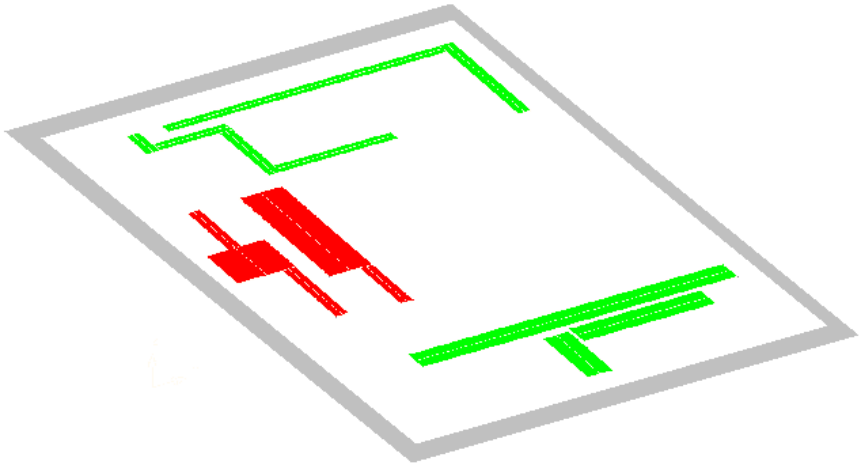


Figure 5.7. Improved PCB layout of flyback converter (the traces are the improved traces and the layer is the EMI shielding acting as a ground plane).

$$L_p' = \begin{bmatrix} 32.7 & -1.5 & -0.4 & 0 & 0 & 0 & 0 & 0 & 0 \\ & 13.0 & 0.1 & 0.3 & 0.1 & 0 & 0 & 0 & 0 \\ & & 8.6 & 0 & 0 & 0 & 0 & 0 & 0 \\ & & & 13.0 & 0.6 & 1.1 & 0 & 0 & 0 \\ & & & & 4.9 & 0 & 0 & 0 & 0 \\ & & & & & 6.5 & 0 & 0 & 0 \\ & & & & & & 19.5 & 0 & -3.6 \\ & & & & & & & 4.0 & 0 \\ & & & & & & & & 7.4 \end{bmatrix} nH, \quad R_p' = \begin{bmatrix} 22.4 \\ 10.2 \\ 6.2 \\ 6.2 \\ 3.9 \\ 5.0 \\ 8.9 \\ 2.0 \\ 3.7 \end{bmatrix} mW. \qquad (5\text{-}5)$$

Compared with the matrices shown in Eq. (5-1), not only the self-inductances (the diagonal terms) are reduced, but so are the mutual-inductances (off-diagonal terms). Therefore, the mutual coupling between traces is much reduced. Since differential-mode noise is directly related to $L \cdot di/dt$, it should consequently be reduced with this improved layout and packaging implementation.

Figures 5.8(a) - 5.8(c) show the simulated EMI noises with the improved layout and packaging. As can be seen from the comparison with the noises in Fig. 5.6, the differential noise is reduced by approximately 10 dB, especially for the high frequency region, while the common-mode and total noises remain approximately the same. Although the adapter is common-mode dominant, the differential-mode noise reduction alleviates the requirement for differential-mode attenuation and can reduce the EMI filter size to increase the adapter power-density. In some situations, minimized differential-mode noise can lead to EMI filter designs that utilize the leakage inductance of common-mode filters for differential-mode attenuation. Therefore, the improved layout and packaging design has a better EMI performance. However, the total EMI noise shown in Fig. 5.8(c) still exceeds the Class-B regulation limit, and further measures need to be taken to satisfy the regulatory specification.

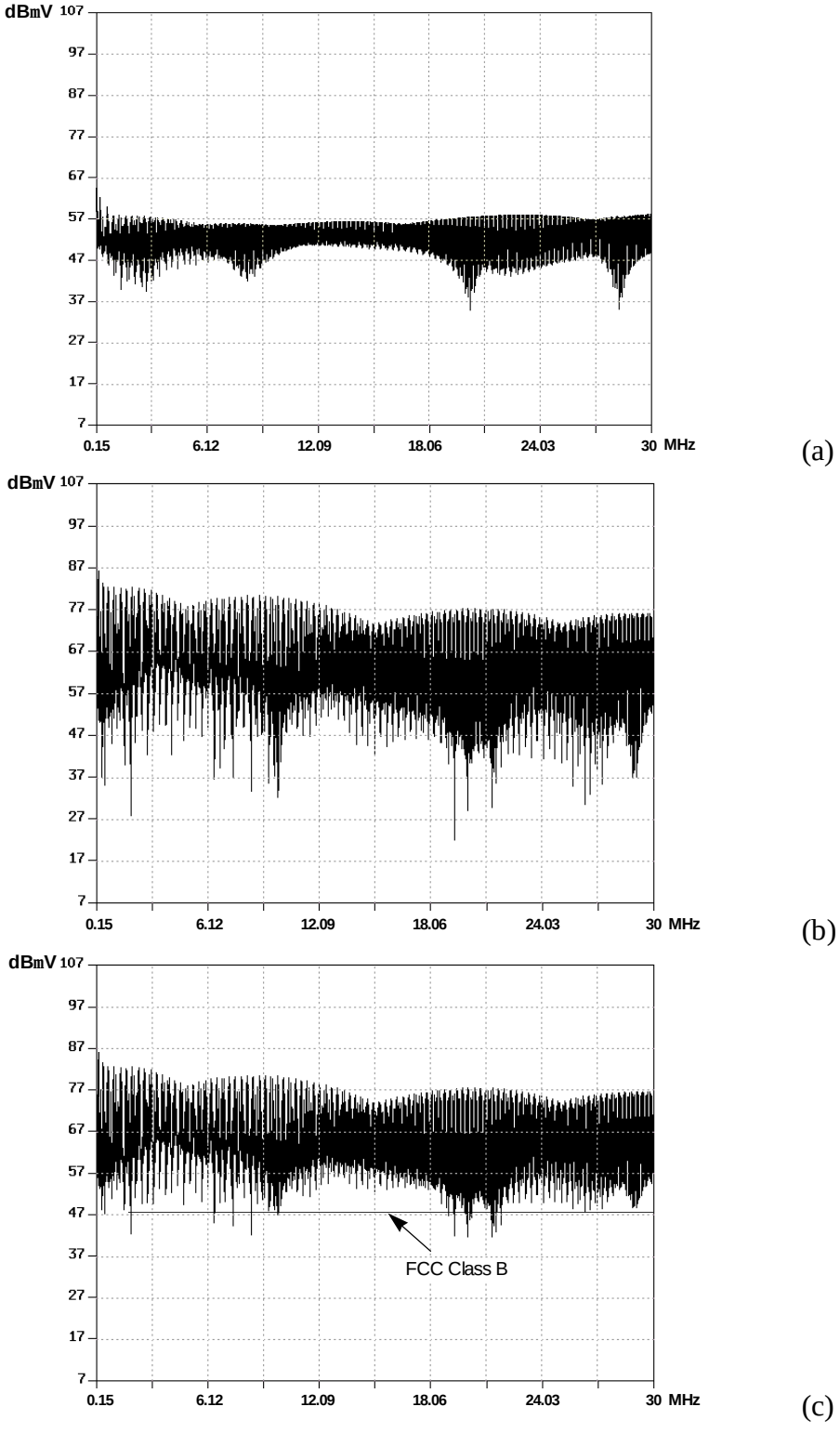
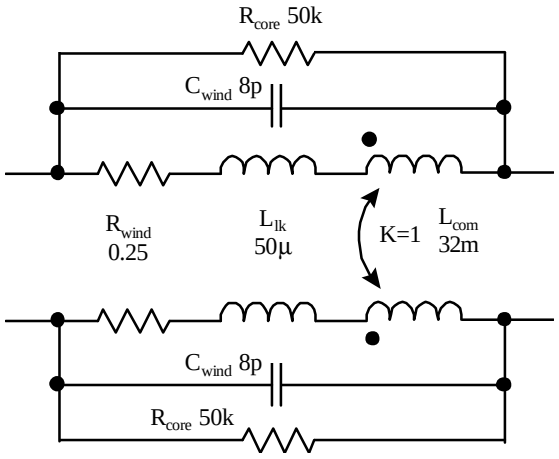


Figure 5.8. Simulated conducted EMI noises for improved layout and packaging at V_{in} = 265 Vac: (a) differential-mode noise; (b) common-mode noise; (b) total noise.

5.3.2. Input Filter Design

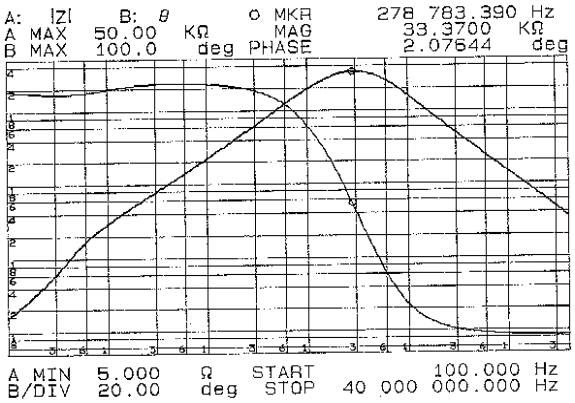
With the minimized conducted EMI emission from the converter by proper layout and packaging, an EMI filter can be designed to further attenuate the generated EMI noises seen from the utility lines. EMI filters can be categorized into common-mode filters and differential-mode filters, addressing different filter requirements [D24].

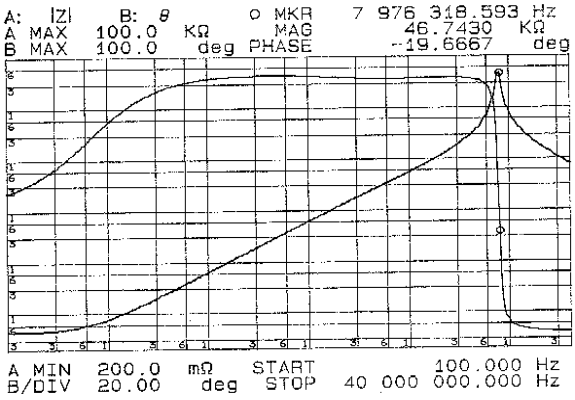
As can be seen from Fig. 5.5, 40-dB attenuation for the common-mode noise and 20-dB attenuation for the differential-mode noise are required to bring the noise levels under the emission limit. With 3.3-nF safety-required Y-caps, a 32-mH common-mode inductor will provide the required 40-dB attenuation (design procedures detailed in [D24]). With the minimized differential-mode noise, the leakage inductance (50 μH) of the wounded common-mode choke would have sufficient differential-mode attenuation. Figure 5.9 shows the equivalent circuit of the common-mode inductor (L_1), together with the measured and simulated characteristics. As can be seen from Fig. 5.9, the significant parasitic winding capacitance (8 pF) in L_1 due to a large number of turns reduces the attenuation effectiveness at high frequency (> 300 kHz), i.e., the inductor becomes capacitive above 300 kHz. To remedy the problem, an additional small common-mode inductor (L_2), which has very few turns and negligible winding capacitance and leakage inductance, can be connected in series with the first large inductor to provide the required high frequency attenuation. The equivalent circuit and the characteristics of L_2 are shown in Fig. 5.10, where the inductive behavior is kept throughout the conducted EMC regulatory frequency range (150 kHz - 30 MHz). Figure 5.11 shows the overall common-mode and differential-mode attenuation of the designed EMI filter. As can be seen from Fig. 5.11, with the high-frequency attenuation compensation from L_2, the required attenuation is achieved.



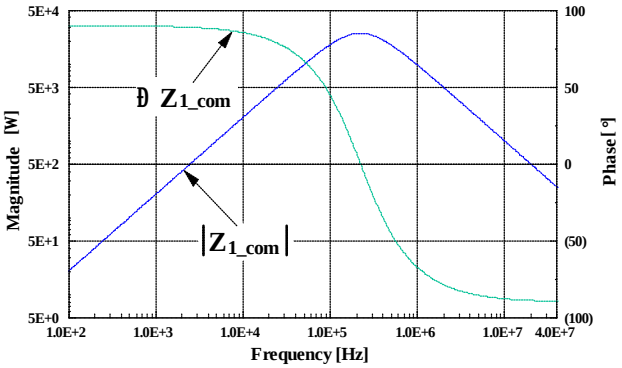
(a)

Measurement

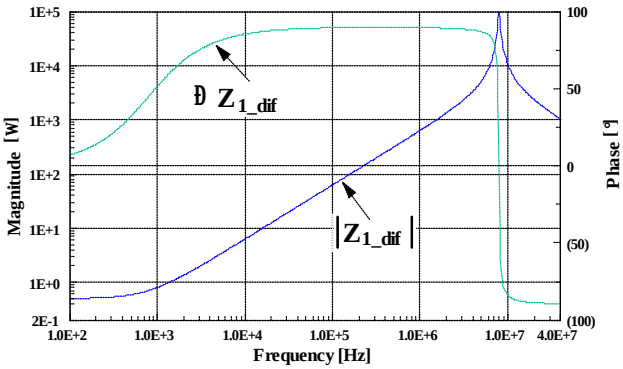




Model

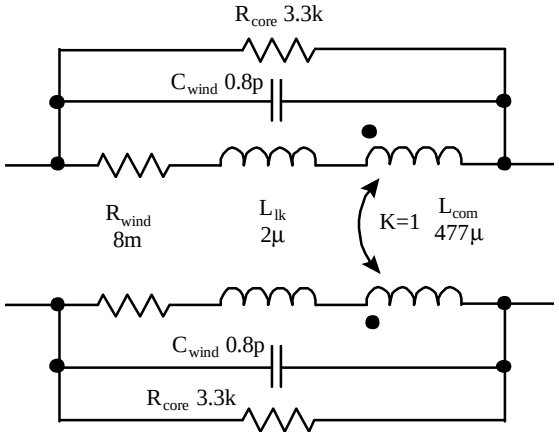


(b)



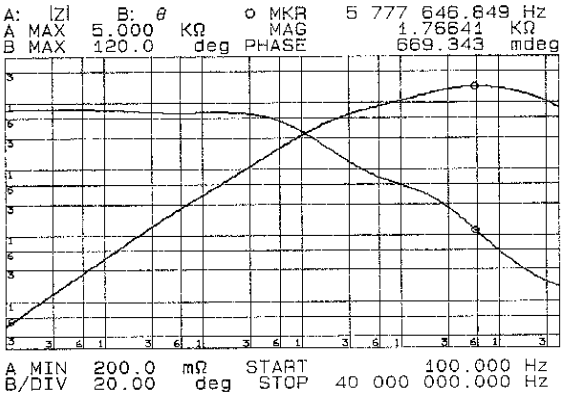
(c)

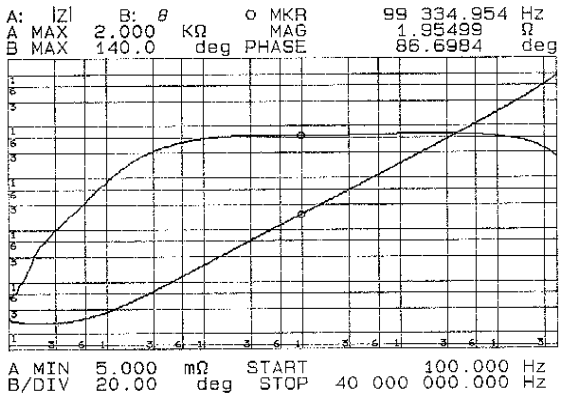
Figure 5.9. Comparison of common-mode choke (L_1) impedance measurement and modeling: (a) equivalent circuit; (b) common-mode Z_{com}; (c) differential-mode Z_{dif}.



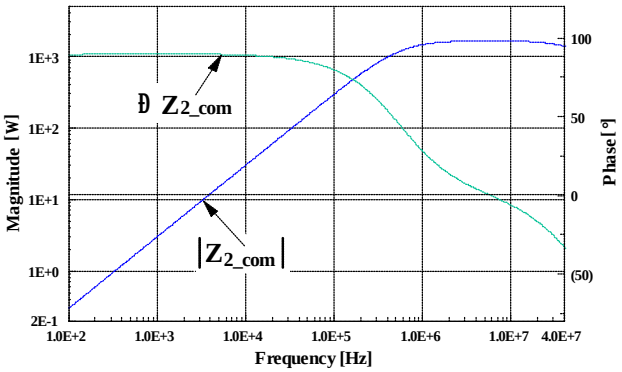
(a)

Measurement

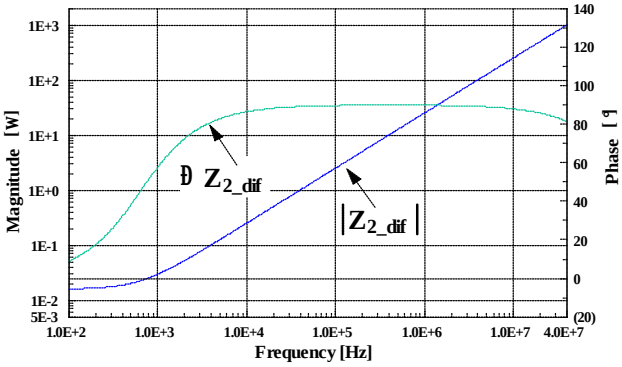




Model

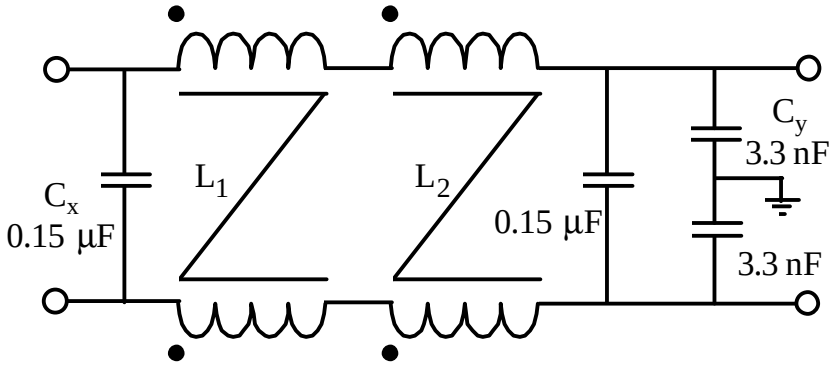


(b)

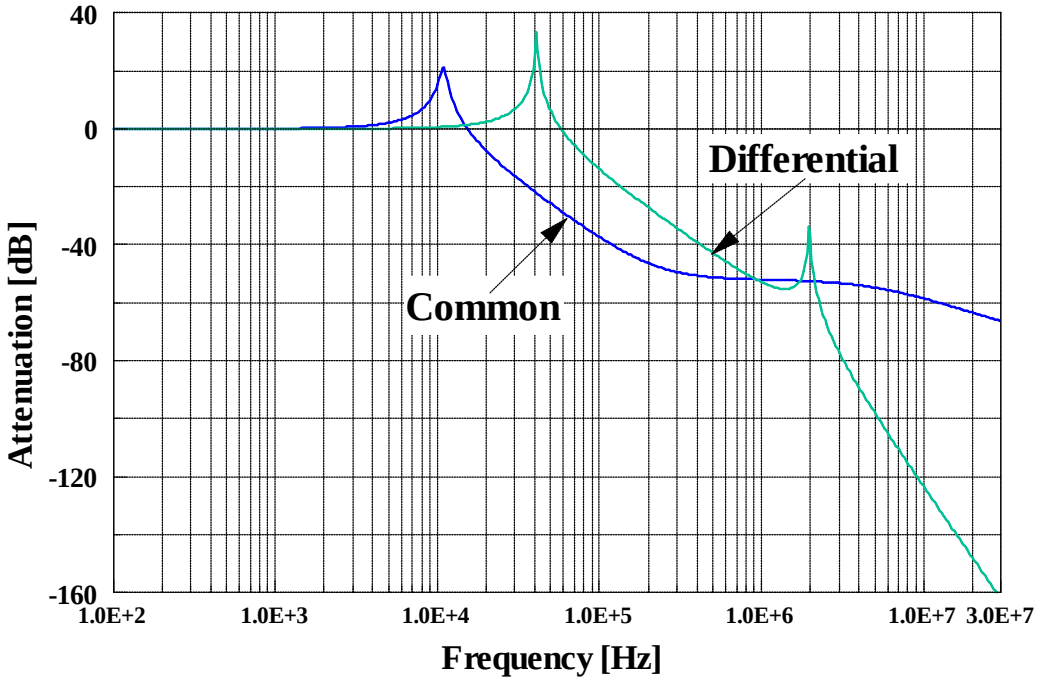


(c)

Figure 5.10. Comparison of common-mode choke (L_2) impedance measurement and modeling: (a) equivalent circuit; (b) common-mode Z_{com}; (c) differential-mode Z_{dif}.



(a)



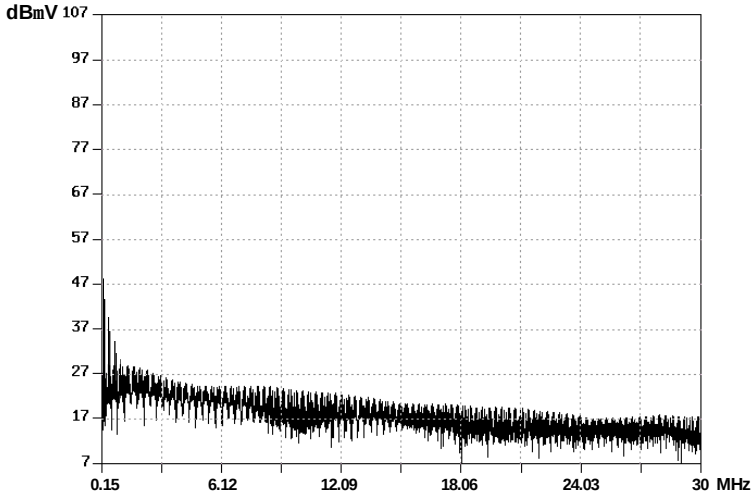
(b)

Figure 5.11. Attenuation of designed EMI filter: (a) EMI filter topology; (b) attenuation of filter shown in (a). Note that the equivalent circuits and the characteristics of the common-mode inductors L_1 and L_2 are shown in Figs. 5.9 and 5.10

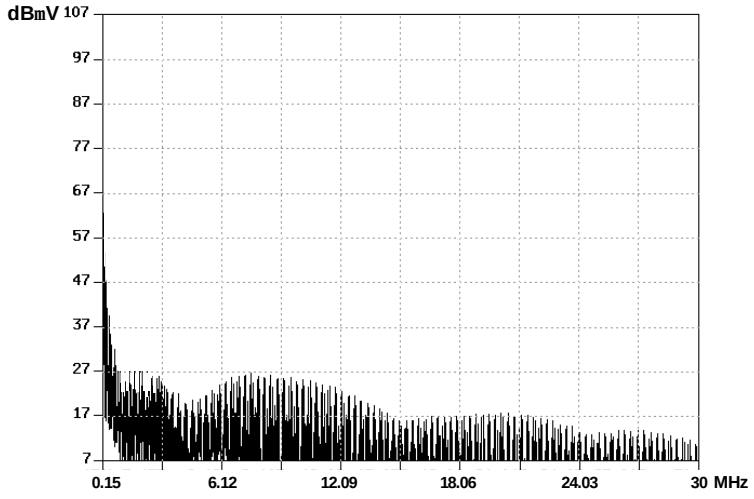
5.4. Performance Evaluation and Experimental Verification - Example: Flyback Adapter

The EMI performance of the flyback converter with the designed EMI filters can be simulated by inserting the filter between the LISN and the converter, as shown by the dashed line in Fig. 5.2. The simulated differential-mode, common-mode, and total noises at V_{in} = 265 Vac are shown in Fig. 5.12. Compared with the EU, FCC, and VDE Class-B emission limits, the total EMI noises of the flyback converter with the designed EMI filter meet the regulation requirements.

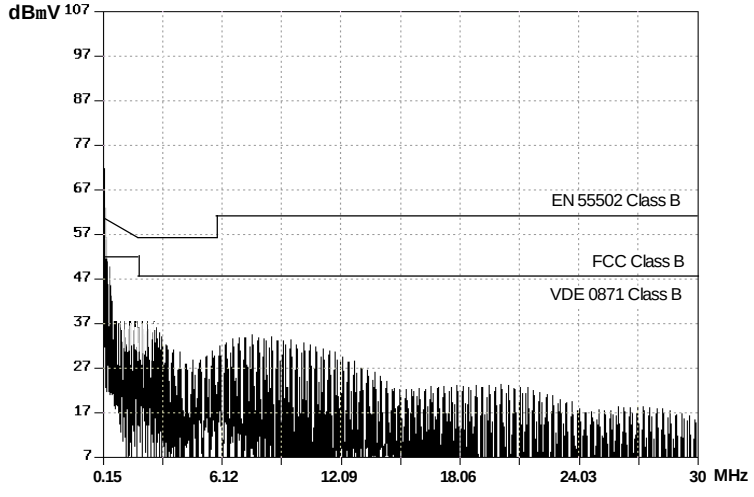
The modeling and prediction of the conducted EMI noises can serve as a fast design tool to optimize the EMC performance of high-density power supplies. However, the accuracy of the EMI models needs to be experimentally verified, especially for the final design. In addition, compliance with the EMI regulation can only be verified with experimental measurements. Figure 5.13 shows the oscillograms of measured differential-mode, common-mode, and total EMI emissions of the flyback adapter at V_{in} = 265 Vac. The separation of the EMI noises into common mode and differential mode is achieved with the help of noise separators (LISN Mate and LISN Mark). Compared with the superimposed envelopes of the simulated waveforms, it can be seen that predictions agree with the measurements very well in terms of peak dB values and the shapes of the waveforms of differential-mode, common-mode, and total noises.



(a)

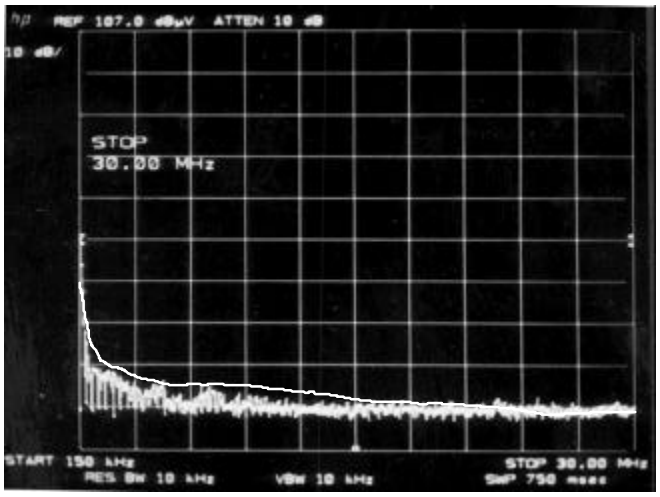


(b)

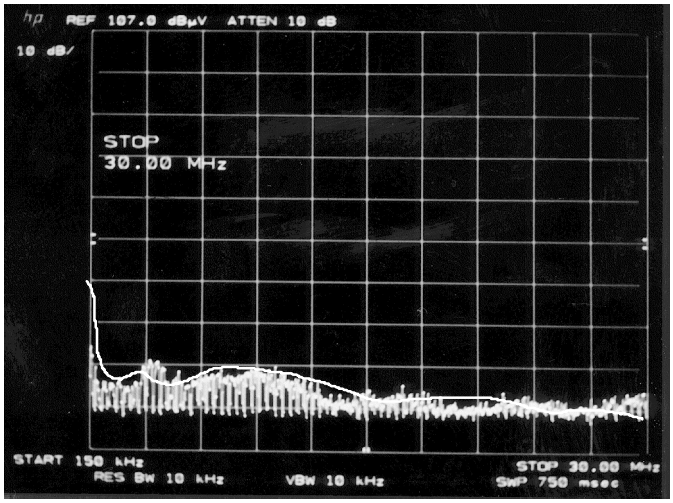


(c)

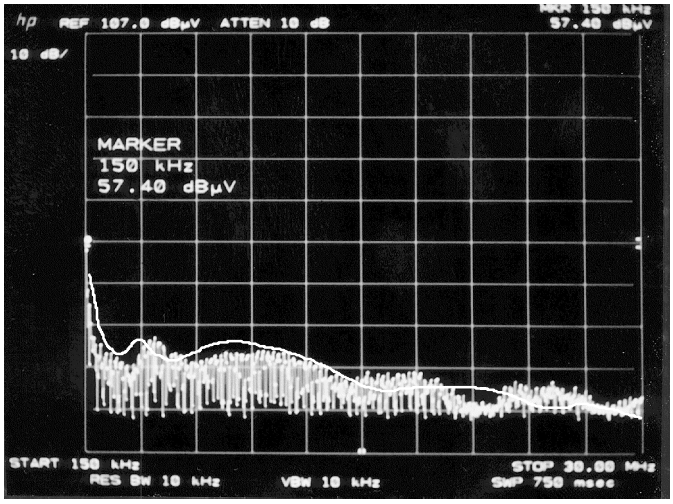
Figure 5.12. Simulated conducted EMI noises at V_{in} = 265 Vac: (a) differential-mode noise; (b) common-mode noise; (b) total noise.



(a)



(b)



(c)

Figure 5.13. Measured conducted EMI noises at V_{in} = 265 Vac: (a) differential-mode; (b) common-mode; (c) total.

5.5. Summary

This chapter has developed a systematic approach to the analysis of conducted electromagnetic compatibility for switch-mode power supplies. The procedure is diagrammed in Fig. 5.14, which shows the steps for a complete EMI analysis and design: parameter extraction, component modeling, performance simulation and analysis, filter design, and experimental verification. The iterative design loops in this approach are used to achieve an optimized EMC design. As an example, a flyback adapter is used to demonstrate the EMI prediction obtained by this approach. The accuracy of the theoretical results was experimentally verified.

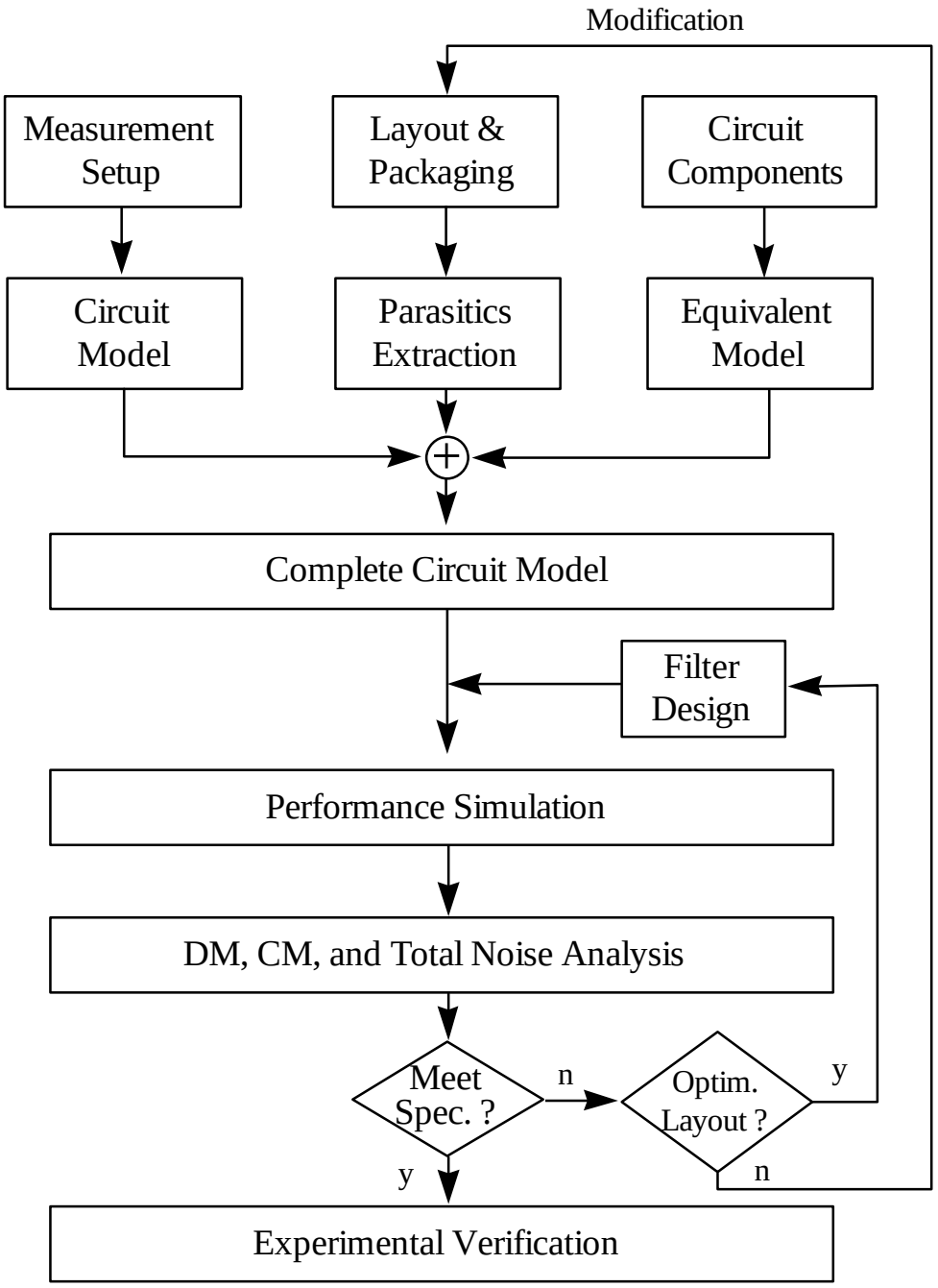


Figure 5.14. Flow chart of conducted EMI analysis.