TOSHIBA

Avalanche
Withstand Capability

PRODUCT GUIDE

Avalanche Withstand Capability

Power MOSFETs are used as high-speed switching devices in applications such as switching power supplies and DC-DC converters, where they contribute to miniaturization and lighter weight. The higher the operating frequency, the greater the tendency for a surge voltage with a narrow pulse profile to occur on turn-off as a result of stray inductance or inductance in the circuit itself. To absorb this surge voltage, the MOSFET needs to have a high breakdown resistance (avalanche withstand capability).

When high-speed switching is performed on the inductance load (L) of a transformer or other sources, the application of overvoltage exceeding the rated voltage activates the MOSFET's internal parasitic bipolar transistor. (This overvoltage arises from the reverse voltage generated by the inductance load (L).) As a result, current is concentrated in the cells and the MOSFET is destroyed. This is referred to as "avalanche breakdown".

Toshiba have developed a device which features improved avalanche withstand capability due to its improved cell structure.

Improved of Avalanche Withstand Capability

1. Improved cell structure

Figure 1 (a) shows a Toshiba power MOSFET cell in cross-section; Figure 1 (b) shows the equivalent circuit.
The power MOSFET contains a parasitic bipolar transistor consisting of source N+, base P and drain N–.
The application of overvoltage to the device triggers a potential difference across the base resistor R_B and the parasitic bipolar transistor, destroying the MOSFET.
Accordingly, it is very important to reduce the base resistance. The new cell structure offers the following improvements:

(a) Shortened horizontal length of source N+ domain and reduced base resistance R_B
(b) Extended deep P+ domain in horizontal direction and reduced base resistance R_B
(c) Uniformly distributed current (due to curvature of cell corners), preventing concentration of electrical field

Figure 1 (a) Cross-section of power MOSFET

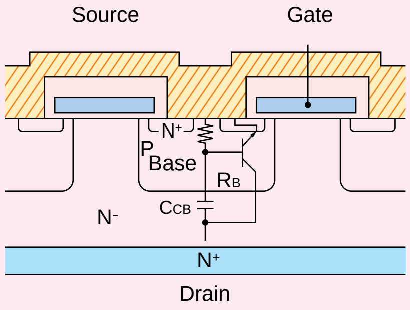
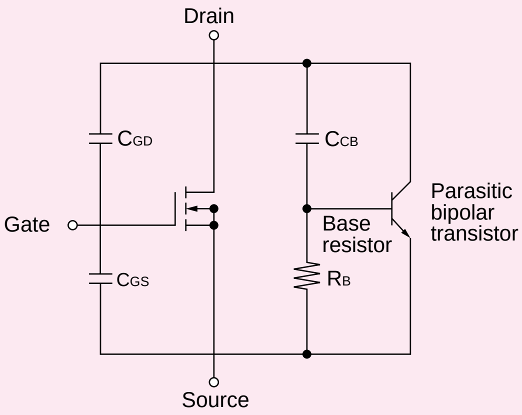


Figure 1 (b) Equivalent circuit



2. Improved gate layout

The power MOSFET consists of multiple small MOSFET cells connected in parallel.
When the current distribution is not uniform, for example when the MOSFET is turned on or off, as mentioned above, the current concentrates in the cells which are slow to turn off, triggering the parasitic bipolar transistor. As a result, these cells are destroyed. To make the power MOSFET highly resistant to destruction, Toshiba have improved the gate wiring and track layout so that the distribution of current received by the cells is balanced.

Avalanche Withstand Capability

Figure 2 shows a power MOSFET avalanche test circuit. Figure 4 shows the test waveform. When the gate voltage V_{GS} falls below the threshold voltage when the MOSFET is turned off, the drain current I_D from the inductance L falls and the drain voltage V_{DS} rises sharply. When the gate voltage V_{GS} rises above the threshold voltage, I_D flows through the channel area of the MOSFET, but when V_{GS} falls below the threshold voltage, the channels are obstructed and I_D finds a new route to the diode between the drain and the base. At the same time, V_{DS} rises. When V_{DS} reaches the self-breakdown voltage BV_{DSS}, the power MOSFET experiences avalanche breakdown and V_{DS} stabilizes. The energy stored in the inductor L is transformed to joule energy and expended in the form of a rise in device temperature. As a result, $I_D = 0$ and V_{DS} becomes equal to the applied voltage V_{DD}. Avalanche withstand capability means that the device has the capacity to expend the energy accumulated in L (the load) without exceeding its rated maximum junction temperature.

Figure 3 shows the test results for the π-MOS V Series, which offers improved avalanche withstand capability, and a comparison with conventional devices. The maximum ratings for the test device were: 500 V for the drain voltage and 8 A for the drain current. In the operating waveform shown in Figure 4, the power MOSFET is not destroyed until the peak current $I_{DP} = 13$ A. Instead of being damaged, the MOSFET absorbs the L energy. Clearly, the improved power MOSFET offers a superior level of breakdown tolerance compared to conventional MOSFETs.

Figure 2 Test circuit

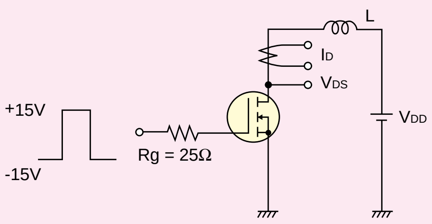
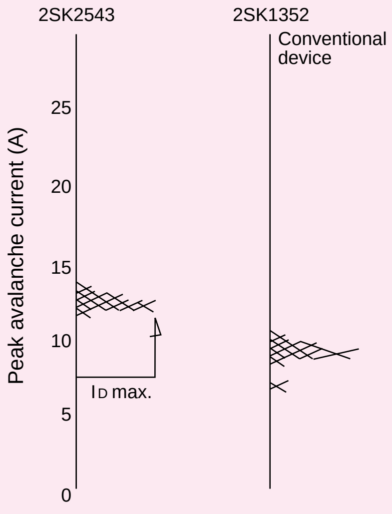
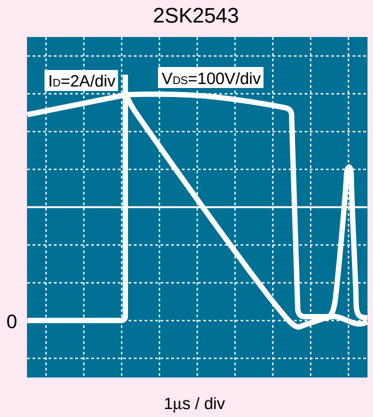


Figure 3 Test results



@L = 200µH, VDD = 90V

Figure 4 Test waveform



Guaranteed Avalanche Withstand Capability Series

For the new generation of recommended products, the measures described above have been used to achieve superior avalanche withstand capability. The devices are guaranteed to be avalanche-resistant for both single pulse and continuous-pulse load.
Table 1 lists the series devices which are guaranteed avalanche-tolerant.

● Table 1 Guaranteed avalanche withstand capability series

Drain-Souvce Voltage [V_{DSS} (V)]	Guranteed Series	Product No. Example	Drain-Souvce Voltage [V_{DSS} (V)]	Guranteed Series	Product No. Example
16~100	L^2-π-MOSV	**2SK2312**	200~250	π-MOSV	**2SK2382**
	U-MOSI	**2SK2466**	400~600	π-MOSV	**2SK2543**
	U-MOSII	**TPC8003**	800~900	π-MOSIII	**2SK2717**

Avalanche Withstand Capability Guarantee Method

1. Description of individual specifications

The specific avalanche current and avalanche energy are given in the maximum ratings column in the technical specifications for each individual device in the guaranteed avalanche resistance series.

Maximum ratings (Ta = 25˚C)

Item		Symbol	Ratings	Unit
Drain-Source Voltage		V_{DSS}	500	V
Drain-Gate Voltage (R_{GS} = 20 kΩ)		V_{DGR}	500	V
Gate-Source Voltage		V_{GSS}	±30	V
Drain Current	DC	I_D	8	A
	Pulse	I_{DP}	32	A
Power Dissipation (T_C = 25˚C)		P_D	40	W
Avalanche Energy (single pulse)**		E_{AS}	312	mJ
Avalanche Current		I_{AR}	8	A
Avalanche Energy (continuous)*		E_{AR}	4	mJ
Channel Temperature		T_{ch}	150	˚C
Storage Temperature		T_{stg}	-55~150	˚C

Notes:
* When current is applied continuously, the pulse width is controlled by the product’s channel temperature.
** Conditions for measurement of avalanche energy (single pulse)
V_{DD} = 90V, T_{ch} = 25˚C, L = 8.3mH, R_G = 25Ω, I_{AR} = 8A

Applied as a single pulse which can be withstood
If this level of energy is applied under the following conditions (as described in the notes), the channel temperature will reach 150˚C.

Maximum peak current tolerable under avalanche conditions Ensure that this current is never exceeded during an avalanche under any circumstances.

Level of energy for each single pulse which can be withstood during a continuous avalanche
When Tc = 25˚C, f = 10 kHz is specified.

2. How avalanche withstand capability is guaranteed

Avalanche withstand capability is guaranteed for the device’s maximum channel temperature, assuming that the avalanche current (I_{AR}) is below the rating given in the datasheet. The channel temperature, taking into account other losses as well as the ambient temperature, must be less than or equal to 150˚C.

Single pulse

Case 1: When the device breaks down completely

Avalanche withstand capability is guaranteed when a single-pulse surge voltage at power-on exceeds the maximum rating.

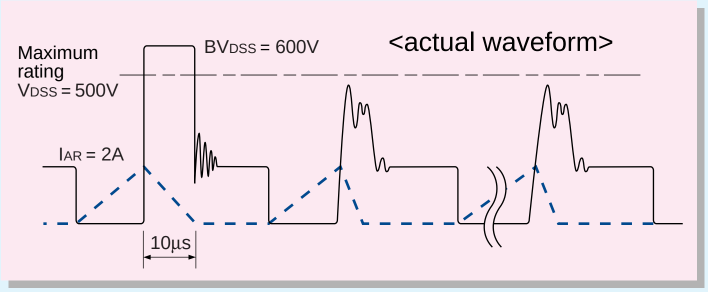
Calculate the channel temperature using equation (1). If the maximum channel temperature, taking into account the ambient temperature, is equal to or less than 150˚C, the avalanche withstand capability is within the guaranteed range.

Equation (1)

$$T_{ch\,max} \fallingdotseq 0.473 \cdot BV_{DSS} \cdot I_{AR} \cdot r_{th(ch\text{-}c)} + T_C$$

0.473: Coefficient ··· See the numbered sections below.
BV_{DSS}: Device breakdown voltage
I_{AR}: Avalanche current
$R_{th(ch\text{-}c)}$: Thermal resistance between channel and case during avalanche
T_C: Case temperature

Example (1) Device used: 2SK2543
Case temperature: Tc = 80˚C



In this case, in which complete breakdown occurs as a result of the surge current generated by a single pulse, the maximum channel temperature can be calculated using equation (1).

$$T_{ch\,max} \fallingdotseq 0.473 \cdot 600 \cdot 2 \cdot 0.0147 + 80$$
$$\fallingdotseq 88^\circ C$$

In this case the rise in channel temperature ΔT_{ch} caused by the avalanche is 8˚C. The maximum channel temperature Tch is therefore 88˚C. Accordingly, it is possible to ascertain whether or not the device can be used by determining whether or not temperature rise caused by subsequent normal operation will cause the channel temperature to exceed the maximum rating.

Section 1

About equation (1)

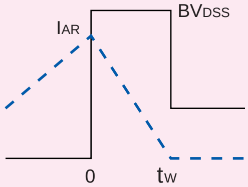


Figure 4 (a)

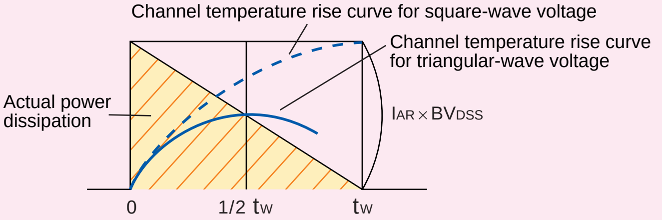


Figure 4 (b)

The power dissipation (P_D) for the current and voltage waveform (Figure 4 (a)) is a triangular waveform, as shown in the shaded area of Figure 4 (b). The corresponding temperature rise curve is shown by the solid line in Figure 4 (b), with the maximum temperature at 1/2tw. The maximum channel temperature at 1/2tw can be calculated as 0.669 × the square wave channel temperature.

Hence, the maximum channel temperature $T_{ch\ max}$ is:

$$T_{ch\ max} \fallingdotseq 0.669 \cdot BV_{DSS} \cdot I_{AR} \cdot r_{th(1/2tw)} + T_{ch}$$

$$r_{th(1/2tw)} \fallingdotseq 1/\sqrt{2} r_{th(tw)}$$ Since this can be approximated to (1/2tw) . . .

$$T_{ch\ max} \fallingdotseq 0.669 \cdot 1/\sqrt{2} \cdot BV_{DSS} \cdot I_{AR} \cdot r_{th(tw)} + T_{ch}$$

$$\fallingdotseq 0.473 \cdot BV_{DSS} \cdot I_{AR} \cdot r_{th(tw)} + T_{ch}$$

Case 2: Although the maximum rating is exceeded, device breakdown does not occur

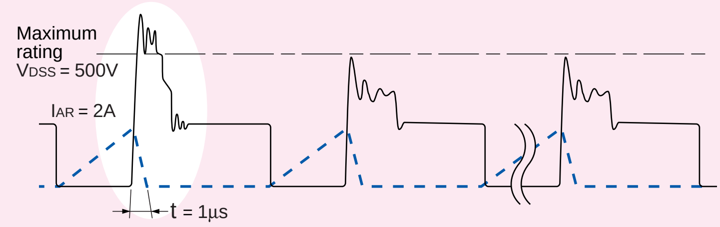
Likewise, if the device does not break down when the surge voltage generated at power-on exceeds the maximum rating (since a 2SK2543 is used, the maximum rating for V_{DSS} is 500 V), approximate the power dissipation waveform to a square waveform and calculate the channel temperature using equation (2).

Equation (2)

$$T_{ch\ max} \fallingdotseq P_D \cdot r_{th\ (ch\text{-}c)} + T_c$$

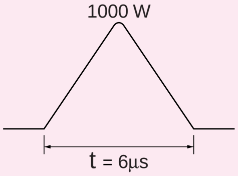
P_D: Power dissipation waveform approximated to a square waveform
$R_{th(ch\text{-}c)}$: Thermal resistance between channel and case for power dissipation waveform approximated to a square waveform with pulse width X.

Example (2) Device used: 2SK2543
Case temperature: Tc = 80˚C

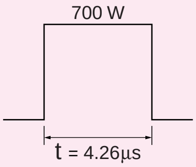


Calculate the power dissipation from Section 2. Strictly speaking, the temperature rise caused by switching loss and the temperature rise from the avalanche loss ought to be considered separately. However, these losses can be calculated together, since device operation is guaranteed for channel temperatures up to a given maximum temperature.

Power dissipation



Power dissipation waveform approximated to a square waveform



Calculate the channel temperature from the power dissipation waveform approximated to a square waveform using equation (2).

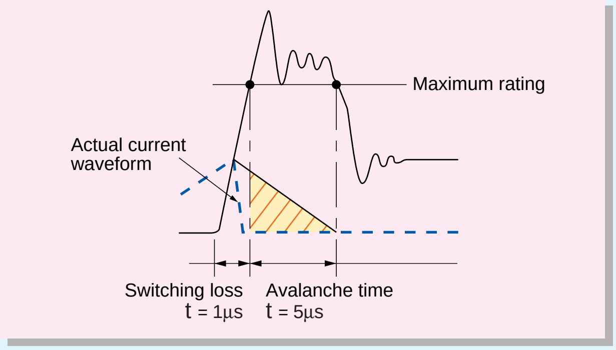
$$T_{ch\ max} \fallingdotseq 700 \cdot 0.0094 + 80$$

$$\fallingdotseq 87^\circ C$$

In this case the rise in channel temperature (including switching loss) ΔT_{ch} caused by the avalanche is 7˚C. Hence, the resulting channel temperature T_{ch}max is 87˚C

Accordingly, it is possible to ascertain whether or not the device can be used by determining whether or not temperature rise caused by subsequent normal operation will cause the channel temperature to exceed the maximum rating

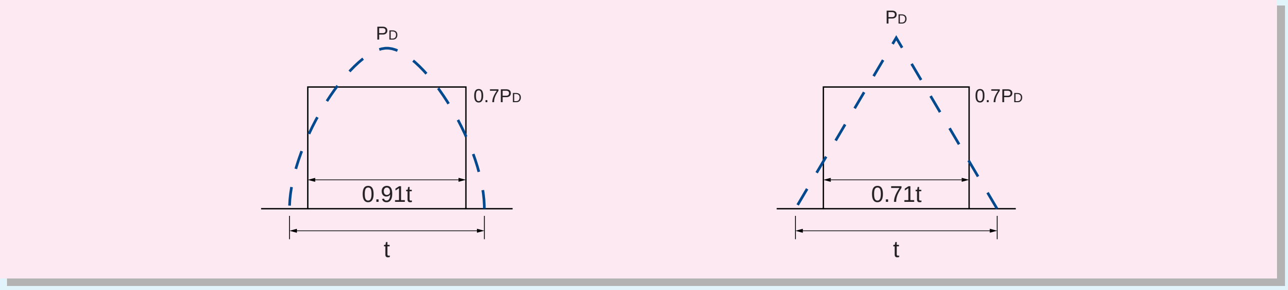
Section 2



Calculation of the period for which the maximum rating (V_{DSS} = 500 V) is exceeded assumes that the current indicated by the solid line is flowing.

Section 3

When the power loss has been calculated using approximation to a square waveform, it is then straightforward to use the following diagrams to calculate the actual temperature.



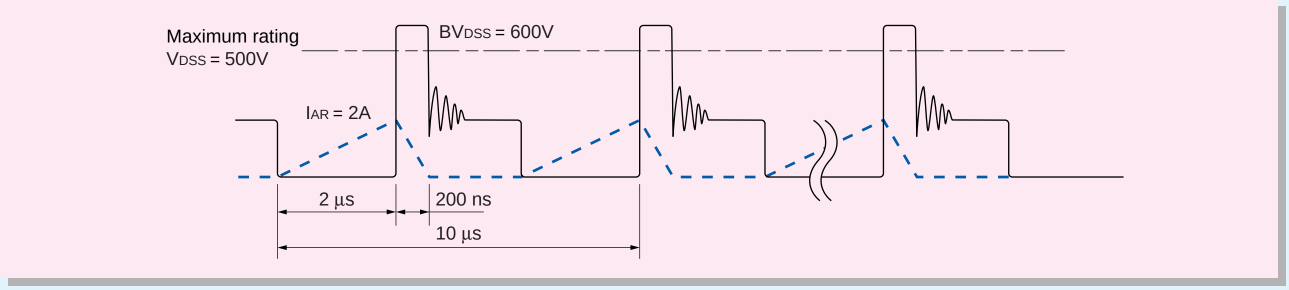
Continuous pulse

So far, only methods for guaranteeing against a single-pulse avalanche have been shown. The following section describes how to calculate the channel temperature for a continuous pulse, a more likely occurrence under actual operating conditions.

Case 3: In which the device breaks down completely

Even during normal operation, the device may breakdown regularly. If this continues, the total channel temperature must be calculated. Therefore, taking the temperature rise when the power MOSFET is turned on to be (1) and the temperature rise caused by the avalanche effect to be (2), calculate the maximum channel temperature from the combination of (1) and (2) (by the superposition theorem).

Example (3) Device used: 2SK2543
Case temperature: Tc = 80˚C



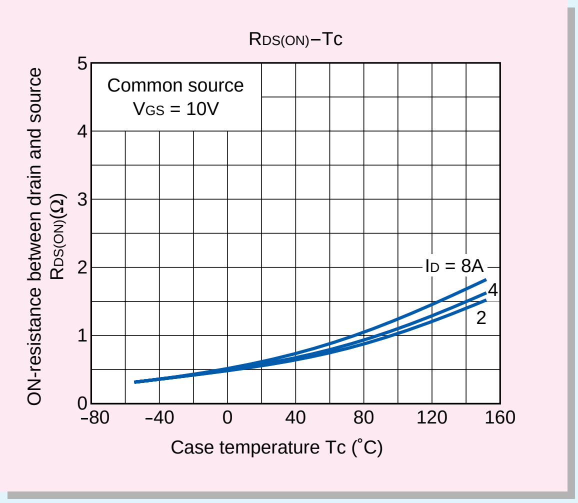
(1) Rise in temperature caused by ON-resistance

Calculate the power dissipation due to the rise in temperature caused by ON-resistance using a value for Tc of 150˚C (the maximum case temperature rating).

Section 4

● **Assumes 2SK2543 R_{DS}(ON).**

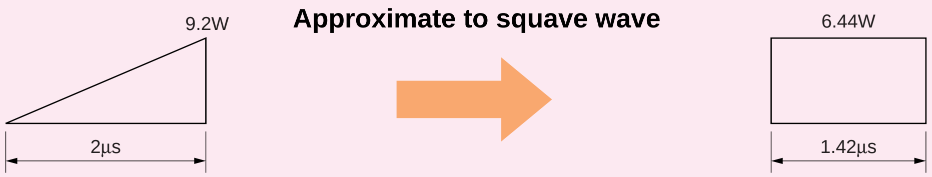
	Typ.	Max
TC = 25˚C	0.75Ω	0.85Ω
TC = 150˚C	1.8Ω	2.04Ω



Calculate the ON-resistance (typ.) at Tc = 150˚C from the R_{DS}(ON) – Tc curve and the typical ratio shown in the electrical characteristics (1.8/0.75 = 2.4×). Applying the same ratio to the device's maximum standards, assume that R_{DS}(ON)max = 2.04Ω at Tc = 150˚C.

Allowing a safety margin of about 10%, assume the maximum ON-resistance = 2.3Ω.

To calculate the power dissipation in this case, assume R_{DS}(ON) = 2.3Ω, based on Section 4.
Using the method shown in Section 3 in which the power dissipation is approximated to a square wave, the power dissipation can be calculated as follows:



Next, from this power dissipation value, calculate the temperature rise using equation (3).

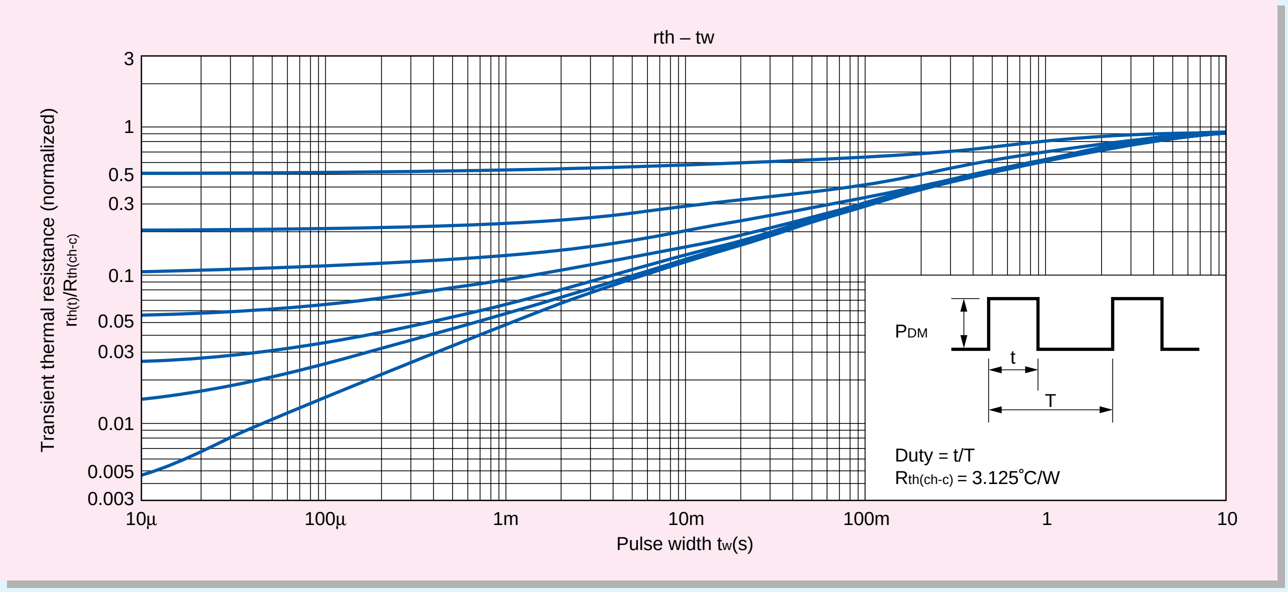
Equation (3)

$$\Delta T_{ch} \fallingdotseq P_D \left[\frac{T_1}{T} R_{th(ch\text{-}c)} + \left(1 - \frac{T_1}{T}\right) \cdot R_{th(T+T_1)} - R_{th(T)} + R_{th(T_1)} \right]$$

P_D : Drain loss approximated to square wave
$R_{th(ch\text{-}c)}$: Thermal resistance between channel and case as described in catalog
T_1 : Pulse width when drain loss is approximated to square wave
T : Cycle
$R_{th(X)}$: Thermal resistance between channel and case for pulse width X

$$\Delta T_{ch} \fallingdotseq 6.44 \left[\frac{1.42}{10} \cdot 3.125 + \left(1 - \frac{1.42}{10}\right) \cdot 0.0159 - 0.0144 + 0.0054\right]$$
$$\fallingdotseq 3^\circ C$$

The transient thermal resistance for a pulse width X in a MOSFET operating at high frequency is not always given in the device’s datasheet. For the 2SK2543, the transient thermal resistance is given for pulse widths of as low as tw = 10µ s. If the transient thermal resistance for a shorter pulse width is required, it can be calculated from equation (4).



Equation (4)

$$R_{th(tw1)} = \sqrt{\frac{tw_1}{tw_2}} \cdot R_{th(tw2)}$$

$R_{th(tw1)}$: Transient thermal resistance for required pulse width tw1

$R_{th(tw2)}$: Transient thermal resistance for pulse width tw2 given in datasheet

Example: Transient thermal resistance for tw = 200 ns

Transient thermal resistance when tw = 10µ s is: $R_{th(ch\text{-}c)} \fallingdotseq 0.00046 \times 3.125 \fallingdotseq 0.0144$

According to equation (4), $R_{th(200ns)} \fallingdotseq \sqrt{\frac{200n}{10\mu}} \cdot 0.0144 \fallingdotseq 0.002^\circ C/W$

(2) Temperature rise caused by avalanche

Calculate the temperature rise caused by the avalanche using equation (5).

Equation (5)

$$\Delta T_{ch} \fallingdotseq 0.473 \cdot BV_{DSS} \cdot I_{AR} \left[\frac{T_1}{T} \cdot R_{th(ch\text{-}c)} + \left(1 - \frac{T_1}{T}\right) \cdot R_{th(T+T_1)} - R_{th(T)} + R_{th(T_1)}\right]$$

$$\begin{aligned}\Delta T_{ch} &\fallingdotseq 0.473 \cdot 600 \cdot 2 \cdot \left[\frac{200n}{10\mu} \cdot 3.125 + \left(1 - \frac{200n}{10\mu}\right) \cdot 0.0147 - 0.0144 + 0.002\right] \\ &\fallingdotseq 37^\circ C\end{aligned}$$

(3) Maximum channel temperature

Calculate the maximum channel temperature by adding the temperature rises calculated in (1) and (2) to the specified case temperature.

$$\begin{aligned}T_{ch\ max} &\fallingdotseq \Delta T_{ch}(R_{DS(ON)}) + \Delta T_{ch(avalanche)} + T_c \\ &\fallingdotseq 3 + 37 + 80 \\ &\fallingdotseq 120^\circ C\end{aligned}$$

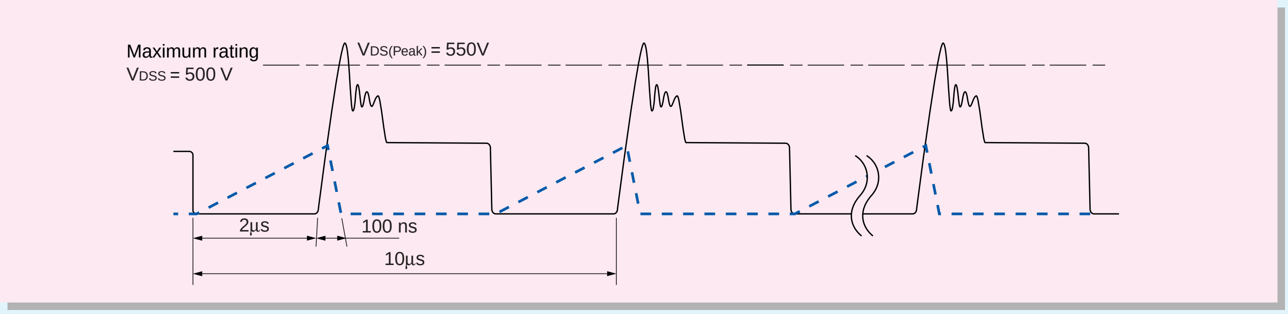
Hence, the maximum channel temperature T_{ch} is 120˚C. In addition, since $I_{AR} < I_D$ (DC), the device can be used during an avalanche.

Case 4: Although the maximum rating is exceeded, the device does not break down.

This is the most common occurrence during actual operation. As described earlier, calculate the resulting temperature by individually calculating the temperature rises caused by the ON-resistance and by the avalanche.

Example (4) Device used: 2SK2543

Case temperature: Tc = 80˚C



Section 6

In this case, the surge voltage, V_{DS}(peak), of 550 V exceeds the maximum rating (V_{DSS} = 500 V), but the device does not break down. As in the previous section, when calculating the power dissipation it is necessary to assume that the current continues flowing during the period in which V_{DSS} = 500 V is exceeded.

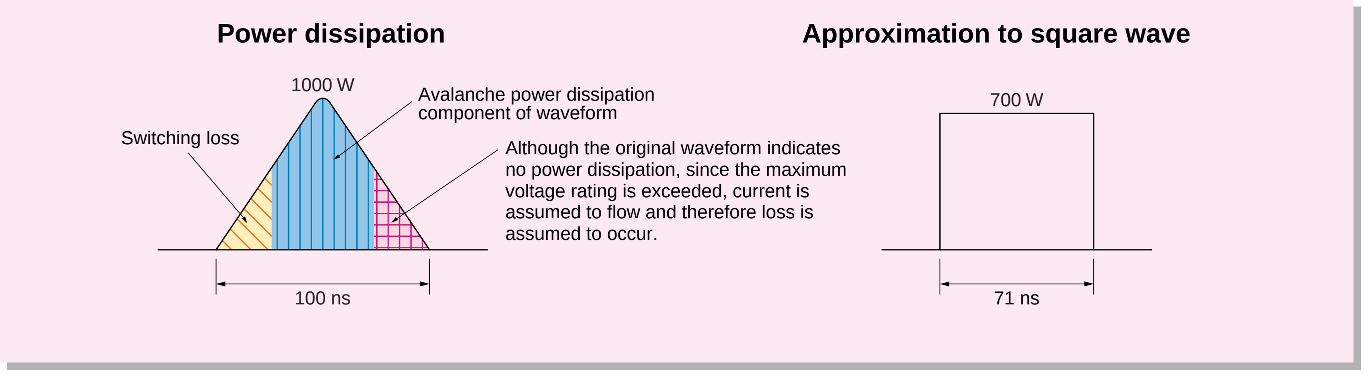
(1) Temperature rise caused by ON-resistance

As before, the channel temperature rise ΔT_{ch} is 3˚C

(2) Temperature rise caused by avalanche

For the purposes of calculating the power dissipation, it is assumed in this case that the current still flows during the period in which the maximum rating is exceeded. By plotting power dissipation versus time, determine the power dissipation during actual operation.

The switching loss represents one component of the power dissipation during the time in which the voltage is rising to its maximum rating. However, as mentioned earlier, these losses can be calculated together, since device operation is guaranteed for channel temperatures up to a given maximum temperature.


Power dissipation **Approximation to square wave**

Although the original waveform indicates no power dissipation, since the maximum voltage rating is exceeded, current is assumed to flow and therefore loss is assumed to occur.

Calculate the channel temperature from equation (3).

$$\Delta T_{ch} \fallingdotseq 700 \cdot [\frac{71n}{10\mu} \cdot 3.125 + (1-\frac{71n}{10\mu}) \cdot 0.0156 - 0.0144 + 0.0012]$$

$$\fallingdotseq 17^\circ C$$

(3) Maximum channel temperature

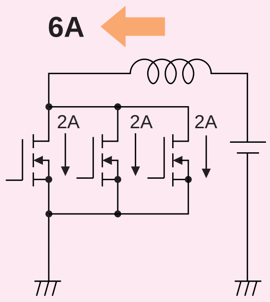
As described earlier, calculate the maximum channel temperature from the specified case temperature and the temperature rises calculated in (1) and (2).

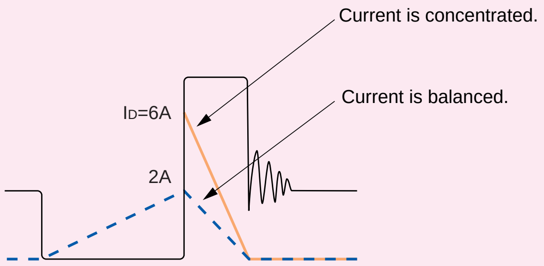
$$
\begin{aligned}
T_{ch\ max} &\fallingdotseq \Delta T_{ch}\,(R_{DS(ON)}) + \Delta T_{ch(\text{switching and avalanche})} + T_c \\
&\fallingdotseq 3 + 17 + 80 \\
&\fallingdotseq 100^{\circ}\mathrm{C}
\end{aligned}
$$

Hence, the channel temperature is within the maximum rating ($T_{ch\ max} = 150^{\circ}\mathrm{C}$). In spite of the fact that the maximum rating is exceeded, it is clear that the maximum temperature is within the range in which the device is guaranteed against avalanche breakdown.

3. Avalanche withstand capability in parallel connection

The power MOSFET's ON-resistance increases with temperature. It is easy to balance the current and, in general, it is easy to connect power MOSFETs in parallel. However, when MOSFETs are connected in parallel, avalanche withstand capability must take account of current concentration caused by fluctuations in the withstand voltage of individual devices. Therefore, take measures against avalanche resulting from the maximum rated current.





Calculate the heat caused by the maximum rated current using the method described on the previous page. Check that the maximum channel temperature does not exceed 150°C (i.e. that $T_{ch\ max} = 150^{\circ}\mathrm{C}$).

Remarks

The method for guaranteeing avalanche withstand capability in this case is described in the section describing the method for calculating device channel temperature. The temperature for the non-avalanche state (in which the maximum rating is not exceeded) can be calculated in the same way.
When using MOSFET products, note that methods for guaranteeing a device against avalanche breakdown vary from manufacturer to manufacturer.

Power MOSFETs Line-up

● π-MOS V (V_{DSS} = 400 ~ 700V)

Applications	Product No.	Maximum Ratings			Package	$R_{DS(ON)}$ (Ω)				V_{th} @ I_D = 1mA (V)	Qg (Typ.) (nC)
		V_{DSS} (V)	I_D (A)	P_D (W)		Typ.	Max	V_{GS} (V)	I_D (A)		
AC 115 V switching power supplies Ballst inverters Motor controllers	**2SK2679**	400	5.5	40	TO-220(NIS)	0.84	1.2	10	3	2.0 ~ 4.0	17
	2SK2838	400	5.5	40	TO-220FL/SM	0.84	1.2	10	3	2.0 ~ 4.0	17
	2SK2952	400	8.5	40	TO-220(NIS)	0.4	0.55	10	5	2.0 ~ 4.0	34
	2SK2841	400	9	80	TO-220AB	0.4	0.55	10	4.5	2.0 ~ 4.0	17
	2SK2949	400	10	65	TO-220FL/SM	0.4	0.55	10	5	2.0 ~ 4.0	34
	2SK3126	450	10	40	TO-220(NIS)	0.48	0.65	10	5	2.0 ~ 4.0	35
	2SK2998	500	0.5	0.5	TO-92MOD	10	18	10	0.25	2.0 ~ 4.0	5
	2SK3302	500	0.5	1.3	TPS	10	18	10	0.25	2.0 ~ 4.0	5
	2SK2599	500	2	1.3	TPS	2.9	3.2	10	1	2.0 ~ 4.0	9
	2SK2862	500	2	25	TO-220(NIS)	2.9	3.0	10	1	2.0 ~ 4.0	9
	2SK2661	500	5	75	TO-220AB	1.35	1.5	10	2.5	2.0 ~ 4.0	17
	2SK2662	500	5	35	TO-220(NIS)	1.35	1.5	10	2.5	2.0 ~ 4.0	17
	2SK2991	500	5	40	TO-220FL/SM	1.35	1.5	10	2.5	2.0 ~ 4.0	17
	2SK2542	500	8	100	TO-220AB	0.75	0.85	10	4	2.0 ~ 4.0	30
	2SK2543	500	8	40	TO-220(NIS)	0.75	0.85	10	4	2.0 ~ 4.0	30
	2SK2776	500	8	65	TO-220FL/SM	0.75	0.85	10	4	2.0 ~ 4.0	30
	✻ 2SK2600	500	8	80	TO-3P(N)IS	0.75	0.85	10	4	2.0 ~ 4.0	30
	2SK2601	500	10	125	TO-3P(N)	0.75	1.0	10	5	2.0 ~ 4.0	30
	2SK2842	500	12	40	TO-220(NIS)	0.4	0.52	10	5	2.0 ~ 4.0	45
	2SK3068	500	12	100	TO-220FL/SM	0.4	0.52	10	6	2.0 ~ 4.0	45
	2SK2916	500	14	80	TO-3P(N)IS	0.35	0.4	10	7	2.0 ~ 4.0	58
	2SK2698	500	15	150	TO-3P(N)	0.35	0.4	10	8	2.0 ~ 4.0	58
	2SK2917	500	18	90	TO-3P(N)IS	0.21	0.27	10	10	2.0 ~ 4.0	80
	2SK2837	500	20	150	TO-3P(N)	0.21	0.27	10	10	2.0 ~ 4.0	80
	2SK3117	500	20	150	TO-3P(SM)	0.21	0.27	10	10	2.0 ~ 4.0	80
	2SK3132	500	50	250	TO-3P(L)	0.07	0.095	10	25	2.0 ~ 4.0	280
	2SK2836	600	1	2.5	SP	6.4	9.0	10	0.5	2.0 ~ 4.0	9
	2SK2846	600	2	1.3	TPS	4.2	5.0	10	1	2.0 ~ 4.0	17
	2SK2865	600	2	20	PW-MOLD	4.2	5.0	10	1	2.0 ~ 4.0	17
	2SK3067	600	2	25	TO-220(NIS)	4.2	5.0	10	1	2.0 ~ 4.0	9
	2SK2750	600	3.5	35	TO-220(NIS)	1.7	2.2	10	1.8	2.0 ~ 4.0	20
	✻ 2SK3085	600	3.5	75	TO-220AB	1.7	2.2	10	1.8	2.0 ~ 4.0	20
	2SK2544	600	6	100	TO-220AB	1.0	1.25	10	3	2.0 ~ 4.0	30
	2SK2545	600	6	40	TO-220(NIS)	1.0	1.25	10	3	2.0 ~ 4.0	30
	2SK2777	600	6	65	TO-220FL/SM	1.0	1.25	10	3	2.0 ~ 4.0	30
	2SK2602	600	6	125	TO-3P(N)	1.0	1.25	10	3	2.0 ~ 4.0	30
	2SK2996	600	10	45	TO-220(NIS)	0.74	1.0	10	5	2.0 ~ 4.0	38
	2SK2843	600	10	40	TO-220(NIS)	0.54	0.75	10	5	2.0 ~ 4.0	45
	2SK2886	600	10	100	TO-220AB	0.54	0.75	10	5	2.0 ~ 4.0	45
	2SK2889	600	10	100	TO-220FL/SM	0.54	0.75	10	5	2.0~ 4.0	45
	2SK2699	600	12	150	TO-3P(N)	0.52	0.65	10	6	2.0 ~ 4.0	60
	2SK2953	600	15	90	TO-3P(N)IS	0.31	0.4	10	8	2.0 ~ 4.0	80
	2SK2915	600	16	150	TO-3P(N)	0.31	0.4	10	8	2.0 ~ 4.0	80
	2SK3265	700	10	45	TO-220(NIS)	0.72	1.0	10	5	2.0 ~ 4.0	53

✻ Under development

● π-MOS Ⅲ (V_{DSS} = 800 ~ 1000V)

Applications	Product No.	Maximum Ratings			Package	$R_{DS(ON)}$ Max(Ω)	V_{th} @I_D=1mA (V)	Qg (Typ.) (nC)
		V_{DSS} (V)	I_D (A)	P_D (W)				
220-V/240-V AC input switching power supplies	**✻ 2SK2997**	800	1.5	40	DP	8.0	2.0~4.0	—
	2SK2603	800	3	100	TO-220AB	3.6	2.0~4.0	25
	2SK2883	800	3	80	TO-220FL/SM	3.6	2.0~4.0	25
	2SK2604	800	5	125	TO-3P(N)	2.2	2.0~4.0	34
	2SK2605	800	5	45	TO-220(NIS)	2.2	2.0~4.0	34
	2SK2884	800	5	100	TO-220FL/SM	2.2	2.0~4.0	34
	2SK2746	800	7	150	TO-3P(N)	1.7	2.0~4.0	55
	2SK2606	800	8.5	85	TO-3P(N)IS	1.2	2.0~4.0	68
	2SK2607	800	9	150	TO-3P(N)	1.2	2.0~4.0	68
	2SK3301	900	1	20	PW-MOLD	20	2.4~3.4	6
	2SK2733	900	1	60	TO-220AB	9.0	2.0~4.0	15
	2SK2845	900	1	40	DP	9.0	2.0~4.0	15
	2SK2718	900	2.5	40	TO-220(NIS)	6.4	2.0~4.0	21
	2SK2608	900	3	100	TO-220AB	4.3	2.0~4.0	25
	2SK2700	900	3	40	TO-220(NIS)	4.3	2.0~4.0	25
	2SK2719	900	3	125	TO-3P(N)	4.3	2.0~4.0	25
	✻ 2SK3088	900	3	80	TO-220FL/SM	4.3	2.0~4.0	25
	2SK2610	900	5	150	TO-3P(N)	2.5	2.0~4.0	45
	2SK2717	900	5	45	TO-220(NIS)	2.5	2.0~4.0	45
	2SK2749	900	7	150	TO-3P(N)	2.0	2.0~4.0	55
	2SK2847	900	8	90	TO-3P(N)IS	1.4	2.0~4.0	58
	2SK3017	900	8.5	90	TO-3P(N)IS	1.25	2.0~4.0	70
	2SK2611	900	9	150	TO-3P(N)	1.4	2.0~4.0	58
	2SK2968	900	10	150	TO-3P(N)	1.25	2.0~4.0	70
	✻ 2SK2613	1000	8	150	TO-3P(N)	1.8	2.0~4.0	—

✻ Under development

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