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Digital Controller Design for Buck and Boost Converters Using Root Locus Techniques

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Abstract—**Root locus techniques to design digital controllers for buck and boost converters are discussed in this paper. The small signal models of both converters are first transformed into discrete-time models using the matched pole-zero mapping method. Digital controllers are designed based on the discrete-time model using the root locus method. By selecting the poles, zeros and gain of the digital controllers, the closed-loop poles are placed at desired locations in the z-plane. The digital controllers are then implemented on a TI DSP. The root locus design method is compared with the frequency response design method. Experimental results from the buck converter indicate that the results obtained using the root locus method are comparable to the results obtained using the frequency response method, while results from the boost converter indicate the nonlinear nature of the boost converter small signal model may degrade the performance of the design using the root locus method.**

I. INTRODUCTION

Different methods can be utilized to design digital controllers for buck and boost converters. Analog PID controllers were designed using converter small signal models and frequency response methods [8]. The main criteria considered in the design were the gain at low frequency, the crossover frequency and the phase margin. The analog controllers were then transformed into digital controllers using the backward integration method [4], and implemented on a TI TMS320F240 DSP. With the regular PID algorithm, the duty cycle oscillated in steady state. The regular PID algorithm was modified to reduce this oscillation and improve the controller's stability while maintaining the fast transient response. Three algorithm modifications were applied to the controller to improve the steady state performance. The modifications were a dead zone, an averaging digital filter and two sets of gains.

Another approach for the design of digital controllers for DC-DC converters is discussed in this paper. The small signal models for the converters are first transformed into discrete-time models using the matched pole-zero mapping method. The root locus technique is then utilized to design digital controllers. The poles, zeros and gain of the digital controller are designed to place the closed-loop poles at the desired positions. The digital controllers are then implemented on the TI DSP. Experimental results are obtained and compared with the results obtained using the frequency response method. In the root locus design, the duty cycle in steady state doesn't oscillate as much as in the frequency response method for both the buck and boost converters, therefore no algorithm modifications are required for the digital controllers. For the buck converter, the two design methods generate comparable results. For the boost converter, the frequency response method produces experimental results that match the design better. The zero and complex poles of the boost converter small signal model move as a function of the duty cycle D [1]. This makes the boost converter's transfer function a nonlinear function of D. The digital controller is only designed for a specific duty cycle. On the other hand, change of the duty cycle only affects the DC gain, but has no impact on the poles and zeros of the buck converter's small signal model.

II. CONVERTER SMALL SIGNAL MODELS

A. Buck Converter

The small signal model of the buck converter is [1]:

$$\frac{\hat{v}_0(s)}{\hat{d}(s)} = \left(\frac{V_o}{D}\right)\left[\frac{1+sRcC}{1+s\left(RcC+[R//R_L]C+\frac{L}{R+R_L}\right)+s^2LC\left(\frac{R+Rc}{R+R_L}\right)}\right] \quad (1)$$

The input voltage of the prototype buck converter is 20 V, and the output voltage Vo is 12 V. The load resistance R is 10 Ω, L is 150 μH and C is 1000 μF. The parasitic elements, Rc and R_L, are estimated to be 30 mΩ and 10 mΩ, respectively. The actual frequency response of the buck converter is measured using a Model 102B analog network analyzer from AP Instruments, and compares favorably with the small signal model in (1).

The small signal model is then transformed into the discrete-time model using the matched pole-zero mapping method. The small signal model's poles and zeros are mapped to the z plane according to the relation of $z = e^{sT}$. A finite pole or zero at $s = -a$ is mapped to $z = e^{-aT}$, and an infinite pole or zero is mapped to $z = -1$ [3]. The sampling period T is 50 μs. It is the same as the sampling period in the frequency response design method for the sake of comparison. The discrete-time

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model obtained using the matched pole-zero mapping method has good accuracy to reproduce the transient response and relatively low sensitivity to coefficient variations [6]. The discrete-time model obtained for the buck converter is:

$$G(z) = \frac{0.4058z - 0.0767}{z^2 - 1.9654z + 0.9819} \quad (2)$$

The zero of the discrete-time model is 0.1889, and the poles are 0.9827 +/- 0.1271i. The root locus for the model is shown in Fig. 1. The two poles are very close to the unit circle, which results in the system being very close to critical stability. This will be adjusted using the root locus design method in a later section.

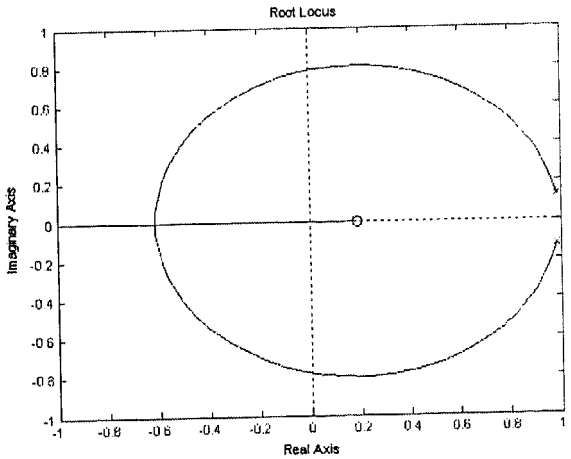

Fig. 1. Root locus of the buck converter discrete-time model

B. Boost Converter

The small signal transfer function of the boost converter is [5]: (3)

$$\frac{\hat{v}_o(s)}{\hat{d}(s)} = \frac{V_O}{D_O L_e C} \frac{(1 - \frac{sL_e}{R})(sR_C C + R_C/R + 1)}{s^2 + s\left[\frac{(R_L/D_O^2) + (R_C/D_O)}{L_e} + \frac{1}{CR}\right] + \frac{(R_L/D_O^2) + (R_C/D_O)}{L_e CR} + \frac{1}{L_e C}}$$

where $Le = L/(1-D)^2$ and $D_O = 1\text{-}D$.

For the experiment the input voltage is 5 V, the output voltage Vo is 12 V, and the duty cycle D is 58%. C is 1056 μF, L is 250 μH, and R is 25 Ω. The parasitic elements, R_C and R_L, are estimated from data sheets to be 30 mΩ and 10 mΩ, respectively. The frequency response of the boost converter when operating at steady state is also obtained using the analog network analyzer. There is a clear discrepancy between the theoretical model and the frequency response measured. By fitting the experimental frequency response data using Matlab, a transfer function for the boost converter is:

$$\frac{\hat{v}_o(s)}{\hat{d}(s)} = \frac{-5.6956*10^{-3}s^2 - 2.5589*10^2 s + 4.9831*10^6}{s^2 + 8.2525*10^2 s + 5.4241*10^5} \quad (4)$$

The discrete-time model for the boost converter is obtained by converting this transfer function into the z-plane transfer function using the matched pole-zero mapping method. The sampling period T is also 50 μs. The discrete-time transfer function is:

$$G(z) = \frac{-0.0119z^2 + 0.0253z - 0.0013}{z^2 - 1.9582z + 0.9596} \quad (5)$$

The root locus of the boost converter is shown in Fig. 2. The zeros of the z-plane model are 2.0832 and 0.0508. The poles are at 0.9791 +/- 0.0299i, and are also very close to the unit circle. The zeros don't affect the absolute stability of the system[3].

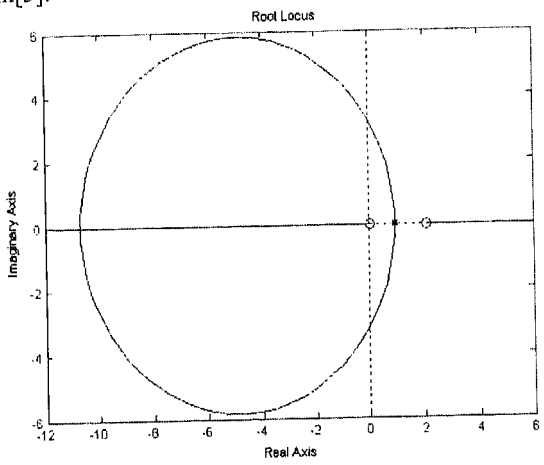

Fig. 2. Root locus of the boost converter discrete-time model

III. DIGITAL CONTROLLER DESIGN USING ROOT LOCUS

A. Buck Converter Controller Design

Based on the z-plane model in (2) and the root locus plot in Fig. 1, a digital controller for the buck converter is designed. The two poles of the controller are placed on the real axis. Their values are 1 and 0.1353, respectively. The two zeros of the controller are placed at 0.6 and 0.8, respectively. The gain of the controller is tuned to be 3.6. The resulting root locus of the compensated system is shown in Fig. 3. The closed-loop poles are at 0.0015, 0.8241 and 0.4071 +/- 0.4338i. Since all the closed-loop poles lie well within the unit circle, the system's stability is guaranteed. The transfer function of the controller is:

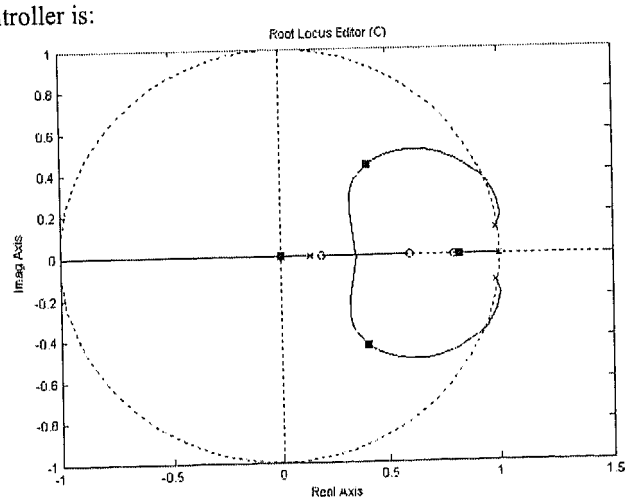

Fig. 3. Root locus of the compensated buck converter

$$G_C(z) = \frac{3.6z^2 - 5.04z + 1.728}{z^2 - 1.13z + 0.13} \quad (6)$$

B. Boost Converter Controller Design

A digital controller for the boost converter is also designedusing the root locus method, based on the model in (5), and the root locus in Fig. 2. The two poles of the controller are chosen to be 1 and 0.13, respectively. The controller's two zeros are placed at 0.85 and 0.9. By using the root locus design tools in Matlab, the gain is adjusted to be 30 to provide the root locus in Fig. 4. The closed-loop poles are 0.73 +/- 0.254i, 0.273 and 0.915. The digital controller's transfer function is:

$$G_C(z) = \frac{z^2 - 1.75z + 0.765}{z^2 - 1.13z + 0.13} \quad (7)$$

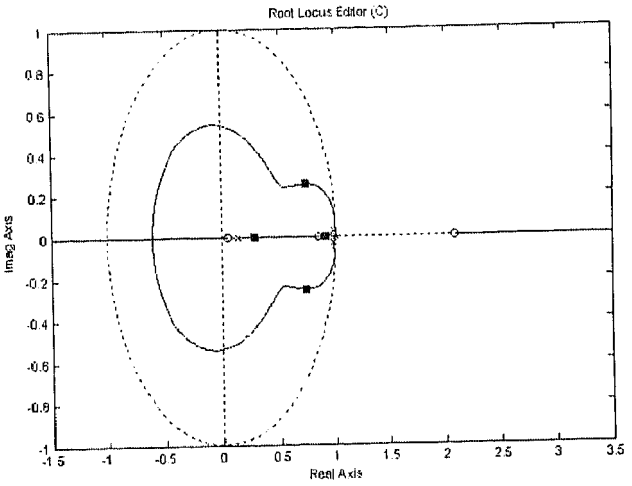

Fig. 4. Root locus of the compensated boost converter

IV. EXPERIMENTAL RESULTS

A. Buck Converter

The transfer function of the digital controller in (6) is converted into a difference equation, which is utilized to calculate a new duty cycle:

$$u(k) = 1.13u(k-1) - 0.13u(k-2) + 3.6e(k) - 5.04e(k-1) + 1.728e(k-2) \quad (8)$$

In the difference equation, u(k) is the controller's output for the kth sample, and e(k) is the error of the kth sample. The digital controller is implemented on the TI TMS320F240 DSP. The start up transient response of the buck converter is shown in Fig. 5. The settling time is about 1 ms with very little overshoot. The steady state response and PWM signal are shown in Fig. 6. Fig. 7 shows the ripple in steady state. The magnitude of the ripple is about 200 mV.

Previous work was done to design digital PID controllers for the buck and boost converters using the frequency response technique [8]. The PID algorithm was modified to reduce the oscillation of the duty cycle and improve the controller's stability while maintaining the fast transient response. Three algorithm modifications were added to the controller to improve the steady state response. They were

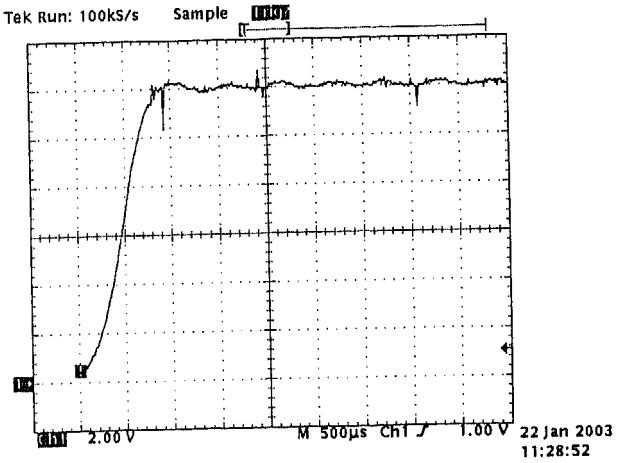

Fig. 5. Start up transient response of the buck converter using root locus method
(2V/div, 500µs/div)

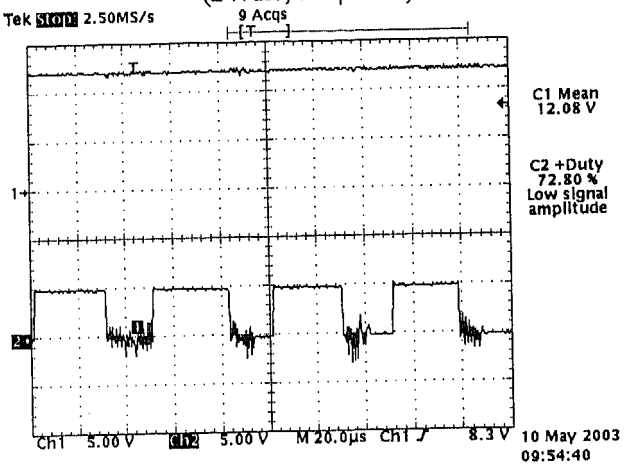

Fig. 6. Steady state response of the buck converter using root locus method
(5V/div, 20 µs/div)

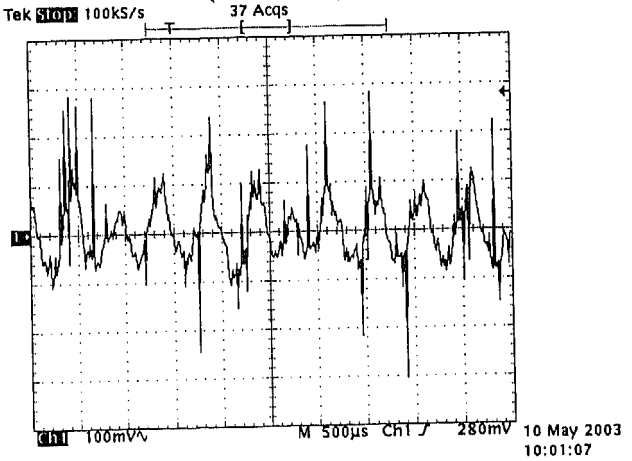

Fig. 7. Steady state ripple of the buck converter using root locus
(100mV/div, 500 µs/div)

dead zone, averaging digital filter and two sets of gains.

The digital controller monitors the output voltage error to determine if a modification should be employed to calculate

the next duty cycle. The start up transient response is shown in Fig. 8. R1 is the dead zone, R2 is the digital filter, and R3 is the two sets of gains. The settling time is comparable to the result in Fig. 5.

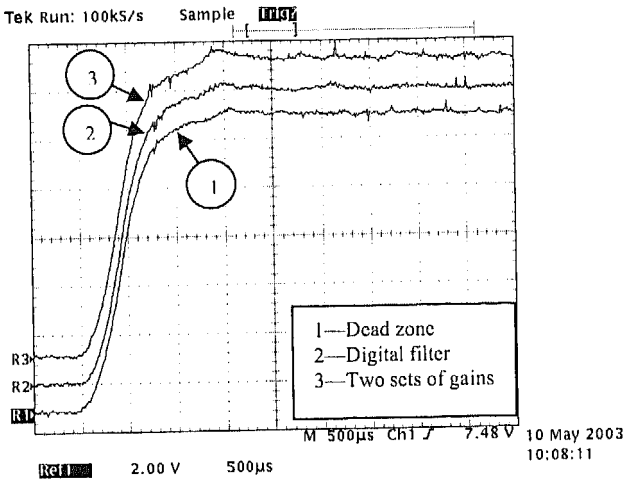

Fig. 8. Start up transient response of the buck converter using frequency response method (2V/div, 500µs/div)

B. Boost Converter

According to the root locus design in Fig. 4, a digital controller was implemented on the TI DSP. The difference equation converted from the transfer function in (7) is :

$$u(k) = 1.13u(k-1) - 0.13u(k-2) + e(k) - 1.75e(k-1) + 0.765e(k-2) \quad (9)$$

The start up transient response is shown in Fig. 9. The output voltage is able to reach the reference in about 10 ms, but there are oscillations in steady state. An expanded view of the steady state response is shown in Fig. 10. The experimental response is not stable, while the root locus in Fig. 4 shows the system is stable. There is a mismatch between the experimental result and the design. The gain of the controller is tuned to improve the performance. When the gain is reduced to 1, a stable start up transient response is obtained, and is shown in Fig. 11. The settling time is about 10 ms. The steady state response and the corresponding PWM signal are shown in Fig. 12. The steady state error is 40 mV. The steady state ripple is shown in Fig. 13. The magnitude of the ripple is about 60 mV. The root locus of the compensated system when the controller's DC gain is 1 is shown in Fig. 14. The three closed-loop poles are close to the unit circle, which makes the system almost critically stable. The experimental results don't correspond to the design. This may be due to the nonlinear property of the boost converter's small signal model, which severely complicates the control problem. The variation of the poles and zeros of the boost converter's discrete-time model is shown is Table I. With the increase of the duty cycle, the two complex conjugate poles move closer to the unit circle, and the value of the zero outside of the unit circle decreases.

TABLE I. Variation of the Poles and Zeros of the Boost Converter Discrete-Time Model

D	Pole1&2	Zero1	Zero2
50%	0.9954 + 0.0484i	0.2063	3.4782
63%	0.9963 +/- 0.0358i	0.2063	2.3754
70%	0.9967 +/- 0.0291i	0.2063	1.5643
75%	0.9970 +/- 0.0242i	0.2063	1.3636

On the other hand, the frequency response design method provides an experimental result that matches the design better. The start up transient, steady state response & PWM signal and ripple are shown in Fig. 15 - 17. The settling time is about the same as the one using the root locus method [8].

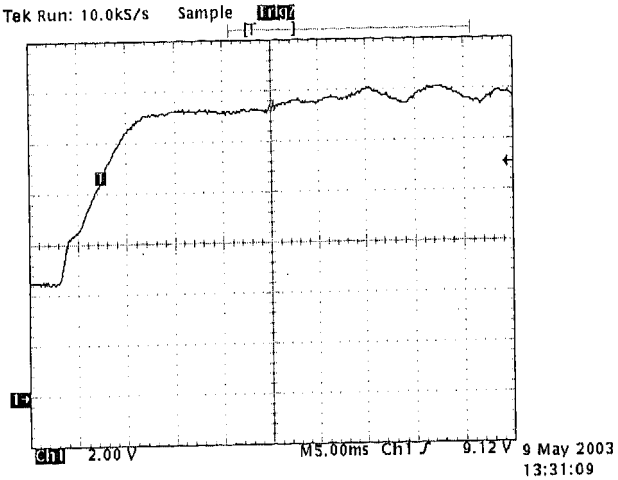

Fig. 9. Start up transient response of the boost converter with controller gain = 30 (2V/div, 5ms/div)

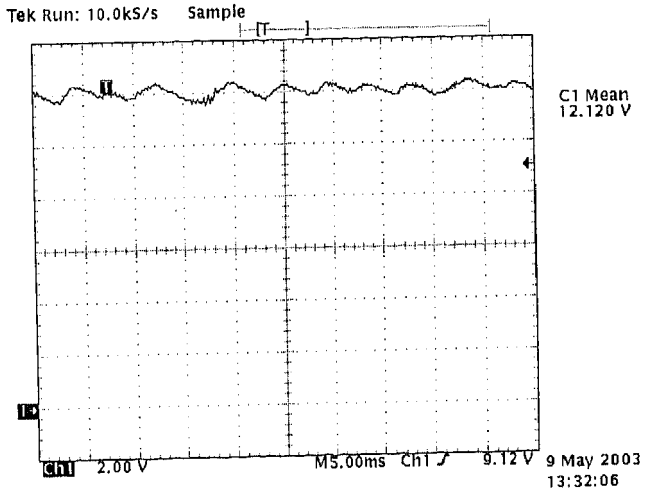

Fig. 10. Steady state response of the boost converter with controller gain = 30 (2V/div, 5ms/div)

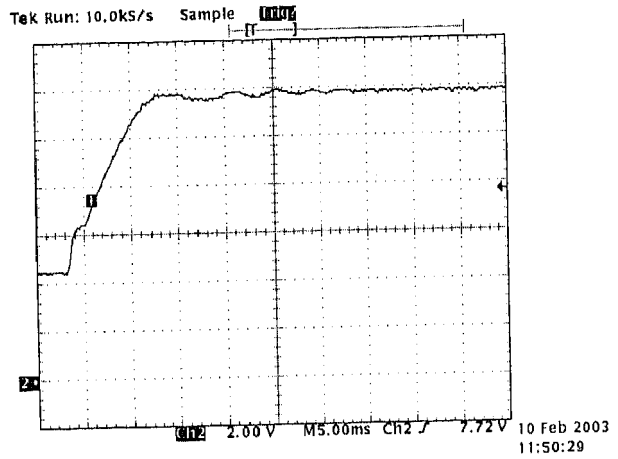

Fig. 11. Start up transient response of the boost converter with controller gain = 1
(2V/div, 5ms/div)

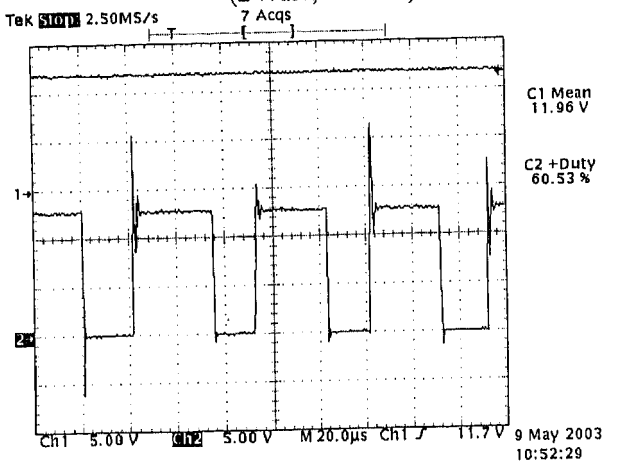

Fig. 12. Steady state response and PWM signal of the boost converter with controller gain = 1
(5V/div, 20 µs/div)

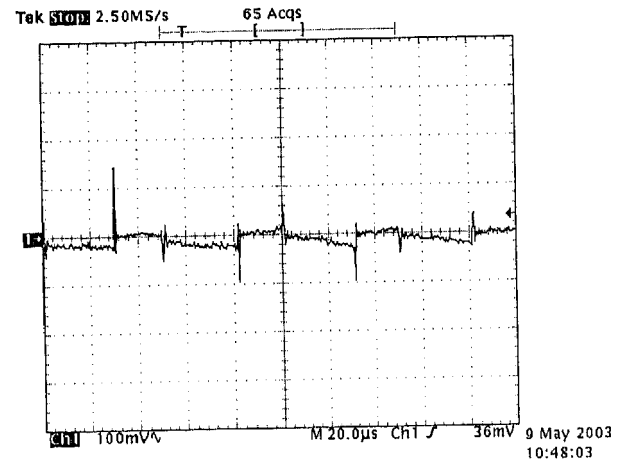

Fig. 13. Steady state ripple of the boost converter with controller gain = 1
(100mV/div, 20 µs/div)

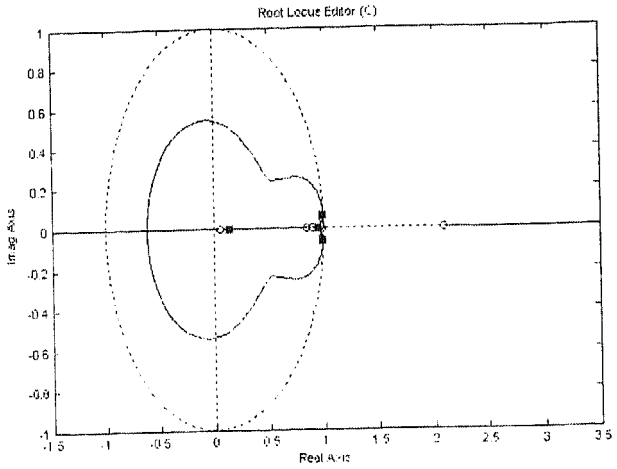

Fig. 14. Root locus of the compensated boost converter with controller gain = 1

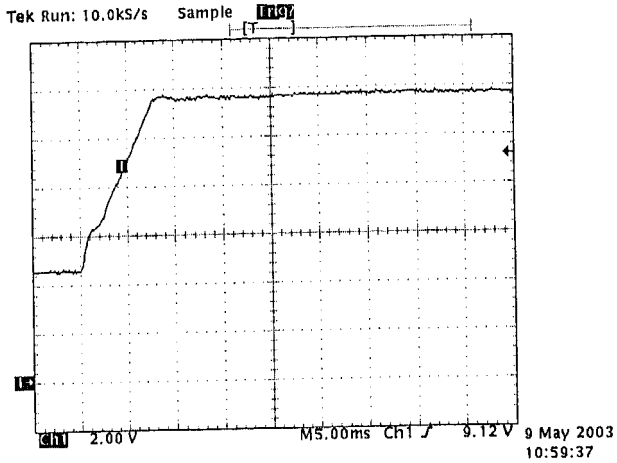

Fig.15. Start up transient response of the boost converter using frequency response design method
(2V/div, 5ms/div)

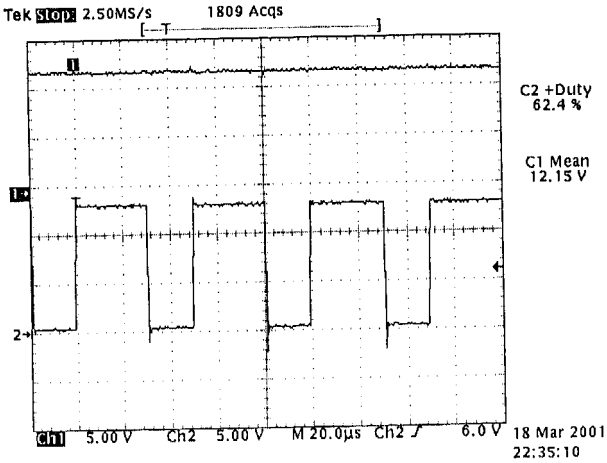

Fig.16. Steady state response and PWM signal of the boost converter using frequency response design method
(5V/div, 20 µs/div)

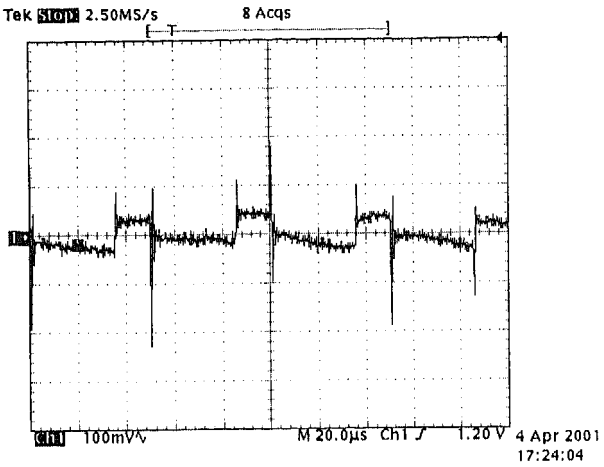

Fig. 17. Steady state ripple of the boost converter using frequency response design method (100mV/div, 20 µs/div)

V. CONCLUSION

This paper discusses using the root locus method to design digital controllers for the buck and boost converters. The matched pole-zero mapping method is used to convert the small signal models of both converters into discrete-time models. Closed-loop poles are placed at certain positions to ensure the system stability and achieve the desired transient and steady state responses. The digital controllers are implemented on a TI TMS320F240 DSP. Experimental results are evaluated and compared with the results achieved using the standard frequency response design method. In the frequency response design method, a standard PID algorithm was first implemented. To reduce the oscillation in the duty cycle and improve steady state response, three modifications were added to the standard PID algorithm [8, 9]. In the root locus design method, these algorithm modifications are not needed.

Experimental results show that, for the buck converter, both design methods are able to generate comparable performance with fast transient response and stable steady state response. While for the boost converter, the frequency response method achieves the result that matches the design better. In the root locus design for the boost converter, the experimental results and the design don't match very well. The differences between the experimental and theoretical results may be caused by the nonlinear character of the boost converter dynamics, which are not well described by the small signal model. This hypothesis is under further investigation.

VI. ACKNOWLEDGMENT

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