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Digital PWM Controller with Feed-Forward Compensation

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***Abstract*— This paper describes a complete digital PWM controller IC with feed-forward compensation of the input voltage. The feed-forward compensation is accomplished through a delay-line digital pulse-width modulator (DPWM) where the cell delay is made inversely proportional to the input voltage. The complete digital controller IC with the feed-forward DPWM operating at 1 MHz switching frequency can be used in a range of DC-DC applications. In particular, with low power consumption, small silicon area (less than 0.25 mm^2 in a standard 0.5 μ CMOS process) and a programmable compensator requiring no external passive components, the controller is targeted to DC-DC conversion applications in low-power battery-operated electronics. Experimental results are presented for the feed-forward DPWM and mixed signal simulations show the validity of the complete digital PWM controller chip.**

Keywords: digital control; feed-forward; DC-DC converter; digital PWM

I. INTRODUCTION

Feasibility of practical high-frequency, high-performance digital controllers in DC-DC applications has recently been demonstrated [1-3]. Based on custom architectures and realizations of the key building blocks, including high-resolution high-frequency digital pulse-width modulators (DPWM), simplified discrete-time compensator schemes, and A/D converters, such controllers can offer the advantages of lower sensitivity to parameter variations, programmability, and reduction or elimination of passive components, without compromising dynamic performance, simplicity or cost.

In this paper, we show how the input-voltage feed-forward compensation, which is well-known and often used in analog voltage-mode PWM controllers [4-6], can be implemented effectively within a high-frequency DPWM without additional A/D converters or any other increase in the chip complexity. The proposed feed-forward DPWM, which is described in Section II, has been tested on an experimental prototype IC. The experimental results show good feed-forward compensation over a wide range of input voltages. A complete digital PWM controller IC having the feed-forward DPWM, a simple table-based programmable compensator, and a very small two-comparator A/D converter, has been designed as reported in Section III. The complete prototype chip is designed for operation at the switching frequency of 1 MHz and is well suited for a range of DC-DC applications. In particular, low power consumption, small controller area, and the programmable compensator requiring no external passive components, are targeted to DC-DC conversion in low-power battery-operated applications [7,8], where the battery voltage (assuming a single-cell Li-Ion battery) varies in the range from about 2.5 V to about 5.5 V. In such applications, it is highly desirable to have all controller components, including the power switches and the compensation, integrated on the same chip. In analog realizations (such as [8] for example), wide process and temperature variations of parameter values of on-chip discrete resistors and capacitors present an important design constraint in terms of the chip area and dynamic performance. The digital table-based compensator implementation described in this paper effectively addresses these problems. Mixed-signal simulation results with the complete controller are presented in Section IV.

This work was supported by National Semiconductor through Colorado Power Electronics Center.

II. FEED-FORWARD DIGITAL PULSE WIDTH MODULATOR

A. Architecture of the feed-forward DPWM

In a switching regulator with voltage-mode control, benefits of a pulse-width modulator with feed-forward compensation include improved line regulation, as well as independence of the loop gain with respect to the input voltage variations [4-6]. Practical implementations of digital controllers for high-frequency switching power converters require high-resolution digital pulse-width modulators [1-3] to enable precise output voltage regulation without limit-cycle oscillations caused by A/D and DPWM quantization [9]. Previously proposed approaches to high-frequency, high-resolution DPWM have not addressed the feed-forward (FF) compensation. To introduce the FF-DPWM proposed in this paper, let us consider the basic delay-line DPWM configuration shown in Fig. 1 [10]. The same idea can be applied to other DPWM realizations [1-3].

At the start of a switching cycle, a clock signal sets the SR flip-flop and starts the clock signal propagation through a chain of delay cells. When the signal reaches the delay cell selected by the digital duty-cycle command $d[n]$, the flip-flop is reset. The output pulse width t_{on} is equal to

$$t_{on} = kt_d, \tag{1}$$

where k is the numerical value of the duty command $d[n]$, and t_d is the cell delay. To achieve the feed-forward compensation, the product of the converter input voltage V_{in} (or a voltage proportional to the input voltage) and the pulse width t_{on} should

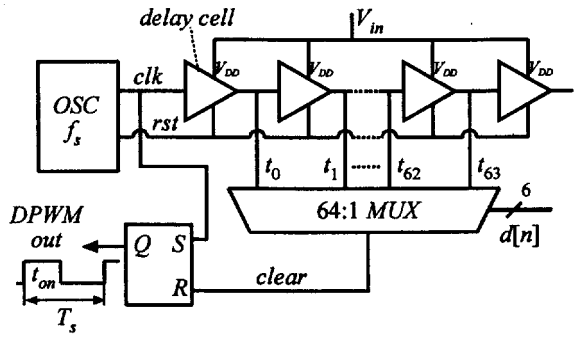


Figure 1. Simplified diagram of the 6-bit feed-forward DPWM.

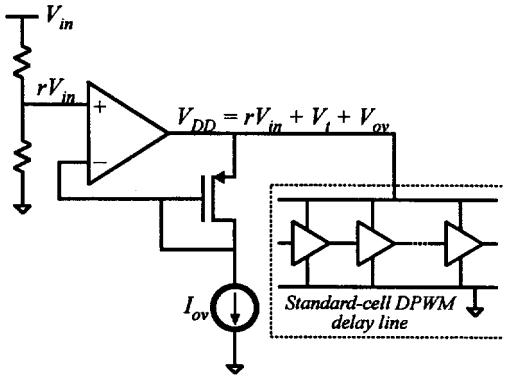


Figure 2. Feed-forward DPWM with standard-cell gates supplied from a scaled supply voltage.

be independent of the input voltage. From (1), it follows that the feed-forward compensation in the DPWM can be achieved if the cell delay t_d is inversely proportional to V_{in},

$$t_d = \frac{A}{V_{in}}, \tag{2}$$

where A is ideally a constant. In a step-down (buck) converter, the output quantization step V_{qDPWM} of the DPWM, i.e. the least-significant bit (LSB) value in volts, is given by $V_{in}\, t_d/T_s$, where $T_s = 1/f_s$ is the switching period. From (2), it follows that the FF-DPWM has a constant quantization step,

$$V_{qDPWM} = V_{in}\frac{t_d}{T_s} = \frac{A}{T_s}, \tag{3}$$

independent of the input voltage V_{in}. With the constant quantization step and the loop gain independent of the input voltage, the limit-cycle conditions [9] are also independent of the input voltage, which is another advantage of the feed-forward DPWM.

In contrast to the DPWM designs reported in [1-3], where the DPWM operates as a ring oscillator, the DPWM delay line in the configuration of Fig. 1 is driven by an external clock in an "open-loop" manner. This configuration allows simple synchronization to an external clock: the switching frequency f_s is equal to the external clock frequency. However, it should be noted that the cell delay and the length of the delay line must be selected so that the desired maximum output duty cycle is achievable under worst-case conditions. In the practical IC implementation based on the DPWM of Fig. 1, we assume that the clock frequency is constant, independent of the input voltage or other operating conditions.

B. *Delay cell design and feed-forward performance*

A number of possibilities exist to design a delay-line based DPWM to meet the objective (2). Three different ways are discussed in this section.

1) Standard-cell logic gate as the delay cell

As discussed in [2], there is a strong incentive to use standard-cell logic gates in the DPWM design: a standard-cell DPWM can be designed and realized using standard digital design flow based on HDL (hardware description language). The delay of a standard logic cell as a function of the supply voltage V_{DD} (which we assume is equal to the input voltage V_{in}) is given as:

$$t_d = \frac{k_d}{(V_{in} - V_t)^{\alpha}} \tag{4}$$

where α is typically between 1 and 2, V_t is the threshold voltage of CMOS devices, and k_d is a constant associated with a particular structure of the standard cell. Using (4), and assuming that $V_{DD} = V_{in}$, for a typical process with $V_t = 0.8$V and $\alpha = 1.5$, we find that the parameter A in (2) varies by a factor of 1.94 over the range of input voltages from 2.5 V to 5.0 V. In conclusion, although it is possible to use standard-cell logic gates without further modifications to build a feed-forward DPWM, the feed-forward performance over the expected range of input voltages is relatively poor. The threshold V_t offset in the delay characteristic (4) is the main reason the simplest standard-cell approach to FF-DWPM design may not have the desired performance.

2) Standard-cell logic gate with scaled supply voltage

To reduce the dependence on the V_t offset, it is possible to scale the supply voltage to the standard cells as shown in Fig 2. In this design, the supply voltage V_{DD} of the standard-cell DPWM delay line is:

$$V_{DD} = rV_{in} + V_t + V_{ov}, \tag{5}$$

which gives the relationship:

$$t_d = \frac{k_d}{(rV_{in} + V_{ov})^{\alpha}} \tag{6}$$

where $r < 1$ is a constant, and V_{ov} is a small overdrive voltage of the diode-connected PMOS device, which can be controlled by the I_{ov} bias current. This configuration allows one to make the parameter A in (2) almost constant over the entire V_{in} range by adjusting V_{ov} and r. In addition, the power consumption of the DPWM supplied from the reduced V_{DD} voltage is also reduced. A disadvantage associated with this approach is the requirement for an analog op-amp to generate the regulated V_{DD} and issues related to noise decoupling at the V_{DD} line in

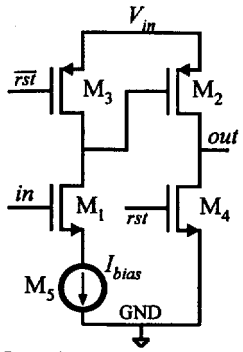


Figure 3. Configuration of the current starved delay cell.

the presence of current spikes generated by the DPWM logic gates supplied from V_{DD}.

3) Custom delay cell with current starving

This design relies on the adjustment of t_d by incorporating a current starved branch in the delay cell as shown in Figure 3. The desired objective of constant A in (2) can be obtained by sizing the devices M1 and M2, and the constant current sink (device M5). In order to get good DPWM linearity, the current sinks (M5) need to be matched from one delay cell to another. This is one of the potential design overheads with this scheme. Table I shows the simulation results for the effective DPWM quantization step obtained with the current starved delay cell for the typical and the worst-case process, temperature and input voltage corners. It can be observed that even under the worst-case process/temperature corners the FF-DPWM has an almost constant effective quantization step.

Out of above three approaches described in this section, the last one was selected for the design reported in this paper. A prototype test chip with the FF-DPWM circuit has been designed and fabricated. Experimental results are shown in Figure 4. Figure 4(a) shows the measured duty ratio of the output pulse as a function of the digital command, for three input voltages. Figure 4(b) shows how the product $V_{in}\,t_{on}$ stays approximately constant over the wide range of input voltages, which is an indication of good feed-forward compensation with the experimental FF-DPWM chip.

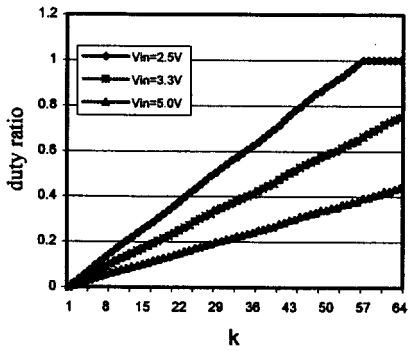
TABLE I. CELL DELAY t_d AND THE EFFECTIVE QUANTIZATION STEP V_{QDPWM} (FOR A 6-BIT DPWM WITH 2 BITS OF DITHER) FOR PROCESS/TEMPERATURE AND INPUT VOLTAGE CORNERS.

Temperature/ Process	Quantity	V_{in} = 2.5 V	V_{in} = 3.3 V	V_{in} = 5.5 V
T = -25°C/ Slow process	Delay of a unit cell [ns]	24.9	17.1	10.2
	FF-DWPM quantization step [mV]	15.6	14.1	12.8
T = +25°C/ Typical process	Delay of a unit cell [ns]	19.5	14.5	9.6
	FF-DWPM quantization step [mV]	12.2	12.0	11.9
T = +80°C/ Fast process	Delay of a unit cell [ns]	15.5	12.3	8.9
	FF-DWPM quantization step [mV]	9.7	10. 1	11.1

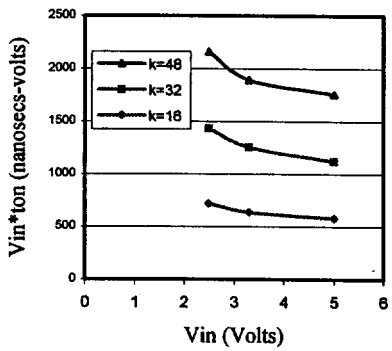
III. COMPLETE DIGITAL CONTROLLER WITH FEED-FORWARD COMPENSATION

The FF-DPWM is used to construct a complete digital PWM controller as shown in Figure 5. The controller architecture is similar to the digital PWM controller described in [2], but with several important modifications in the design of the A/D converter and the compensator, in addition to the new feed-forward DPWM described in Section II.

The A/D converter is a windowed flash converter [1], consisting of only two comparators. The output voltage is compared to the references $V_{ref} \pm V_q/2$, and the comparator outputs {x, y} are sampled to produce a digital error signal e. The digital error signal can take only three values: +1, 0 or –1, compared to the A/D reported in [2] where the errors in the range from –4 to +4 were allowed. Taking advantage of the minimum A/D range, the digital error signals from the current



(a)



(b)

Figure 4. Experimental results: (a) measured duty ratio of the output pulse as a function of the 6-bit digital command k, for three values of V_{in}: V_{in} = 2.5 V, V_{in} = 3.3 V, and V_{in} = 5 V; (b) Measured $V_{in}\,t_{on}$ product as a function of V_{in}, for three digital command inputs, k = 16, 32, and 48.

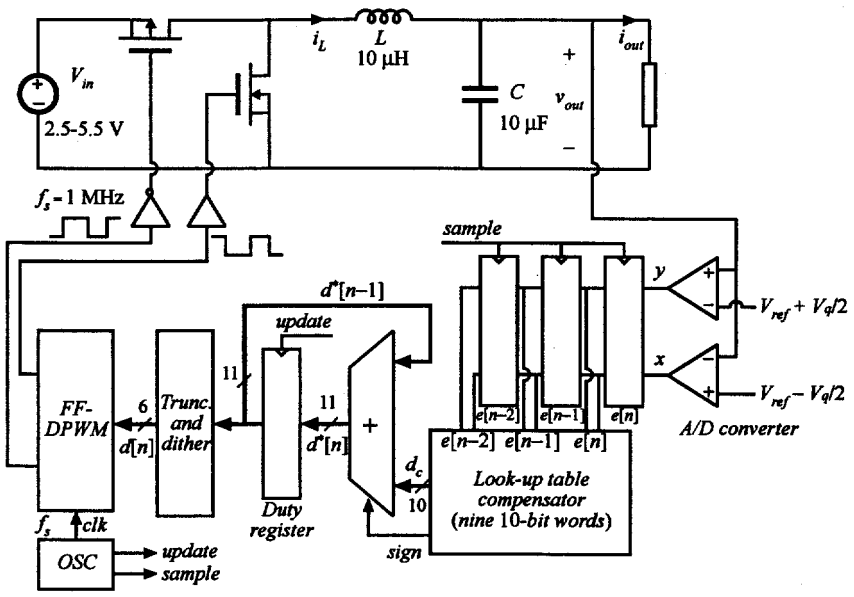


Figure 5. Digital controller with feed-forward DPWM in a battery-powered DC-DC conversion application.

and the two previous cycles are used with a *single* look-up table compensator to determine a correction d_c for the duty cycle. As a result, a single addition is required to compute the new duty-cycle command, compared to the implementation with three tables and three additions per period in [2]. The calculated duty cycle command d^* is then truncated to 6 bits and dithered using the technique described in [11] to achieve 8 bits of effective resolution with the 6-bit FF-DPWM described in Section II.

A. A/D converter

The A/D converter in the prototype chip is a flash converter having only two comparators. The conversion characteristic is shown in Figure 6. A small hysteresis (about 5 mV) around the transition points is added to improve the noise immunity. The output digital error signal e is 0 if the sensed output voltage is within $V_q/2$ around the reference V_{ref}. The error of +1 or –1 indicates that the output voltage is out of regulation. In closed-loop operation, the steady-state error is 0, which means that the dc output voltage is regulated in the $V_{ref} \pm V_q/2$ band. The converter and the compensator can be designed so that in transients the output voltage does not depart from the regulation by more than about V_q, which means that only three quantization levels are needed to represent the digital error signal. The comparators designed on the prototype chip and experimentally tested have about 300 ns delay, current consumption of about 15 µA, common-mode input voltage range from 0.8 V to V_{in}.

B. Look-Up Table Based Digital Compensator

The digital compensator can be designed in a number of ways including direct digital design techniques and digital redesign technique starting from a continuous–time compensator design [12]. In the design reported in this paper we used the pole-zero matching digital redesign technique [12, 13].

The continuous time control to output transfer function for a buck converter is given by [14]:

$$G_{vd}(s) = \frac{V_{in}}{1 + \frac{s}{Q\omega_0} + \left(\frac{s}{\omega_0}\right)^2}, \tag{7}$$

where

$$Q = R\sqrt{\frac{L}{C}} \quad \text{and} \quad \omega_0 = 2\pi f_0 = \frac{1}{\sqrt{LC}}. \tag{8}$$

The magnitude and phase responses of the control-to-output transfer function are shown in Fig. 7(a).

The compensator design starts from the continuous time equivalent $G_{cmp}(s)$ of a PID compensator:

$$G_{cmp}(s) = \frac{d^*(s)}{v_e(s)} = K_C \frac{1 + \frac{s}{Q_{cmp}\omega_z} + \frac{s^2}{\omega_z^2}}{s}, \tag{9}$$

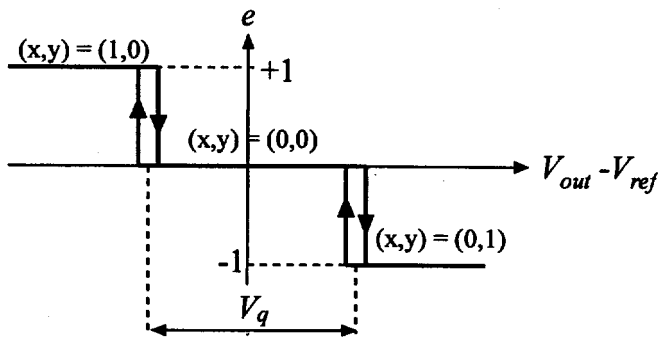


Figure 6. A/D converter characteristic.

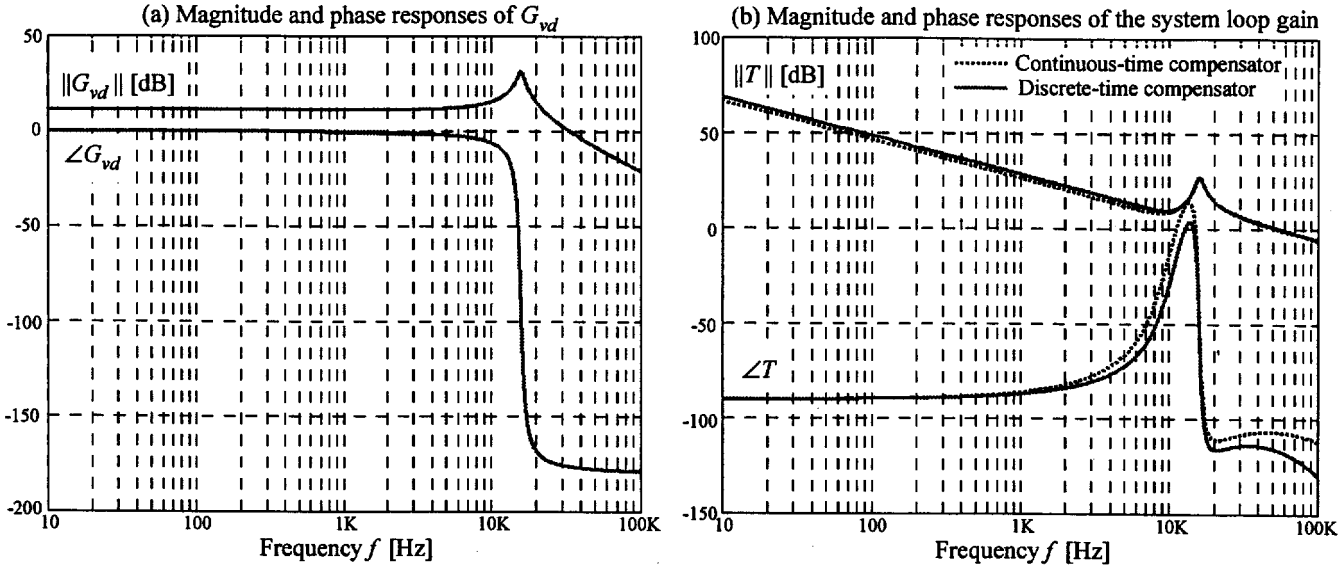


Figure 7. (a) Magnitude and phase responses of the converter control-to-output transfer function G_{vd}; (b) Magnitude and phase responses of the system loop gain using the continuous-time compensator and the digital discrete-time compensator.

where the parameter $Q_{cmp} = 1.27$, the zero frequency $f_z = \omega_z/2\pi = 10.4$ kHz, and the gain $K_c = 38$ krad/s are adjusted to achieve the desired cross-over frequency (about 55 kHz) and phase margin (about 60°), taking into account the delay of about $T_s/2$ from the time the output voltage is sampled to the time the duty cycle of the gate-drive pulse is updated, and using. $V_{in} = 3.6$ V.

The discrete-time equivalent of the PID compensator has the following form [2,13]:

$$d^*[n] = d^*[n-1] + ae[n] + be[n-1] + ce[n-2], \qquad (10)$$

where $e[n]$, $e[n\text{-}1]$, $e[n\text{-}2]$ are the digital error signals, $d^*[n\text{-}1]$ is the digital duty-cycle command stored from the previous cycle, and $d^*[n]$ is the current duty cycle command. The compensator coefficients a, b and c are found from (9) following the pole-zero matching method [12,13]:

$$r = \exp\left(-\frac{\pi f_z}{Q_{comp} f_{sw}}\right) \qquad (11)$$

$$b = -a \cdot 2r \cdot \cos\left(2\pi \frac{f_z}{f_{sw}}\right) \qquad (12)$$

$$c = a \cdot r^2 \qquad (13)$$

The value of the coefficient a is determined such that the magnitude response of the discrete-time implementation approximately matches the magnitude response of the continuous-time compensator (9) at the desired crossover frequency f_c. With the digital error signal represented as –1, 0, or +1, we take into account the A/D converter gain of $1/V_q = 33.3$ for $V_q = 30$ mV. The resulting discrete-time compensator parameters are:

$$a = 0.29199,\ b = -0.56787,\ c = 0.27734 \qquad (14)$$

Figure 7(b) shows the magnitude and phase responses of the system loop gain for the continuous-time compensator $G_{cmp}(s)$ in (9), and for the discrete-time digital compensator defined by (10) and (14).

In [2], to implement the discrete-time compensator

TABLE II. LOOK-UP TABLE COMPENSATOR DESIGN. THE DUTY-CYCLE CORRECTION IS THE 10-BIT TABLE ENTRY (LAST COLUMN) DIVIDED BY 512.

Table index	e[n]	e[n-1]	e[n-2]	$512(d_e)$	10-bit table entry
1	-1	-1	-1	-0.75	-1
2	-1	-1	0	141.25	141
3	-1	-1	1	283.25	0
4	-1	0	-1	-291.50	-292
5	-1	0	0	-149.50	-150
6	-1	0	1	-7.50	-7
7	-1	1	-1	-582.25	0
8	-1	1	0	-440.25	0
9	-1	1	1	-298.25	0
10	0	-1	-1	148.75	149
11	0	-1	0	290.75	291
12	0	-1	1	432.75	0
13	0	0	-1	-142.00	-142
14	0	0	0	0.00	0
15	0	0	1	142.00	142
16	0	1	-1	-432.75	0
17	0	1	0	-290.75	-291
18	0	1	1	-148.75	-149
19	1	-1	-1	298.25	0
20	1	-1	0	440.25	0
21	1	-1	1	582.25	0
22	1	0	-1	7.50	7
23	1	0	0	149.50	150
24	1	0	1	291.50	292
25	1	1	-1	-283.25	0
26	1	1	0	-141.25	-141
27	1	1	1	0.75	1

computation (10), three look-up tables were used to store the pre-computed products $ae[n]$, $be[n\text{-}1]$, and $ce[n\text{-}1]$ for all possible values of the error signal in the range from –4 to +4. In the design reported in this paper, we take advantage of the minimum A/D range where the errors $e[n]$, $e[n\text{-}1]$, $e[n\text{-}2]$ can take one of only three possible values, –1, 0, or +1. The computation of the duty-cycle correction,

$$d_c = ae[n] + be[n-1] + ce[n-2], \qquad (15)$$

is performed using a *single* look-up table addressed by the three digital error signals. In the construction of the table, we can make a trade-off between the lengths of the entries and the precision of the stored values [13]. Table II illustrates the construction of the look-up table implemented on the test chip. The table entries are 10-bit values, with one bit representing the sign (the two's complement is used to store positive and negative values). Given that there are three error signals, each with three possible values, there are a total of 27 possible values for the duty cycle correction d_c. The fifth column ($512\,d_c$) shows the correction value (scaled by $2^9 = 512$), computed from (14) and (15). The actual table entries are shown in the last column of Table II. The values are rounded to the closest integer in order to fit into the 10-bit table entries. The table size is further reduced by noting that the entries with the indices 27 to 15 are the same as the entries with the indices 1 to 13, except for the sign. Instead of storing the entries 15 to 27 in the table, the adder is extended to perform addition or subtraction of the duty-cycle correction depending on the sign, as shown in the diagram of Fig. 5. Finally, an additional step in the table design includes eliminating the entries corresponding to the sequence of error values that should never occur during transients. As seen in Table II, the entries with indices 3, 7, 8, 9, and 12 are assigned the default value of $d_c = 0$, instead of the values computed from (14) and (15). The final complete look up table includes only nine 10-bit values shown in bold in the last column of Table II. Using the look-up table to compute the duty-cycle correction $d_c[n]$, the duty cycle command $d[n]$ is then found as:

$$d^*[n] = d^*[n-1] + d_c[n], \qquad (16)$$

$$d[n] = \text{Truncate and dither}(d^*[n]). \qquad (17)$$

In the truncate and dither step, the 11-bit signed value of $d^*[n]$ is first truncated to a 6-bit unsigned value corresponding to the duty cycle command between 0 and 1. Then, a dither scheme described in [11] is applied to extend the effective DPWM resolution. In our test chip, the number of dither bits (0, 1, 2, or 3) is selectable by a two-bit external digital input, to allow experimentation with different effective DPWM resolutions.

The compensator, including the truncate and dither functions was designed using Verilog hardware description language. The complete prototype chip takes about one fourth of the silicon area and power of the design reported in [2]. The layout of the chip submitted for fabrication is shown in Figure 8.

IV. Application Example

The digital PWM controller chip described in Section III can be used in a wide range of DC-DC applications. A particular application considered here is shown in Fig. 5: a low-power 1 MHz buck DC-DC converter supplied from a Lithium-Ion battery ($2.5\text{ V} < V_{in} < 5.5\text{ V}$), and producing a regulated output voltage of $V_{out} = 1.5$ V at the load current of up to 300 mA.

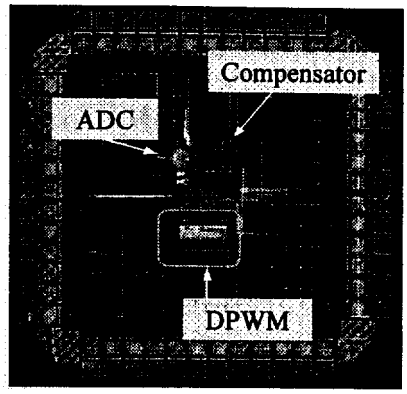


Figure 8. Layout of the prototype digital PWM controller chip with feed-forward compensation in 0.5 μ CMOS. The active chip area is 0.3 mm^2

Mixed-signal simulation results illustrating start-up and load transients are shown in Figure 9. It can be observed that the system includes a soft start feature: upon start-up, the error voltage is large, and the digital error signal is saturated at $e = +1$. As a result, the compensator exhibits a "slew-rate" limited response where the duty cycle is gradually increased from 0 to the steady-state value. The load transient response is relatively fast. Even during relatively large load transients (50% to 100%), the output voltage error stays so small that minimum-range two-comparator A/D converter is sufficient to

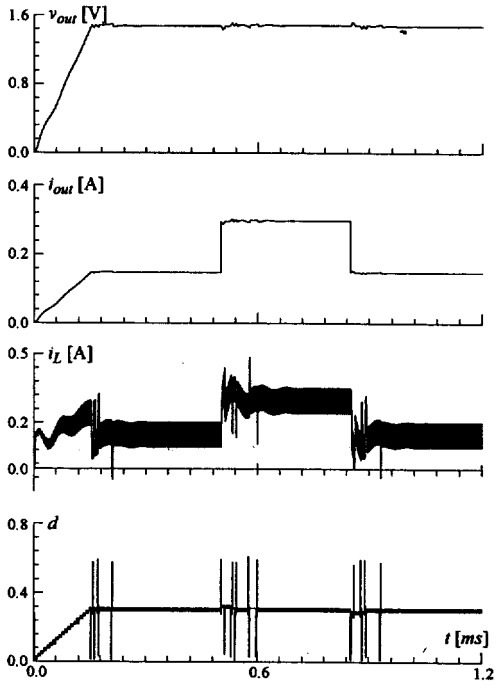


Figure 9. Start-up and 50-100% load transient waveforms obtained by mixed-signal simulation of the closed-loop regulator shown in Fig. 5; $V_{in} = 5$ V, $V_{ref} = 1.5$ V, $V_q = 30$ mV. Top-to-bottom: the output voltage v_{out}, the load current i_{out}, the inudctor current i_L, and the duty cycle command d.

adequately produce the digital error signal. Increasing the A/D conversion range by increasing the number of comparators would not improve the load transient response.

Figure 10 shows mixed signal simulation results for the line transient response of the DC-DC converter with and without feed-forward compensation. As evident from the figure feed-forward DPWM almost completely rejects any transient in the line voltage.

V. Conclusion

This paper describes a complete digital PWM controller IC with feed-forward compensation of the input voltage. The feed-forward compensation is accomplished through a delay-line digital pulse-width modulator (DPWM) where the cell delay is made inversely proportional to the input voltage. The complete digital controller IC with the feed-forward DPWM operating at 1 MHz switching frequency can be used in a range of DC-DC applications. In particular, low power consumption, small controller area (less than 0.25 mm^2 in a standard 0.5μ CMOS process) and a programmable compensator requiring no external passive components, are well suited for DC-DC conversion in low-power battery-operated devices. Experimental results are presented for the feed-forward DPWM. Mixed-signal simulation results for the complete chip show excellent performance under start-up, load and line transients.

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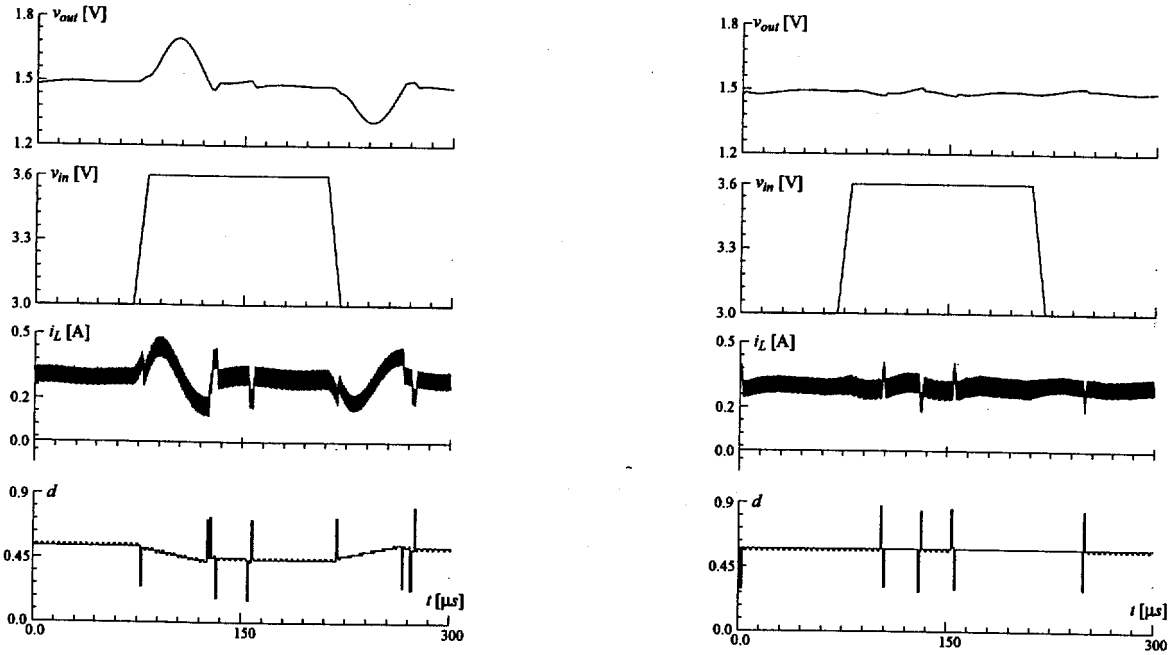

(a) DPWM without feed-forward compensation

(b) DPWM with feed-forward compensation

Figure 10. Line voltage transient waveforms obtained by mixed-signal simulation in the voltage regulator of Fig. 5 with: (a) DPWM without feed forward; (b) feed-forward DPWM; V_{in} undergoes a transient from 3.0V to 3.6V and comes back to 3.0V, V_{ref} = 1.5 V, V_q = 30 mV, load current 300mA. Top-to-bottom: the output voltage v_{out}, the input voltage v_{in}, the inudctor current i_L, and the duty cycle command d.

computation (10), three look-up tables were used to store the pre-computed products $ae[n]$, $be[n-1]$, and $ce[n-1]$ for all possible values of the error signal in the range from –4 to +4. In the design reported in this paper, we take advantage of the minimum A/D range where the errors $e[n]$, $e[n-1]$, $e[n-2]$ can take one of only three possible values, –1, 0, or +1. The computation of the duty-cycle correction,

$$d_c = ae[n] + be[n-1] + ce[n-2], \qquad (15)$$

is performed using a *single* look-up table addressed by the three digital error signals. In the construction of the table, we can make a trade-off between the lengths of the entries and the precision of the stored values [13]. Table II illustrates the construction of the look-up table implemented on the test chip. The table entries are 10-bit values, with one bit representing the sign (the two's complement is used to store positive and negative values). Given that there are three error signals, each with three possible values, there are a total of 27 possible values for the duty cycle correction d_c. The fifth column ($512\ d_c$) shows the correction value (scaled by $2^9 = 512$), computed from (14) and (15). The actual table entries are shown in the last column of Table II. The values are rounded to the closest integer in order to fit into the 10-bit table entries. The table size is further reduced by noting that the entries with the indices 27 to 15 are the same as the entries with the indices 1 to 13, except for the sign. Instead of storing the entries 15 to 27 in the table, the adder is extended to perform addition or subtraction of the duty-cycle correction depending on the sign, as shown in the diagram of Fig. 5. Finally, an additional step in the table design includes eliminating the entries corresponding to the sequence of error values that should never occur during transients. As seen in Table II, the entries with indices 3, 7, 8, 9, and 12 are assigned the default value of $d_c = 0$, instead of the values computed from (14) and (15). The final complete look up table includes only nine 10-bit values shown in bold in the last column of Table II. Using the look-up table to compute the duty-cycle correction $d_c[n]$, the duty cycle command $d[n]$ is then found as:

$$d^*[n] = d^*[n-1] + d_c[n], \qquad (16)$$

$$d[n] = \text{Truncate and dither}(d^*[n]). \qquad (17)$$

In the truncate and dither step, the 11-bit signed value of $d^*[n]$ is first truncated to a 6-bit unsigned value corresponding to the duty cycle command between 0 and 1. Then, a dither scheme described in [11] is applied to extend the effective DPWM resolution. In our test chip, the number of dither bits (0, 1, 2, or 3) is selectable by a two-bit external digital input, to allow experimentation with different effective DPWM resolutions.

The compensator, including the truncate and dither functions was designed using Verilog hardware description language. The complete prototype chip takes about one fourth of the silicon area and power of the design reported in [2]. The layout of the chip submitted for fabrication is shown in Figure 8.

IV. Application Example

The digital PWM controller chip described in Section III can be used in a wide range of DC-DC applications. A particular application considered here is shown in Fig. 5: a low-power 1 MHz buck DC-DC converter supplied from a Lithium-Ion battery ($2.5\ \text{V} < V_{in} < 5.5\ \text{V}$), and producing a regulated output voltage of $V_{out} = 1.5$ V at the load current of up to 300 mA.

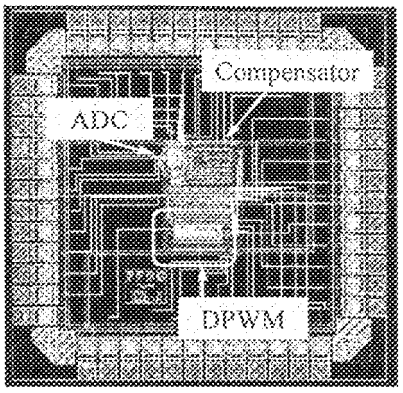

Figure 8. Layout of the prototype digital PWM controller chip with feed-forward compensation in 0.5 μ CMOS. The active chip area is 0.3 mm^2.

Mixed-signal simulation results illustrating start-up and load transients are shown in Figure 9. It can be observed that the system includes a soft start feature: upon start-up, the error voltage is large, and the digital error signal is saturated at $e = +1$. As a result, the compensator exhibits a "slew-rate" limited response where the duty cycle is gradually increased from 0 to the steady-state value. The load transient response is relatively fast. Even during relatively large load transients (50% to 100%), the output voltage error stays so small that minimum-range two-comparator A/D converter is sufficient to

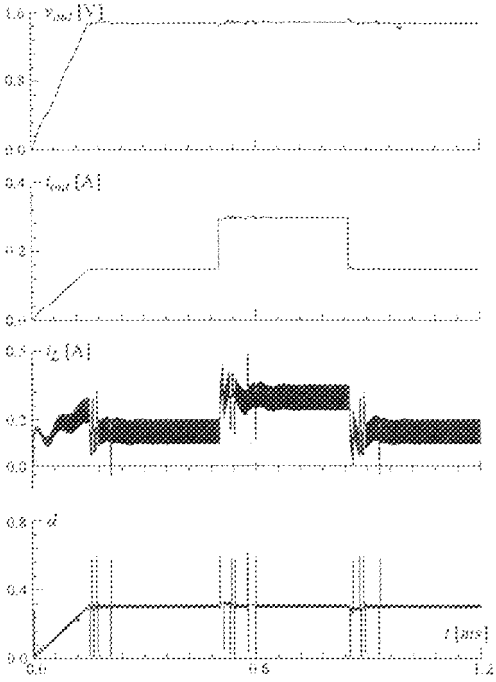

Figure 9. Start-up and 50-100% load transient waveforms obtained by mixed-signal simulation of the closed-loop regulator shown in Fig. 5; $V_{in} = 5$ V, $V_{ref} = 1.5$ V, $V_q = 30$ mV. Top-to-bottom: the output voltage v_{out}, the load current i_{out}, the inductor current i_L, and the duty cycle command d.