Characterization of an Active Clamp Flyback Topology for Power Factor Correction Applications

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***Abstract*—Flyback derived topologies have long been attractive because of their relative simplicity when compared with other topologies used in low-power applications. Incorporation of active clamp circuitry provides the additional benefit of recycling transformer leakage energy while minimizing switch voltage stress. This paper presents the analysis, design, and experimental results of 500 W single stage and 600 W interleaved active clamp flybacks used for power factor correction. Several practical issues, including the application of charge control, the use of mixed power devices, and a solution to the hold-up time problem are discussed and experimentally verified.**

I. Introduction

THE flyback topology is suitable for achieving power factor correction, isolation, and bus voltage regulation using only one power conversion step. In addition, the active switch is in series with the input, allowing simple inrush current limiting and overcurrent protection. As a result, the flyback configuration is an attractive alternative to the conventional two-stage scheme typically used in power distribution systems.

A drawback to the use of the flyback is the relatively high voltage and current stress suffered by its switching components. Utilization of charge control methods [1] allow for operation over a larger portion of the input line in continuous conduction mode (CCM), thereby reducing device peak current stress. Also, by incorporating mixed power devices into the flyback switch, increased power levels can be processed without incurring a severe penalty in conversion efficiency. Switch voltage stress can be minimized by incorporation of an active clamp circuit that serves to limit the turn-off voltage spike while recycling the flyback transformer leakage energy [5].

This paper presents evaluation of the active clamp flyback converter for PFC applications in distributed power systems. Experimental results for both single-stage (to 500 W) and interleaved (to 600 W) designs are presented. A solution to the hold-up problem is also presented and experimentally verified. Flyback interleaving significantly reduces input filter requirements over single-stage designs by introducing 180° out-of-phase input current harmonics, resulting in a reduction of input current ripple.

Manuscript received June 14, 1995; revised July 21, 1995. This work was supported in part by Delta Electronics Company and Zytec Corporation.

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Publisher Item Identifier S 0885-8993(96)00607-2.

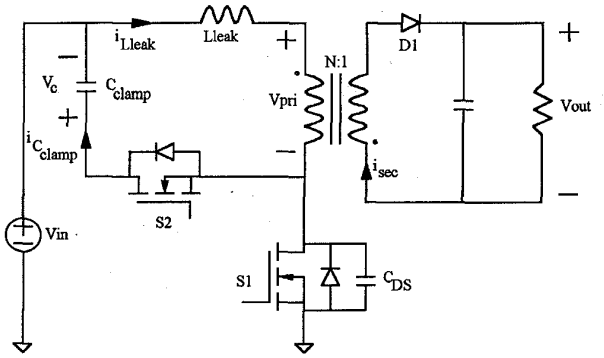

Fig. 1. Simplified schematic of the active clamp flyback converter.

II. Active Clamp Flyback Converter Overview

The incorporation of an active clamp circuit into the basic flyback topology is shown in Fig. 1. Here L_{leak} represents the total transformer leakage inductance reflected to the primary. With the active clamp circuit, the transistor turn-off voltage spike is clamped, the transformer leakage energy is recycled, and zero-voltage-switching (ZVS) for both primary (S1) and auxiliary (S2) switches becomes a possibility. These advantages come at the expense of additional power stage components and increased control circuit complexity.

Fig. 2 shows the topological states and Fig. 3 the key waveforms for the active clamp flyback converter. For steady-state operation and unidirectional magnetizing current, assuming L_{leak} is much less than the transformer magnetizing inductance, L_m, and $\pi\sqrt{L_{\text{leak}}C_{\text{clamp}}} \gg T_{\text{off}}$, the sequence of topological states is as follows:

$T_0 - T_1$: At T_0, switch S1 is on, and the auxiliary switch, S2, is off. The output rectifier, D1, is reversed biased, as is the antiparallel diode of S2. The magnetizing and leakage inductances are being linearly charged, just as they would be during the inductor charging phase in "normal" flyback operation.

$T_1 - T_2$: S1 is turned off at T_1. C_{DS} is charged by the magnetizing current (which is also equal to the current through the leakage inductance). C_{DS} is actually charged in a resonant manner, but the charge time is very brief, leading to an approximately linear charging characteristic.

$T_2 - T_3$: At T_2, C_{DS} is charged ($V_{\text{DS}} = V_{\text{in}} + V_c$) to the point where the antiparallel diode of S2 starts to conduct. The clamp capacitor fixes the voltage across L_{leak} and the transformer magnetizing inductance to $V_C(\cong NV_o)$, forming a voltage divider between the two inductances. Since C_{clamp}

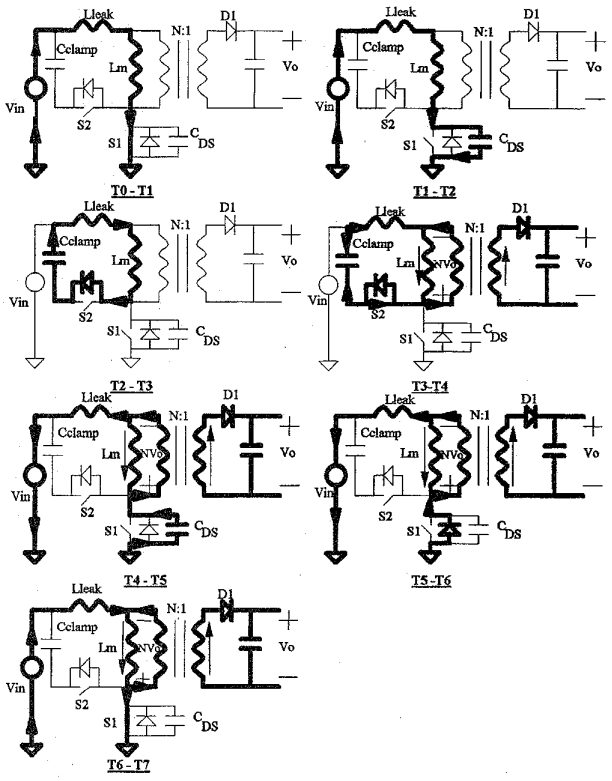

Fig. 2. Active clamp flyback topological states.

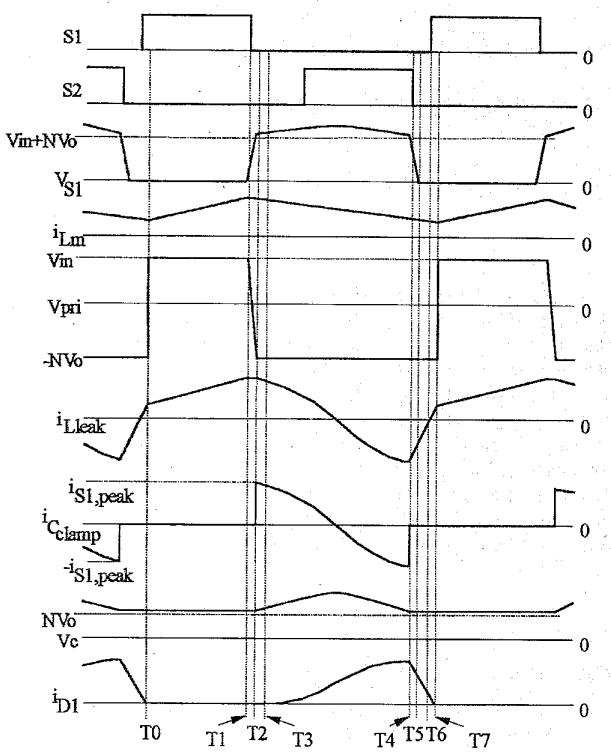

Fig. 3. Active clamp flyback steady-state waveforms.

is much larger than C_{DS}, nearly all of the magnetizing current is diverted through the diode to the clamp capacitor.

$T_3 - T_4$: At T_3, V_{pri} has decreased to the point where the secondary transformer voltage is sufficient to forward bias D1. The transformer primary voltage is then clamped by the secondary to approximately NV_o. L_{leak} and C_{clamp} begin to resonate. S2 is turned on during this interval to allow the resonating clamp capacitor current to reverse direction.

$T_4 - T_5$: The auxiliary switch, S2, is turned off at T_4, effectively removing C_{clamp} from the circuit. A new resonant network is formed between the leakage inductance and the MOSFET drain-to-source capacitance. The transformer primary voltage remains clamped at NV_o as C_{DS} is discharged.

$T_5 - T_6$: Assuming the energy stored in L_{leak} is greater than the energy stored in C_{DS}, at T_5 C_{DS} will be sufficiently discharged to allow S1's body diode to start conducting. The voltage across the leakage inductance becomes clamped at $V_{in} + NV_o$. It is during this interval that switch S1 can be turned on under zero voltage conditions.

$T_6 - T_7$: S1 is on, and the secondary current is decreasing as the leakage inductor current increases. At T_7, the secondary current reaches zero (because the leakage inductor current has equaled the magnetizing current), and D1 reverse biases, allowing the polarity to reverse on the transformer primary. The magnetizing and leakage inductances begin to linearly charge again, starting another switching cycle ($T_7 = T_0$).

Note that the length of the time intervals, T_1 to T_3 and T_4 to T_7, have been greatly exaggerated in Fig. 3 in order to more clearly show the transition periods.

III. Active Clamp Flyback for PFC Applications

For PFC applications, the active clamp flyback offers essentially the same advantages as for dc/dc conversion applications. The method of charge control [1] can be applied for "CCM" (unidirectional magnetizing current) operation, reducing component current stress, and increasing power processing capabilities. Fig. 4 shows a block diagram and the basic waveforms pertinent to charge control. This PFC control method forces the input charge to follow an input line replica reference pulse by pulse, resulting in a sinusoidal input current waveform. The switching frequency is constant, and (because of the integrating capacitor) the control scheme offers good immunity from switching noise.

IV. 500 W Active Clamp Power Stage Design

A. PFC Specifications

To determine the feasibility of using the active clamp flyback in PFC applications, a single-stage converter operating at 70 KHz was built to the following I/O specifications:

- input: 90–270 V rms (Universal Line);
- output: 48 VDC nominal; and
- output power: 500 W maximum.

B. Primary Switch Selection

1) Transformer Turns Ratio Selection: The transformer turns ratio is selected to accommodate as low a voltage-rated device as possible while still being able to realize reasonable values for the range of minimum duty cycles.

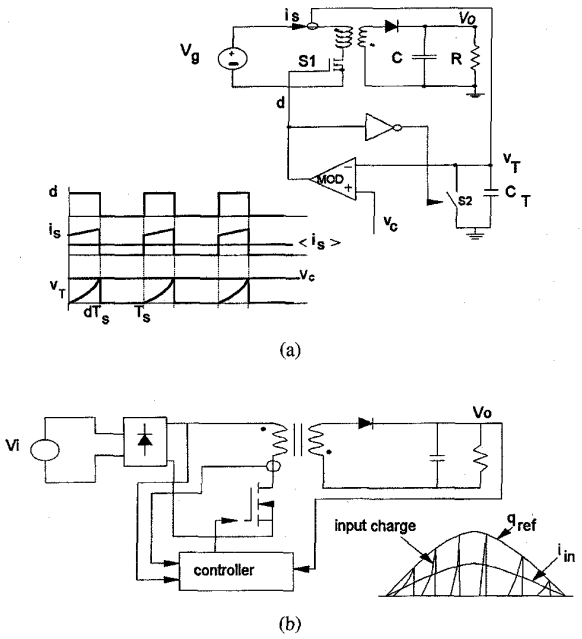

Fig. 4. Charge control method. (a) Switching frequency waveforms. (b) Line frequency waveforms.

Assuming initially that the active clamping provides for perfect suppression of the leakage spike appearing across the main switch (i.e., no overshoot), then the maximum off-state voltage appearing across S1 is given by

$$V_{\mathrm{S1,max}} = \sqrt{2}V_{\mathrm{rms}}^{HL} + NV_o \tag{1}$$

where N is the transformer turns ratio ($= N_P/N_S$) and V_o is the output voltage ($=$ 48 VDC). The range of the minimum duty cycle is given by

$$D_{\min}^{LL} = \frac{V_o}{V_o + \dfrac{\sqrt{2}V_{\mathrm{rms}}^{LL}}{N}} \tag{2}$$

$$D_{\min}^{HL} = \frac{V_o}{V_o + \dfrac{\sqrt{2}V_{\mathrm{rms}}^{HL}}{N}}. \tag{3}$$

For the 500 W design, the turns ratio was selected to be 3, which resulted in a peak voltage stress of 526 V for S1. Therefore, a 600 V device can be used. The minimum duty cycle ranges from 0.53 at minimum line to 0.27 at high line.

2) Calculating Primary Switch Currents: The maximum average current seen by S1 over one switching cycle occurs at maximum load and minimum line voltage (assuming approximately unity power factor) and is given by

$$I_{\mathrm{S1,avg}}^{\max} = \frac{P_o^{FL}\sqrt{2}}{\eta V_{\mathrm{rms}}^{LL}} \tag{4}$$

where η is the converter efficiency at the maximum output power, minimum line operating condition. Assuming an efficiency of 85% at full load and minimum line, the maximum average switch current is 9.2 A. The worst case maximum peak switch current also occurs under the same operating conditions

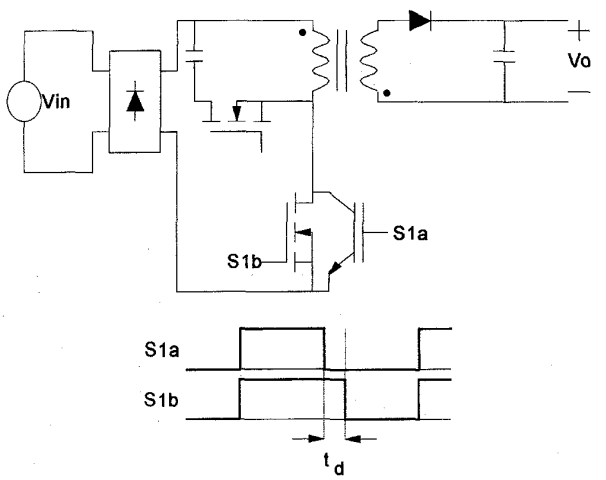

Fig. 5. Basic concept of mixed power devices.

as above and is calculated from

$$I_{\mathrm{S1,peak}}^{\max} = \frac{P_o^{FL}\sqrt{2}}{\eta D_{\min}^{LL} V_{\mathrm{rms}}^{LL}} + \frac{D_{\min}^{LL} V_{\mathrm{rms}}^{LL}\sqrt{2}}{2L_m F_S} \tag{5}$$

where L_m is the flyback transformer magnetizing inductance and F_S is the switching frequency. For this particular design, with a 20% peak-to-peak ripple current at low line, full load, $L_m \cong 220\ \mu$H. Assuming $\eta = 0.85$, the resulting peak switch current is about 19.6 A.

These calculated switch currents preclude using a single MOSFET for S1. The alternatives are to parallel MOSFET's or parallel IGBT's and MOSFET's to form a mixed device switch.

3) Device Paralleling: The limiting factor in being able to switch an IGBT at higher frequencies is the presence of a collector current tail at device turn-off, resulting in excessive switching losses. As shown in Fig. 5, the paralleling of a MOSFET with an IGBT, acting as a single switch, enables the IGBT to be turned off without the simultaneous presence of high collector voltage and current [2]. The MOSFET is left on for a sufficient length of time after the IGBT has been turned off (about 750 ns in the case of the IGBT selected for use in this circuit) to allow the collector current to reach zero before the collector voltage is allowed to rise. Because the on-state voltage drop of the IGBT is typically lower than for the MOSFET, the strengths of both types of switches are taken advantage of in this type of arrangement. Fig. 6 displays the dc/dc conversion efficiencies for a dual MOSFET switch (IRFPC40), a single IGBT switch (IRGPC40U), and the mixed device switch as a function of output power. All measurements were made at 90 VDC input to approximate the worst-case low-line operating condition.

C. Clamp Circuit Design

1) Auxiliary Switch Selection: The active clamp switch (S2) consists of a diode in series with the MOSFET to prevent conduction of the slow MOSFET body diode and an antiparallel fast recovery rectifier (FRR) to replace it. This is necessary because if the main switch (S1) is turned on

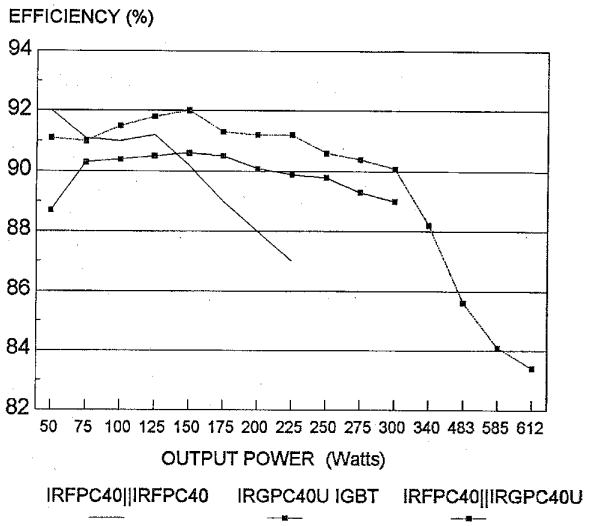

Fig. 6. Experimental active clamp flyback dc/dc efficiencies. $V_{\text{in}} = 90$ VDC and $F_S = 90$ KHz for all three curves.

while S2's body diode is conducting (e.g., during a transient condition), there is a good chance destruction of the MOSFET will result. The voltage rating of both the MOSFET and fast recovery rectifier is the same as for switch S1, 600 V in this design.

For the purposes of estimating the required current ratings of the devices comprising S2, assume that the $L_{\text{leak}} - C_{\text{clamp}}$ resonant period is much longer than the off-time of S1. In this case, the current through S2 approximates a sawtooth waveform with endpoint currents equal to the peak current through S1 (see Fig. 3). Therefore, the worst-case maximum RMS current seen by both the FRR and the MOSFET (averaged over one switching cycle) is approximately

$$I_{\text{S2,rms}}^{\max} \approx I_{\text{S1,peak}}^{\max}\sqrt{\frac{1 - D_{\min}^{LL}}{6}}. \tag{6}$$

For this design, the maximum RMS current is about 5.5 A. In practice, (6) is somewhat conservative and the RMS current through S2 will be less than calculated (especially if the $L_{\text{leak}} - C_{\text{clamp}}$ resonant period is less than assumed above). Also, in PFC applications, device power dissipation is modulated at a frequency of 120 Hz. The junction-to-case thermal time constant of the device will determine how closely (4), (6), and (12) approximate a steady-state power dissipation condition.

2) Clamp Capacitor Selection: Selection of the clamp capacitor value is somewhat empirical and is done based on the value of leakage and stray inductance resulting from transformer and circuit board construction. The resonant frequency formed by the clamp capacitor and transformer leakage inductance should be sufficiently low so that there is not excessive resonant ringing (and hence voltage overshoot) across the power switch when the switch is turned off. However, too large a value for the clamp capacitor yields no improvement in clamping performance at the expense of a larger (more costly and bulky) capacitor. A good compromise for design purposes is to select the capacitor value so that one-half of the resonant period formed by the clamp capacitor and transformer leakage inductance exceeds the maximum off time of S1. Therefore

$$C_{\text{clamp}} \approx \frac{(1 - D_{\min}^{HL})^2}{\pi^2 L_{\text{leak}} F_S^2}. \tag{7}$$

With the transformer leakage inductance measuring out at about 4 μH, the calculated value of clamp capacitance is 2.8 μF (with the switching frequency at 70 KHz). After breadboard experimentation a value of 2 μF was settled on (values between 0.47 μF and 2 μF yielded good results). The capacitor voltage rating has to exceed NV_o, which is approximately 150 V in this design. Therefore, a 250 V part is used to provide some margin. The required ripple current rating for the capacitor is

$$I_{C\text{clamp,rms}}^{\max} \approx \frac{P_o^{\max}}{\eta N V_o}\sqrt{\frac{2\sqrt{2}NV_o}{3\pi V_{\text{rms}}^{LL}} + \frac{3}{8}}. \tag{8}$$

This gives about 3.8 A rms for this design.

D. Transformer Design

The transformer design for the active clamp flyback is no different than that for a traditional flyback, except that for PFC applications, the peak switch current is larger than for dc/dc applications (assuming $V_{\text{in,dc/dc}} = V_{\text{in,rms,PFC}}$).

For the 500 W design, a Toshiba PC40ETD49-Z core was selected and wound with 45 primary turns of three strands of 150/42 Litz wire. The secondary consisted of 15 turns of five strands of 150/42 Litz wire. The primary and secondary windings were interleaved, and the core was gapped to obtain a magnetizing inductance of about 220 μH. For the purposes of selecting wire size, the maximum primary and secondary RMS current are

$$I_{\text{pri,rms}}^{\max} \approx \frac{P_o^{\max}}{\eta N V_o V_{\text{rms}}^{LL}} \cdot \sqrt{\frac{10\sqrt{2}NV_oV_{\text{rms}}^{LL}}{3\pi} + (NV_o)^2 + \frac{3}{8}(V_{\text{rms}}^{LL})^2} \tag{9}$$

and

$$I_{\text{sec,rms}}^{\max} \approx \frac{P_o^{\max}}{V_o}\sqrt{\frac{3}{2} + \frac{16NV_o}{3\pi\sqrt{2}V_{\text{rms}}^{LL}}}. \tag{10}$$

In this design, the maximum primary and secondary currents are about 9.4 A rms and 19.3 A rms, respectively.

E. Output Stage Design

1) Output Rectifier Selection: The maximum theoretical reverse voltage seen by the output rectifier is given by

$$V_{\text{D1,max}} = \frac{\sqrt{2}V_{\text{rms}}^{HL}}{N} + V_o \tag{11}$$

which is 175 V in this case. For design margin, a 300 V part can be used. The maximum average current (averaged over one switching cycle) through the output rectifier is

$$I_{\text{D1,avg}}^{LL,FL} = \frac{2P_o}{V_o}. \tag{12}$$

This calculates to about 20.8 A for the 500 W design. Because of the operation of the clamp circuit, the rectifier current appears "discontinuous" even though the flyback inductor operating with unidirectional current (see Fig. 3). As a result, peak secondary currents are quite high

$$I_{\mathrm{D1,peak}}^{\max} \approx \frac{4P_o}{(1-D_{\min}^{LL})V_o}. \tag{13}$$

The worst case value in this design example is about 89 A. Because of the quasi-resonant nature of the current through the rectifier, the peak won't be quite this high, but it is much greater than the peak rectifier currents seen in a nonactive clamp flyback operating in CCM.

2) Output Capacitor Selection: The principal factor affecting the selection of the output capacitor is the output voltage ripple specification. C_o is selected to achieve some maximum 120 Hz voltage ripple

$$C_o = \frac{P_o^{\max}}{240\pi V_o V_{or}} \tag{14}$$

where V_{or} is the maximum specified peak output voltage ripple. For a 6 V pp ripple, $C_o \cong 4700$ pF. The required ripple current rating for the output capacitor is given by

$$I_{C_o,\mathrm{rms}}^{\max} = \frac{P_o^{\max}}{\sqrt{2}V_o}. \tag{15}$$

This gives a 120 Hz ripple current component of 7.4 A rms for a 500 W, 48 V output.

F. Experimental Results

Fig. 7 graphs the efficiency versus output power of the single-stage active clamp PFC flyback at the minimum input line (90 V rms). This is the worst-case operating condition with respect to efficiency. The power switch consists of an IRFPC50 MOSFET in parallel with an IRFGPC40U IGBT. The efficiency remains above 83.5% up to 500 W but falls fairly rapidly between 500 and 550 W. The major loss at the high end of output power is transformer copper loss. The efficiency could be improved through a more careful design of the transformer. Fig. 8 shows experimental waveforms of the line current and rectified line voltage at 550 W. The power factor remained above 0.98 over the full load range (to 550 W).

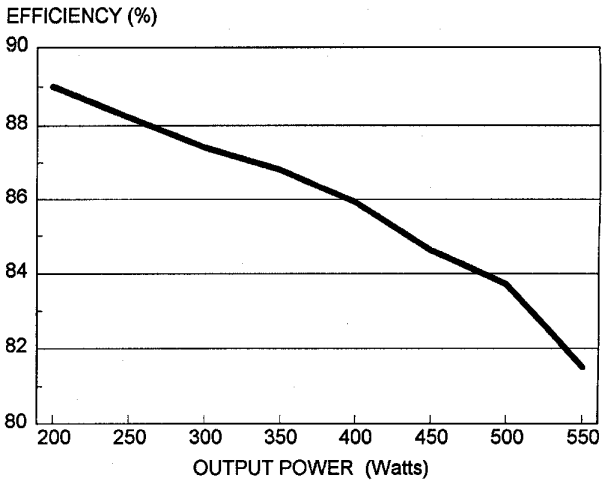

Fig. 7. Active clamp flyback PFC efficiency, $V_{\mathrm{in}} = 90$ V rms.

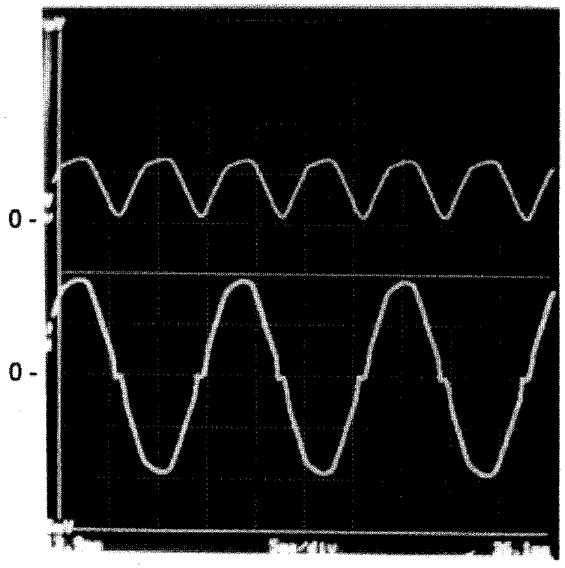

Fig. 8. Active clamp flyback experimental waveforms. Top trace: rectified line voltage @ 100 V/div; bottom trace: line current @ 5 A/div. $P_o = 550$ W.

V. Interleaved Active Clamp Flyback PFC

One of the limitations of the flyback converter is the discontinuous nature of the input current, which results in a large-sized EMI filter (when compared to a topology offering continuous input current operating at similar power levels). To minimize this problem, an interleaved active clamp flyback PFC configuration has been tested up to a 600 W output. The circuit design is similar to that of the single-stage flyback PFC circuit and differs from the interleaved active clamp flyback circuit described in [4] by the difference in behavior of the transformer magnetizing current. In [4] inductor ripple current is deliberately increased to always yield a portion of the switching cycle where the magnetizing current has reversed direction (become negative). This is the method by which soft-switching is achieved in [4]. In the present case, we want to minimize the ripple current to increase efficiency at higher power levels. In the present design the magnetizing current does not go negative (except possibly near the zero crossing points in the input line)—a consequence of reduced ripple current.

A. Power Stage Design

Fig. 9 shows the circuit diagram of the interleaved flyback PFC power stage. The clamp circuit uses only one active clamp switch and one diode. The leakage energy from both transformers is stored in the clamp capacitor and is returned to the load through the lower transformer only. This approach simplifies the circuit design and reduces cost. Each power transformer is built using a Philips ETD44-3F3 core with 47

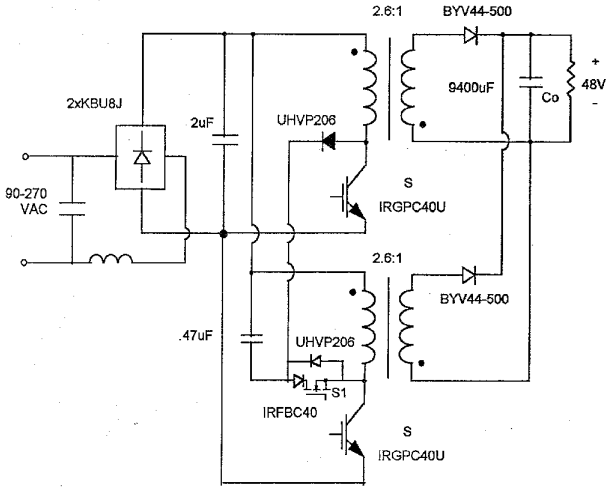

Fig. 9. Interleaved active clamp flyback PFC power stage.

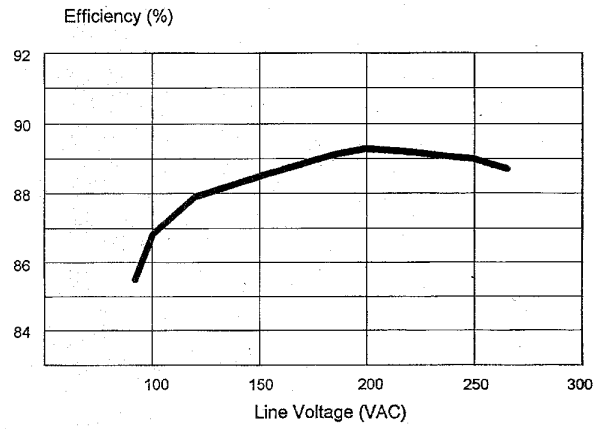

Fig. 10. Efficiency of the interleaved active clamp flyback PFC as a function of input voltage (P_o = 600 W.

primary turns (80/37 Litz wire) and 18 secondary turns (2 paralleled 80/37 Litz wires).

B. Experimental Results

The 70 KHz switching frequency was selected to limit the fundamental ripple frequency to 140 KHz and take advantage of the step change in the VDE EMI specification at 150 KHz. Lowering the switching frequency would provide higher efficiency, but the input filter size would correspondingly increase. Fig. 10 shows the efficiency as a function of line voltage with a 600 W output.

C. Hold-Up Circuit Design

One disadvantage of the single-stage flyback topology compared with a conventional two-stage front-end for a power distribution system is that it does not have inherent hold-up capability. To provide for a reasonable hold-up period after the loss of line voltage, a secondary-side hold-up capacitor would have to be very large. Fig. 11 shows a simple method of providing a specified hold-up time by storing the required

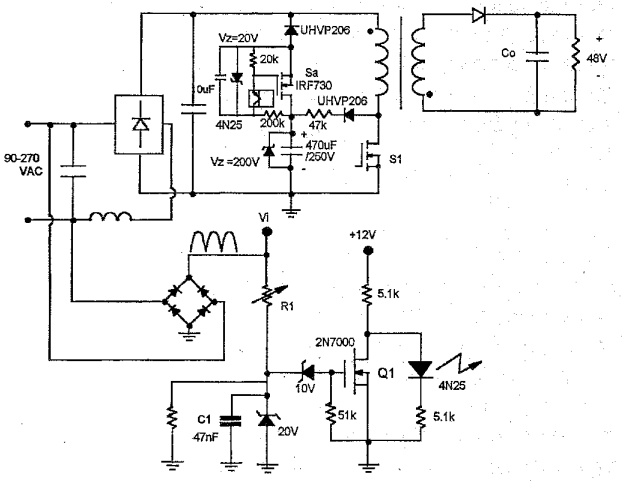

Fig. 11. Flyback converter circuit diagram with primary side hold-up.

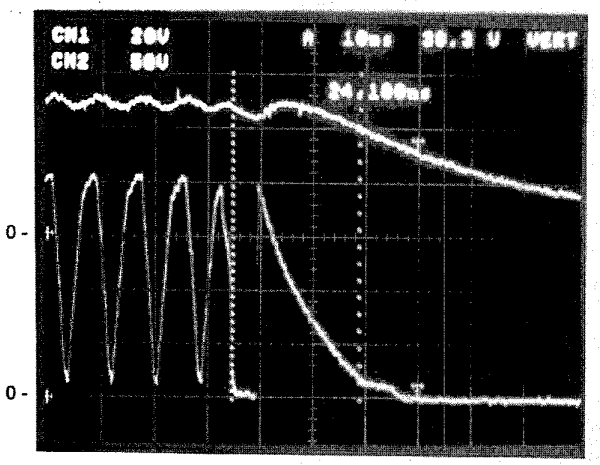

Fig. 12. Hold-up operation of the flyback PFC converter. Top waveform: V_o @ 20 V/div; bottom waveform: rectified line voltage @ 50 V/div. Time base is 10 ms/div.

hold-up energy in the 470 μF capacitor located on the primary side. This capacitor is trickle charged through the 47 k resistor and a diode connected to the drain of the primary switch, S1.

During normal operation, the line voltage is sensed using R1 and the bridge rectifier, resulting in Q1 being on. When the line voltage disappears (requiring the hold-up function to be enabled), Q1 turns off after a short delay, activating the optoisolator. This turns on switch Sa, which connects the energy-storage capacitor to the input of the flyback converter. Fig. 12 shows hold-up operation with the primary side hold-up circuit. It can be seen that practically all of the energy stored in the hold-up capacitor is utilized. For a primary side capacitor value of 470 μF, the resulting hold-up time is about 24 ms.

VI. Conclusion

This paper has presented design and experimental results for both a 500 W single-stage and a 600 W interleaved flyback PFC converter incorporating active clamp circuitry.

Primary areas of application are as for front-end modules in power distribution systems. As demonstrated in the experimental results obtained for both the interleaved and noninterleaved configurations, the active clamp variation of the traditional flyback topology offers an attractive alternative to the more usual two-stage approach (boost cascaded by a buck) to off-line power conditioning for distributed power systems.

APPENDIX

This appendix outlines the derivations of (8)–(10), which appear in Section IV. The derivations of all the equations given in Section IV make use of the following assumptions:

- unity power factor operation with $F_S \rightarrow \infty$ (compared to F_{line});
- flyback "transformer" leakage inductance is small enough to neglect its effects on circuit operation;
- clamp and output capacitors are infinite in value;
- no delay between the turn-off of S2 and turn-on of S1.

Fig. 13 shows the idealized converter waveforms over a switching cycle under the constraints imposed by the assumptions listed above.

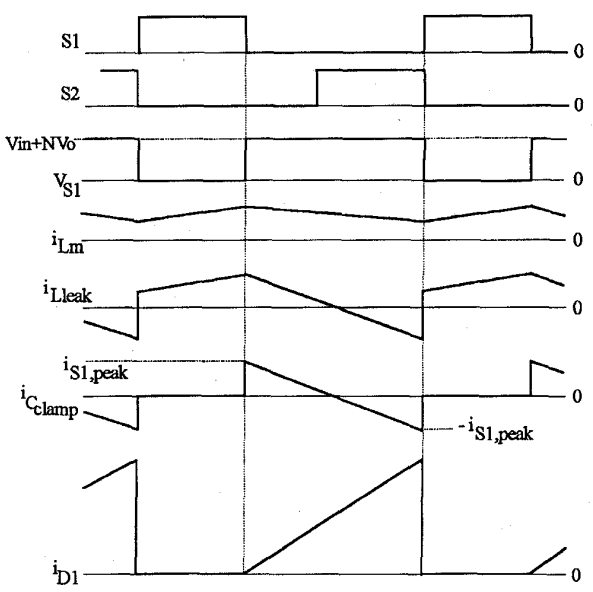

Fig. 13. Switching cycle active clamp flyback ideal waveforms.

Equation (8): For component selection purposes, it is necessary to know the clamp capacitor RMS current averaged over half of the line cycle (120 Hz). Compared with averaging over a switching cycle, line cycle averaging considerably complicates the derivation, necessitating a further simplification of the clamp capacitor waveform. The simplified version is shown in Fig. 14. I_C is selected so that the ideal and simplified waveforms have the same positive and negative areas. Therefore

$$I_C = \tfrac{1}{2} i_{\text{S1}}|_{\text{peak}}. \tag{16}$$

Since the averaging is done over half of the line cycle, I_C is time dependent (a function of S1's peak switch current, which is in turn a function of the converter duty cycle). Therefore, S1's peak switch current needs to determined as a function of where the instantaneous operating point is on the input line cycle ($T_S \rightarrow 0$ compared to the line cycle period). Neglecting ripple current in the switch

$$I_{\text{S1}}(\phi) = \frac{I_{\text{avg}}(\phi)}{D(\phi)}. \tag{17}$$

In (17), one-half the line cycle period is considered to be normalized to the interval $[0, \pi]$, and ϕ is an arbitrary point on that interval. $I_{\text{AVG}}(\phi)$ is the average input line current and is given by

$$I_{\text{AVG}}(\phi) = \frac{\sqrt{2}P_o}{\eta V_{\text{RMS}}} \sin(\phi). \tag{18}$$

The instantaneous duty cycle is

$$D(\phi) = \frac{V_o}{V_o + \frac{\sqrt{2}V_{\text{RMS}}}{N} \sin(\phi)}. \tag{19}$$

Neglecting inductor ripple current, $I_{\text{S1}}(\phi) = I_{\text{S1}}(\phi)|_{\text{peak}}$, and (17)–(19) can be combined and substituted into (16) to yield an expression for I_C that is a function of the instantaneous operating point on the input line. The amplitude (I_C) of each "pulse" shown in Fig. 14 is now known as a function of ϕ, but to calculate the RMS value the pulse area is required

$$\text{RMS value} = \sqrt{\frac{1}{\pi} \sum_{\text{line cycle}} (\text{area of each pulse with amplitude squared})}. \tag{20}$$

From Fig. 14, the pulse area is simply given by

$$\text{area} = I_C^2(\phi)[1 - D(\phi)]. \tag{21}$$

Therefore, the estimated value of clamp capacitor 120 Hz ripple current can now be calculated

$$I_{C\text{clamp,RMS}} \approx \sqrt{\frac{1}{\pi} \int_0^{\pi} \frac{P_0^2}{2\eta^2 V_{\text{RMS}}^2} \sin^2(\phi) \left[\frac{1 - D(\phi)}{D(\phi)}\right] d\phi}. \tag{22}$$

Carrying out the integration called for in (22) yields (8).

Equation 9: The active clamp flyback transformer primary RMS (120 Hz) current is the root-sum-of-squares (RSS) combination of the clamp capacitor RMS current (8) and the RMS value of the primary switch current

$$I_{\text{pri,RMS}} = \sqrt{I_{\text{S1,RMS}}^2 + I_{C\text{clamp,RMS}}^2} = \sqrt{\frac{1}{\pi} \int_0^{\pi} I_{\text{S1}}^2(\phi)\, d\phi + I_{C\text{clamp,RMS}}^2}. \tag{23}$$

Equation (23) is valid because the two current waveforms that comprise the transformer's primary current are non-zero over mutually exclusive intervals (over a switching cycle—see Fig. 13). Substitution of (17) and (8) into (23) yields (9).

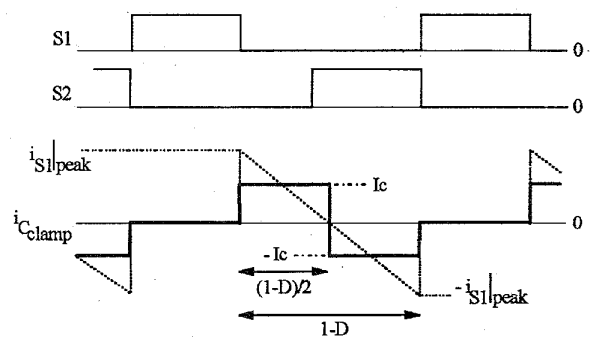

Fig. 14. Simplified clamp capacitor current waveform.

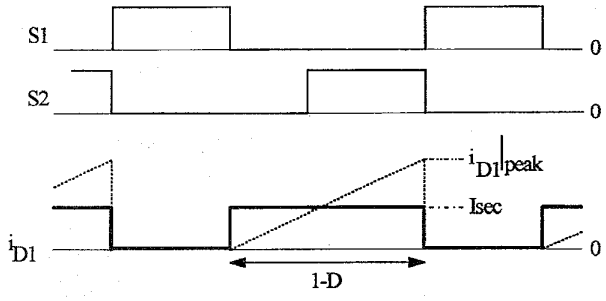

Fig. 15. Simplified output rectifier current waveform.

Equation 10: The flyback transformer's secondary is in series with the output rectifier and so has the idealized current waveform (i_{D1}) shown in Fig. 13. Both the clamp capacitor and transformer secondary current waveforms share similar properties; hence, to make the mathematics tractable, the secondary current waveform will be simplified in an analogous manner. The simplified version is shown in Fig. 15. I_{sec} is chosen so that the average value of the output rectifier's simplified "pulsed" current waveform yields the correct value of average rectifier current. Of course, this average is a function of the line cycle; therefore

$$I_{sec}(\phi) = \frac{\frac{2P_o}{V_o}\sin^2(\phi)}{1 - D(\phi)}. \tag{24}$$

The RMS value is then calculated using (20) and an expression for the area calculated over a switching cycle

$$\text{area} = I_{sec}^2(\phi)[1 - D(\phi)]. \tag{25}$$

Combining (19), (24), and (25) and substituting into (20) yields (10).

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Robert Watson (S'93), for a photograph and biography, see this issue, p. 169.

Guichao C. Hua, for a photograph and biography, see this issue, p. 169.

Fred C. Lee (S'72–M'74–SM'87–F'90), for a photograph and biography, see this issue, p. 169.