Design Optimization of Soft-Switched Insulated DC/DC Converters With Active Voltage Clamp

G. Spiazzi*, L. Rossetto**, P. Mattavelli**

*Dept. of Electronics and Informatics
**Dept. of Electrical Engineering
University of Padova
Via Gradenigo 6/a
35131 Padova - ITALY
Tel: (+39) 49-827.7517 Fax: 827.7599

Abstract - The use of an active voltage clamp in insulated DC/DC converters allows a limitation of the voltage stress due to transformer leakage inductance, a reduction of the commutation losses, and an increase of the switching frequency. It is therefore important to ensure soft switching in the whole operating range, penalty a considerable worsening of converter efficiency and electromagnetic noise generation.

In this paper a design approach of insulated converters with active voltage clamp is presented, which allows soft switching from no load to full load. The approach is described for the case of a flyback converter but is valid also for Sepic and Cuk topologies.

Experimental results of a 100 W-300 kHz converter demonstrate the excellent performances obtained according to the proposed design procedure: switch overvoltage less than 20% of the nominal value in any operating condition and overall converter efficiency above 83% from 50% to 100% of rated load.

I. Introduction

When electric insulation is a prime concern in dc-dc conversion, flyback, Sepic and Cuk topologies are good candidates for their relative simplicity as compared to other solutions. The main problem of these converters is represented by the transformer leakage inductance, which may cause severe voltage stress on the main devices and contributes significantly to conducted and radiated EMI.

Passive clamps, like the usual R-C-D snubber circuit, help to limit the switch overvoltage at the expense of higher losses, while damping of the high frequency parasitic oscillations calls for additional R-C snubbers, further decreasing the overall efficiency.

Active clamps, consisting of an auxiliary switch in series to a clamp capacitor, provide a viable solution to reduce the voltage stress without increasing appreciably the converter losses. Moreover, the auxiliary switch of the active clamp allows a soft commutation of the main devices [1-3]. For this purpose, the energy stored in the transformer is exploited to discharge the switch parasitic capacitance before turning on, thus achieving zero-voltage switching of the main switch, soft turn off of the freewheeling diode and elimination of high frequency parasitic oscillations.

Previous works on this topic have demonstrated that soft switching is feasible for both discontinuous [1] and continuous [2-3] conduction mode.

The purpose of this work is twofold: first, to derive design criteria of a flyback converter with active clamp soft switched in the whole load range; second, to show that the results obtained for the flyback converter can be directly extended also to Sepic and Cuk topologies.

The theoretical forecasts are experimentally tested on a 100 W flyback converter switching at 300 kHz, which in fact demonstrates high efficiency, small voltage stresses and no-load to full-load regulation under soft-switched conditions.

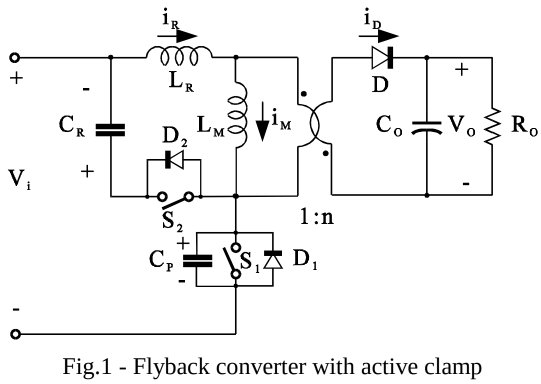

Fig.1 - Flyback converter with active clamp

II. Analysis of Flyback Converter with Active Clamp - A Review

In this section, the behavior of flyback converter with active clamp is reviewed both for Continuous (CCM) and Discontinuous (DCM) Conduction Modes, while in the next section it will be shown that the same analysis is also valid for Sepic and Cuk converters.

Fig.1 shows the basic scheme of a flyback converter with active clamp. Inductance L_R includes the transformer leakage inductance while C_P accounts for the switch output capacitances. In the following analysis, ideal switching components are assumed.

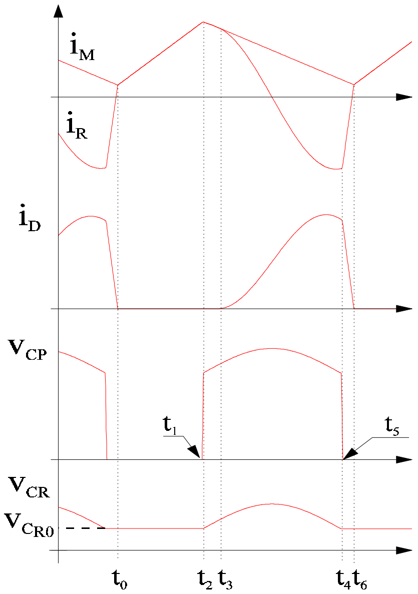

Fig.2 - Main converter waveforms in CCM operation

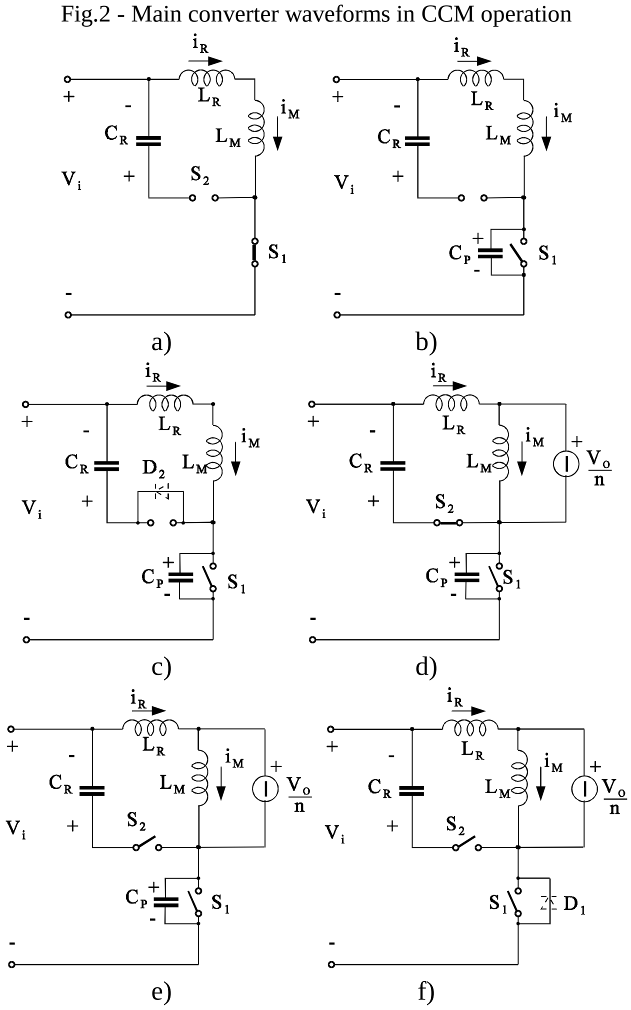

Fig.3 - Subtopologies corresponding to different switch states

A. Continuous Conduction Mode (CCM)

As it can be seen in Fig. 2, which shows the main converter waveforms in CCM, each switching period is subdivided into six intervals, each of them correspondent to a different topology (see Fig.3). In order to simplify the analysis, the relative time of each interval is set to zero at the beginning of the interval.

1) Interval t_0-t_1 (Fig.3a): At instant t_0 the freewheeling diode D stops conduction and switch S_1 is on while switch S_2 is off. The currents in leakage inductance L_R and magnetizing inductance L_M are equal and increase linearly with a slope dependent on the input voltage:

$$i_M(t) = i_M(t_0) + \frac{V_i}{L_M(1+\beta)} \cdot t \tag{1}$$

where $\beta = \frac{L_R}{L_M}$.

2) Interval t_1-t_2 (Fig.3b): S_1 is turned off at instant t_1 and C_P is then charged almost linearly by the magnetizing inductance current:

$$v_{C_p}(t) = \frac{i_M(t_1)}{C_P} \cdot t \tag{2}$$

At instant t_2, this voltage equals V_i+V_{CR0} and diode D_2 starts conducting.

3) Interval t_2-t_3 (Fig.3c): After conduction of D_2, inductors L_R and L_M resonate with capacitors C_R and C_P until the transformer secondary voltage becomes greater than the output voltage and the freewheeling diode starts conducting (instant t_3). Resonant current and voltage are given by the following equations:

$$\begin{cases} i_M(t) = i_R(t) = A_1 \cdot \sin(\omega_1 t + \varphi_1) \\ v_{C_R}(t) = -A_1 Z_1 \cdot \cos(\omega_1 t + \varphi_1) \end{cases} \tag{3.a}$$

where

$$\begin{cases} A_1 = \sqrt{i_M(t_1)^2 + \left(\frac{V_{C_{R0}}}{Z_1}\right)^2} \\ tg(\varphi_1) = \frac{Z_1 \cdot i_M(t_1)}{-V_{C_{R0}}} \end{cases} \tag{3.b}$$

$$\omega_1 = \frac{1}{\sqrt{(C_R + C_P) \cdot L_M(1+\beta)}} \tag{3.c}$$

$$Z_1 = \sqrt{\frac{L_M(1+\beta)}{C_R + C_P}} \tag{3.d}$$

and V_{CR0} is the initial value of the voltage across C_R. This interval ends when

$$v_{C_R}(t_3) = V_{op} \cdot (1+\beta) \tag{4}$$

where V_{op}=V_o/n is the output voltage reported to the primary side.

4) Interval t_3-t_4 (Fig.3d): During this interval the magnetizing current decreases linearly, transferring energy to the output, while

L_R resonates with C_R. Thus from the analysis of Fig.3d we can write:

$$i_M(t) = i_M(t_3) - \frac{V_{op}}{L_M} \cdot t \tag{5}$$

$$\begin{cases} i_R(t) = A_2 \cdot \sin(\omega_2 t + \varphi_2) \\ v_{C_R}(t) = V_{op} - A_2 Z_2 \cdot \cos(\omega_2 t + \varphi_2) \end{cases} \tag{6.a}$$

$$\begin{cases} A_2 = \sqrt{i_R(t_3)^2 + \left(\frac{V_{op}\beta}{Z_2}\right)^2}, i_R(t_3) = i_M(t_3) \\ tg(\varphi_2) = \frac{Z_2 \cdot i_R(t_3)}{-V_{op}\beta} \end{cases} \tag{6.b}$$

$$\omega_2 = \frac{1}{\sqrt{(C_R + C_P) \cdot L_R}} \tag{6.c}$$

$$Z_2 = \sqrt{\frac{L_R}{C_R + C_P}} \tag{6.d}$$

Note that the auxiliary switch S_2 is turned on in lossless manner before the clamp capacitor current reverses.

5) Interval t_4-t_5 (Fig.3e): At instant t_4 S_2 is turned off and L_R resonates with C_P bringing its voltage to zero (assuming that it has enough energy) and forcing the conduction of D_1 (instant t_5). Current and voltage behavior is described by the equations:

$$\begin{cases} i_R(t) = A_3 \cdot \sin(\omega_3 t + \varphi_3) \\ v_{C_P}(t) = V_i + V_{op} - A_3 Z_3 \cdot \cos(\omega_3 t + \varphi_3) \end{cases} \tag{7.a}$$

$$\begin{cases} A_3 = \sqrt{i_R(t_4)^2 + \left(\frac{V_i + V_{op} - v_{C_P}(t_4)}{Z_3}\right)^2} \\ tg(\varphi_3) = \frac{Z_3 \cdot i_R(t_4)}{-(V_i + V_{op} - v_{C_P}(t_4))} \end{cases} \tag{7.b}$$

$$v_{C_P}(t_4) = v_{C_{R0}} + V_i$$

$$\omega_3 = \frac{1}{\sqrt{C_P \cdot L_R}} \tag{7.c}$$

$$Z_3 = \sqrt{\frac{L_R}{C_P}} \tag{7.d}$$

At the same time the magnetizing current continues to decrease linearly following the relation (5) given in the previous interval.

6) Interval t_5-t_6 (Fig.3f): After conduction of diode D_1, the current in L_R increases linearly with a slope proportional to V_i+V_{op}:

$$i_R(t) = i_R(t_5) + \frac{V_i + V_{op}}{L_R} \cdot t \tag{8}$$

Note that S_1 must be turned on when i_R is still negative in order to obtain a zero voltage turn on. At t_6 current i_R becomes equal to the magnetizing current i_M (which was still linearly decreasing), and the freewheeling diode D stops conduction, initiating another switching cycle.

B. Discontinuous Conduction Mode (DCM)

Fig.4 reports the main waveforms of the same converter taken at 5% of rated power. The only difference in the operation sequence is that interval t_3-t_4 is terminated by the turn off of the freewheeling diode D while S_2 is still on. After that, L_R and L_M resonate with C_R until S_2 is turned off (instant t_5). Then, L_R and L_M together resonate with C_P, bringing its voltage to zero (instant t_6) and initiating another switching cycle.

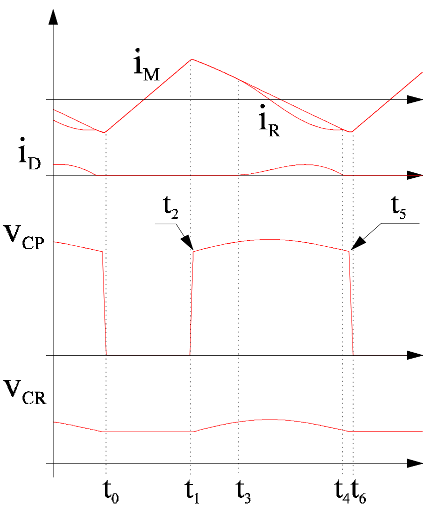

Fig.4 - Main converter waveforms in DCM operation

III. Extension to Isolated CUK and SEPIC Topologies

The analysis done for the flyback converter can be easily extended also to Sepic and Cuk topologies.

A. Sepic Converter

Consider the Sepic converter with active clamp shown in Fig.5a. As for the flyback converter, L_R represents the transformer leakage inductance and C_P the main switch output capacitance.

Assuming that energy transfer capacitor C_1 has a negligible voltage ripple, it can be substituted by a voltage generator V_{C1} having the same value of the input voltage (which is the average voltage across C_1 in steady state). Moving it across node A and rearranging we obtain the scheme drawn in Fig.5b. If the approximation shown in Fig. 5c holds i.e. L_1, $L_M >> L_R$, the scheme of Fig.5b coincides with that of Fig.1.

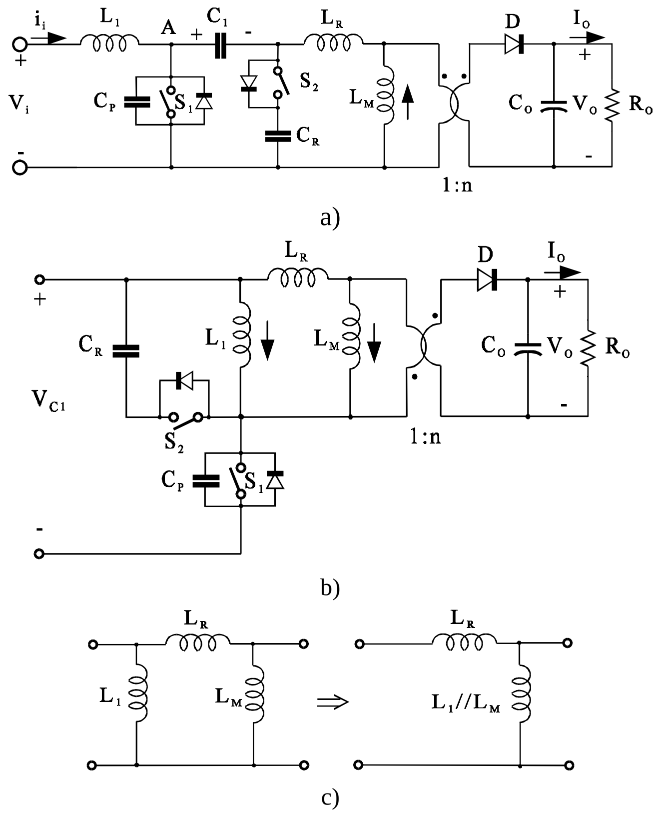

Fig.5 - a) Sepic converter with active clamp; b) the same converter considering C_1 as a voltage generator; c) approximation which holds if L_1, $L_M >> L_R$

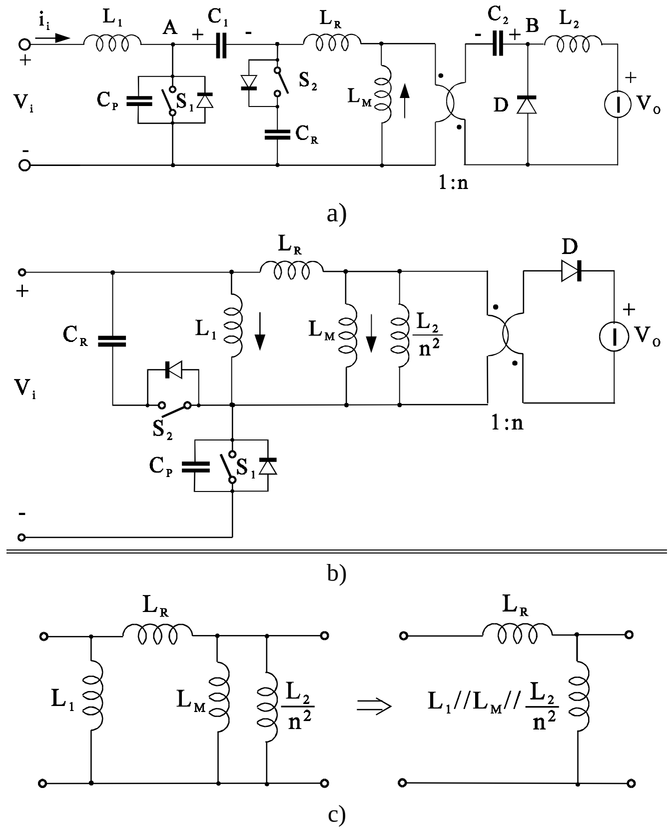

Fig.6 - a) Cuk converter with active clamp; b) the same converter considering C_1 and C_2 as voltage generators; c) approximation which holds if L_1, L_M, $L_2/n^2 >> L_R$

A. Cuk Converter

Let's consider now the Cuk converter with active clamp shown in Fig.6a in which the output filter capacitor and the load are substituted by a voltage generator V_o. Assuming that energy transfer capacitors C_1 and C_2 have a negligible voltage ripple, they can be substituted by voltage generators V_{C1} and V_{C2} having the same value of the input and output voltages respectively (which are the average voltages across C_1 and C_2 in steady state). Moving V_{C1} across node A and V_{C2} across node B and rearranging we obtain the scheme drawn in Fig.6b. If the approximation shown in Fig.6c holds i.e. L_1, L_M, $L_2/n^2 >> L_R$, the scheme of Fig. 6b coincides with that of Fig.1.

It is worthy to note that also for the Cuk converter, the freewheeling diode average current is equal to the load current because the average current in C_2 is zero in steady state.

IV. Simplified Converter Analysis

As we can see from the waveforms of Figs. 2 and 4, the behavior of the flyback converter with active clamp is quite different respect to its hard-switched counterpart. However, using suitable approximations, it is possible to derive useful relations which can greatly simplify the design procedure.

First of all, as far as the conversion ratio is concerned, we can observe that the voltage across the magnetizing inductance L_M is equal to $V_i/(1+\beta)$ during the switch on-time, while during the switch off-time it changes from V_{op} (interval t_3-t_4) to $v_{CR}/(1+\beta)$ during interval t_2-t_3 (and also t_4-t_5 in DCM). Since v_{CR} value in these intervals is close to V_{op} and considering that the duration of this interval is small compared to that of interval t_3-t_4, we have from the voltage balance on L_M:

$$\frac{V_i}{1+\beta}\cdot\delta T_S \cong V_{op}\cdot(1-\delta)T_S$$

$$M=\frac{V_{op}}{V_i}=\frac{\delta}{1-\delta}\cdot\frac{1}{(1+\beta)} \quad (9)$$

which is almost the same of the usual flyback converter. Note that the same expression holds for both CCM and DCM operating modes.

The average current I_M in the magnetizing inductance, assuming unity efficiency, is given by:

$$I_M = I_i + nI_o = nI_o(1+M) \quad (10)$$

while its current ripple amplitude is:

$$\Delta i_M = \frac{V_i}{L_M f_S}\cdot\frac{\delta}{(1+\beta)}=\frac{V_{op}}{L_M f_S}\cdot\frac{1}{1+M(1+\beta)} \quad (11)$$

where $f_S = 1/T_S$ is the switching frequency.

From (10) and (11) the peak current in the magnetizing inductance results:

$$\hat{i}_M = i_M(t_1) = I_M + \frac{\Delta i_M}{2} = nI_o \cdot \left[1 + M + \frac{1}{k[1+M(1+\beta)]}\right] \qquad (12)$$

where

$$k = \frac{2L_M f_S}{R_{op}} = \frac{2L_M f_S n^2}{R_o} \qquad (13)$$

is the usual adimensional parameter used in the flyback analysis.

In order to derive the value of load current at which the operating mode changes between CCM and DCM we must introduce some approximations. In particular, if in interval t_3-t_4 we consider $\beta \approx 0$ (which means $L_R << L_M$) and if we consider $i_M(t_3) \approx i_M(t_1)$, then from (6) current i_R and voltage v_{C_R} simplify to:

$$\begin{cases} i_R(t) = i_M(t_1) \cdot \cos(\omega_2 t) \\ v_{C_R}(t) = V_{op} + Z_2 i_M(t_1) \cdot \sin(\omega_2 t) \end{cases} \qquad (14)$$

Thus,

$$i_R(t_4) = i_M(t_1)\cos(\omega_2 T_{34}) = i_M(t_1)\cos(\varepsilon) \qquad (15.a)$$

where

$$\varepsilon = \omega_2 T_{34} \text{ and } T_{34} = t_3 - t_4 \approx (1-\delta)T_S\,. \qquad (15.b)$$

The discontinuous mode of operation is reached when at instant t_4 resonant inductor current i_R and magnetizing current i_M are equal. Thus:

$$i_R(t_4) = I_M - \frac{\Delta i_M}{2} \qquad (16)$$

which gives the value of parameter Kcrit at the boundary between CCM and DCM:

$$k_{crit} = \frac{1-|\cos(\varepsilon)|}{1+|\cos(\varepsilon)|} \cdot \frac{1}{(1+M)^2} \qquad (17)$$

This means that the converter enters in DCM at a fraction α of the nominal output power, given by:

$$\alpha = R_{op} \cdot \frac{k_{crit}}{2L_M f_S} \qquad (18)$$

V. Zero Voltage Switching Conditions

The analysis reported in section III shows that in CCM operation only the energy stored in the leakage inductance at instant t_4 plays a role in discharging the mosfet parasitic capacitance C_P, while in DCM operation also the magnetizing inductance L_M is involved in this process (instant t_5). Thus, the condition to obtain zero voltage commutation depends on the operating mode.

A. ZVS Condition in CCM

From the previous analysis, looking at the interval t_4-t_5, we can see that the voltage v_{C_P} reaches zero if the following inequality holds:

$$A_3 Z_3 \geq V_i + V_{op} \qquad (19)$$

Using the same approximation for which (14) was derived, and assuming $v_{CR0} \approx V_{op}$, (19) can be written as:

$$Z_3\, i_M(t_1)|\cos(\varepsilon)| \geq V_i + V_{op} \qquad (20)$$

which, rearranged, gives the following constraint on L_R:

$$\sqrt{\frac{L_R}{C_P}} \geq \frac{2L_M f_S}{M} \cdot \frac{(1+M)^2}{1+k(1+M)^2} \cdot \frac{1}{|\cos(\varepsilon)|} \qquad (21)$$

The minimum value of L_R is obtained for $\varepsilon = \pi$.

Note that if inductance L_R is designed so as to meet the above inequality for k = 0, then the ZVS condition should be maintained in the entire load range.

B. ZVS Condition in DCM

In order to derive the ZVS condition for this operating mode, the interval t_5-t_6 of Fig.4 must be analyzed. The subcircuit corresponding to this interval is equal to that of Fig.3b. From this latter, the behavior of inductor currents and switch voltage is:

$$\begin{cases} i_R(t) = i_M(t) = A_4 \cdot \sin(\omega_4 t + \varphi_4) \\ v_{C_P}(t) = V_i - A_4 Z_4 \cdot \cos(\omega_4 t + \varphi_4) \end{cases} \qquad (22.a)$$

$$\begin{cases} A_4 = \sqrt{i_R(t_5)^2 + \left(\dfrac{v_{C_{R0}}}{Z_4}\right)^2} \\ tg(\varphi_4) = \dfrac{Z_4 \cdot i_R(t_5)}{-v_{C_{R0}}} \end{cases} \qquad (22.b)$$

$$\omega_4 = \frac{1}{\sqrt{C_P \cdot L_M(1+\beta)}} \qquad (22.c)$$

$$Z_4 = \sqrt{\frac{L_M(1+\beta)}{C_P}} \qquad (22.d)$$

In order for v_{C_P} to reach zero the following condition must be satisfied:

$$A_4 Z_4 \geq V_i \Rightarrow Z_4^2 \geq \frac{V_i^2 - v_{C_{R0}}^2}{i_R^2(t_5)} \qquad (23)$$

Considering that $i_R(t_5) = I_M - \Delta I_M/2$, considering $\beta = 0$ and using the approximation $v_{CR0} \approx V_{op}$, the above constraint yields;

$$\sqrt{\frac{L_M}{C_P}} \geq \frac{2L_M f_S}{M} \cdot \frac{(1+M)\cdot\sqrt{1-M^2}}{\left|k(1+M)^2 - 1\right|} \qquad (24)$$

VI. Design Guidelines

From the above analysis we are now able to derive a suitable design procedure which allows zero voltage commutation in all operating conditions.

A. Magnetizing Inductance

The choice of the magnetizing inductance, besides the ZVS condition, influences both current and voltage stresses on the main switch. In fact, the switch current stress is equal to the peak inductor current reported in (12) while the switch voltage stress also depends on the peak magnetizing current due to the resonance between C_R

and L_R during interval t_3-t_4. In fact, from the second of (14) it results:

$$\hat{v}_{S_1} = V_i + v_{C_{R,MAX}} \cong V_i + V_{op} + Z_2 \cdot \hat{i}_M \qquad (25)$$

Both Z_2 and $\hat{i}_M$ depend on the magnetizing inductance value (Z_2 indirectly through (21)), but their product decreases for lower inductance values.

Once the desired current ripple r_i on L_M is chosen, the inductance is calculated by:

$$L_M \cong \frac{R_{op}}{2 f_S (1+M)^2} \cdot \frac{1}{r_i} \qquad (26)$$

where

$$r_i = \frac{\Delta i_M}{2 I_M}. \qquad (27)$$

We must remember that a low current ripple implies a high resonant inductor value in order to maintain the soft switching condition. Note that (26) is the same as eq. (6) in ref. [2].

B. Resonant Inductance L_R

The value of inductance L_R is chosen so as to guarantee the zero voltage commutation in all operating condition. Thus, the following procedure should be adopted:

- a suitable value of angle ε defined by (15.b) is chosen;
- the value of critical parameter k_{crit} is found from (17);
- L_R value is calculated from (21) for $k = k_{crit}$ which represents the worst condition;
- the ZVS condition in DCM must be verified from (24) for $k = k_{crit}$.

As far as the choice of angle ε is concerned, we can see from (21) that a value different from π causes an increases of resonant inductor value needed to maintain the soft switching condition because it reduces the current, and thus the energy, available at instant t_4 (see Fig. 2). Thus it is convenient to set $\varepsilon = \pi$ in the worst condition, i.e. at maximum input voltage for which the magnetizing current is minimum.

As suggested in [2], the value of L_R can be chosen also to limit the rate of change of freewheeling diode current during interval t_5-t_6 (see Fig.2).

C. Resonant Capacitor C_R

The value of resonant capacitor C_R is determined by the resonant period in the interval t_3-t_4, thus from the value of angle ε chosen in the previous subsection. From (6.c), (15.b) and (9) and using the approximations $\beta = 0$ and $C_P << C_R$ we can write:

$$C_R \approx \frac{1}{L_R \left[\varepsilon f_S (1+M)\right]^2} \qquad (28)$$

D. Main Switch S_1

Switch S_1 is chosen on the basis of its current and voltage stresses. These latter can be found by using (12) and (25) respectively.

E. Auxiliary Switch S_2

Also switch S_2 is chosen on the basis of its maximum ratings. As far as its voltage stress is concerned, it is easily verified that it is given by the following equation:

$$\hat{v}_{S_2} = V_i + V_{C_{R0}} \qquad (29)$$

while its current stress is the same of the main switch because the current flowing in it coincides practically with resonant current i_R during interval t_2-t_4.

F. Switch Drive Signals

In order to obtain the correct converter behavior, suitable switch drive signal must be generated; in particular, dead times between turn off of S_1 and turn on of S_2, and vice versa, are needed in order to provide a complete charge and discharge of parasitic capacitance C_P. From (7), the dead time t_{d1} between turn off of S_2 and turn on of S_1 in CCM can be approximated by

$$t_{d1} \approx \frac{\pi}{2\omega_3} = \frac{\pi}{2} \cdot \sqrt{L_R C_P} \qquad (30)$$

while in DCM L_R in (30) should be replaced by L_R+L_M. In practice, in DCM the discharge of C_P occurs in an interval of time much shorter than one half of resonant period, thus the suitable delay time lays between the two values.

The dead time t_{d2} between turn off of S_1 and turn on of S_2 can be derived considering interval t_1-t_2 and (2) in the worst case which occurs when the peak magnetizing inductor current is minimum, i.e. $\hat{i}_M = \frac{\Delta i_M}{2}$, with Δi_M given by (11):

$$t_{d2} = \frac{2 C_P \left(V_i + V_{op}\right)}{\Delta i_M} \qquad (31)$$

G. Capacitor C_P

This capacitance usually represents the sum of the parasitic output capacitances of S_1 and S_2 and of the freewheeling diode (reported to the primary side of the transformer). In some applications, it could be convenient to increase this capacitance by adding an external capacitor in order to limit the maximum voltage rate of change across the active devices. This provision reduces both conducted and radiated disturbances and can be necessary when IGBT are used instead of mosfets in order to reduce their turn off losses due the tail current phenomenon.

When an external capacitor is added, it is interesting to see the variation of the normalized switch voltage stress $\hat{v}_{S_N} = \hat{v}_{S_1} / \left(V_i + V_{op}\right)$ as a function of the maximum dv/dt allowed as shown in Fig.7. which reports this behavior for three different values of magnetizing current ripple r_i.

As we can see, the voltage stress increases rapidly as the maximum dv/dt is reduced. This is due to the increase of characteristic impedance Z_2 caused by the contemporary increase of L_R, needed to maintain the soft switching condition, and decrease of C_R.

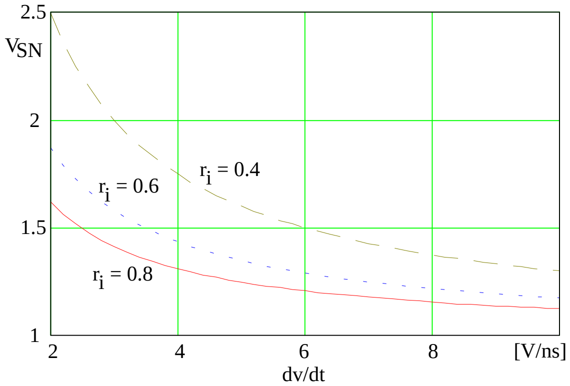

Fig.7 - Normalized switch voltage stress versus maximum dv/dt for three different values of magnetizing current ripple

It is worthy to note that the behavior reported in Fig.7 is only indicative of the phenomenon because, as C_P increases, the dead times t_{d1} and t_{d2} increase becoming non negligible respect to the switching period and thus affecting the validity of the above relations.

VII. Experimental Results

A prototype, based on flyback topology, was built and tested.

Specifications and parameter values are listed in Table I. The main components used are:

S_1, S_2: IRF 640R, D: RUR 1520

L_M: Core E3213A, $N_1 = N_2 = 12$ turns litz wire

L_R: Core P22/13, N = 3 turns litz wire

The control strategy is the peak current control implemented with the UC3823A integrated controller. The two drive signals are generated by a dual power mosfet driver (TC428) commanded by the output of the UC3823A through two delay networks.

Figs.8a) and b) show resonant inductor current i_{LR}, main switch drain-to-source voltage v_{DS1} and gate-to-source voltage v_{GS1} waveforms at 100% and about 10% of rated power respectively. As we can see, soft-switching condition is maintained also at the boundary between discontinuous and continuous conduction mode, which is the most critical point. In fact, at lower output currents, the soft-switching condition is ensured by the energy stored also in the transformer magnetizing inductance. Observe that the switch voltage waveform is very smooth with just a small ringing at the beginning of the off interval due to layout-induced parasitic inductance. Thus, the electromagnetic noise generated is reduced.

The voltage and current stresses in the main switch are 172V and 5.4A respectively. The behavior of the overall efficiency including control stage as a function of the load current is reported in Fig.9. As we can see, it remains above 83% for output currents greater than 50% of the nominal value.

Table I - Converter specifications and parameters

V_i = 100V	V_o = 48V	f_s = 300kHz	R_o = 24Ω
r_i = 0.75	ε = 7π/6	L_M = 25μH	L_R = 3.8μH
C_o = 100μF	C_R = 100nF	C_P = 0.6nF	n = 1

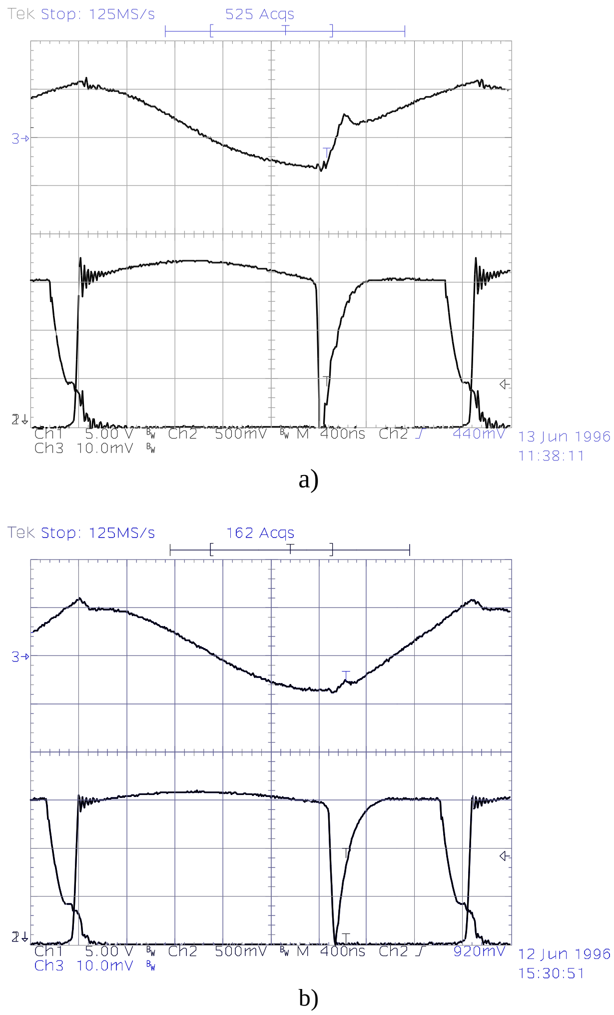

Fig.8 - Resonant inductor current i_{LR}, main switch drain-to-source voltage V_{DS1} [50V/div] and main switch gate-to-source voltage V_{GS1} [5V/div]; a) i_{LR} [5A/div], I_o = 2A; b) i_{LR} [2A/div], I_o = 0.18A

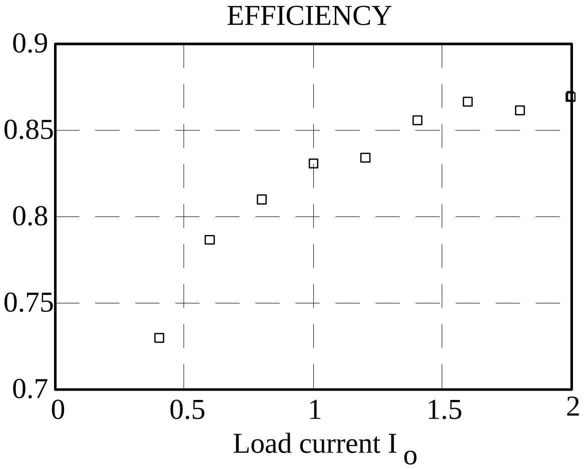

Fig.9 - Overall converter efficiency vs. load current

CONCLUSIONS

A flyback converter with active voltage clamp was analyzed reviewing its behavior for both CCM and DCM operation modes.

Suitable design criteria are given which allow soft commutation of all devices from no load to full load. Moreover, It is shown that the analysis done is also applicable to other insulated DC/DC topologies like Cuk and Sepic.

The power stage is very simple and reliable and the control does not need particular provisions respect to standard PWM controller.

Experimental results of a 100 W-300 kHz converter confirmed the theoretical forecasts showing good performances.

REFERENCES

[1] K. Yoshida, T. Ishii, N. Nagagata, "Zero Voltage Switching Approach for Flyback Converter," INTELEC Conf. Proc., 1992, pp.324-329.

[2] R. Watson, F. C. Lee, G. C. Hua, "Utilization of an Active-Clamp Circuit to Achieve Soft Switching in Flyback Converters," IEEE Power Electronics Specialists' Conf. Rec., 1994, pp. 909-916.

[3] R. Watson, G. C. Hua, F. C. Lee, "Characterization of an Active Clamp Flyback Topology for Power Factor Correction Applications," IEEE Applied Power Electronics Conf. Proc., 1994, pp. 412-418.