



SP6002

Synchronous Rectifier MOSFET Driver

DESCRIPTION

The SP6002 synchronous rectifier driver IC is a prediction based Synchronous Rectifier. The prediction logic circuit uses previous cycle timing to turn OFF the SR in the present cycle to prevent SR reverse condition , while keep the MOSFET body diode conduction at a minimum.

The SR drivers are capable up to a peak current of 1.5A.

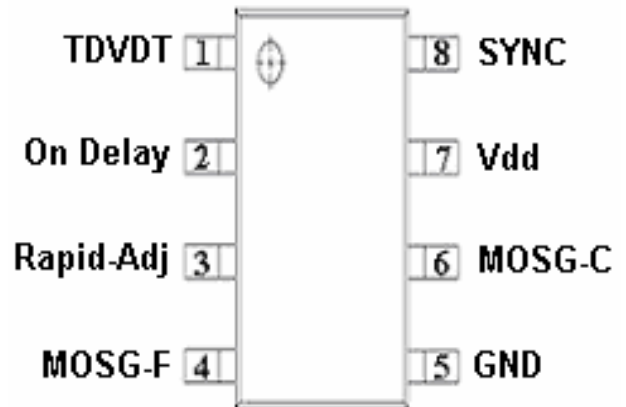
FEATURES

- ◆ Controls Synchronous Rectifier (SR) MOSFETs
- ◆ Forward Converter Topology
- ◆ Prediction gate timing control
- ◆ Minimum MOSFET body diode conduction
- ◆ Drives up to $C_{iss} = 30nF$
- ◆ Operating frequency up to 600Khz
- ◆ Synchronizes to transformer secondary voltage waveform
- ◆ Drives both forward and freewheeling (catch) position SR MOSFETs

APPLICATIONS

- Isolated forward topology power supplied
- Operates in either ac-dc or dc-dc power supplied
- Operates with any Power MOSFETs

PIN CONFIGURATION(SOP-8P)



PART MARKING



SYNC POWER CORP.

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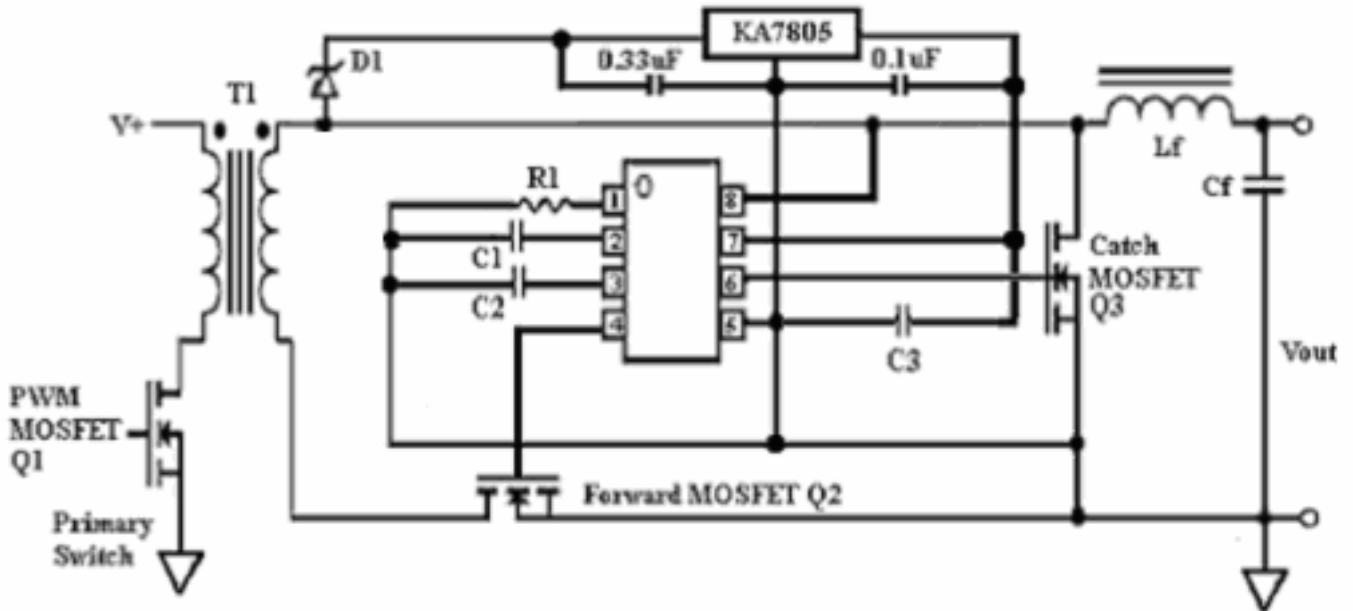
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TYPICAL APPLICATION CIRCUIT



PIN DESCRIPTION

Pin	Symbol	Description
1	TDVDT	Discontinuous current filter timing adjust resistor connection
2	ONdelay	Imposed delay between Catch Gate turn off and Forward Gate turn on
3	Rapid-Adj	Capacitor connection to adjust fast pulse width reduction response
4	MOSG-F	Forward MOSFET Gate Drive
5	GND	Connect to the Gnd
6	MOSG-C	Catch MOSFET Gate Drive
7	Vdd	Supply voltage
8	Sync	Synchronizing signal from transformer

ORDERING INFORMATION

Part Number	Package	Part Marking
SP6002S8R	SOP-8P	SP6002I



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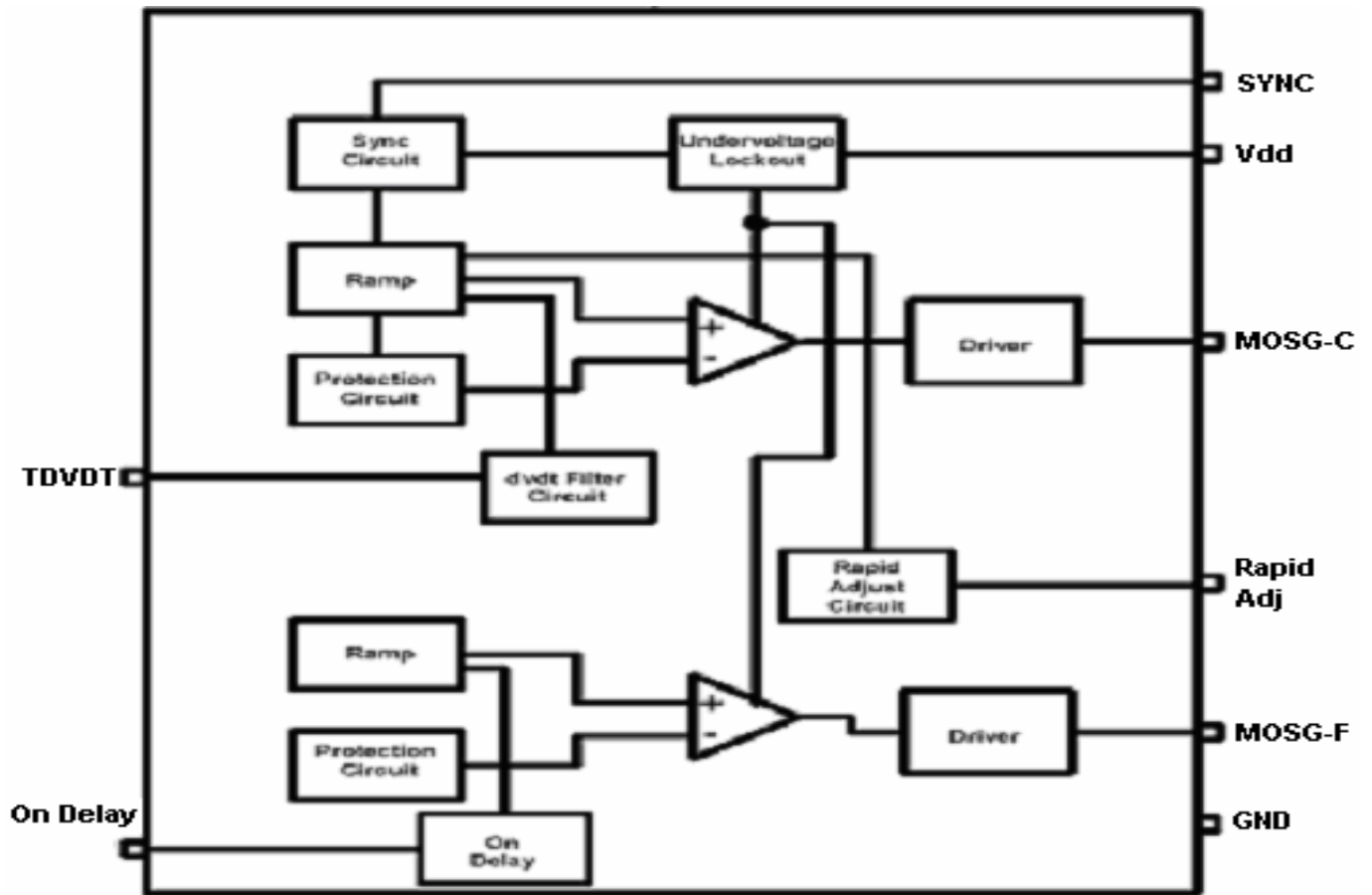
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BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS RATINGS(TA=25 Unless otherwise specified)

Parameter	Symbol	Value	Unit
Supply Voltage Rang	Vdd	7	V
Power Dissipation at 85	P _D	250	mW
Derating Factor Above 85		45	/W
Voltage at all pin		7	V
Input Voltage , Sync		Vdd+0.5	V
Source Current (Peak) Pulsed from Out		1	A
Sink Current (Peak) Pulsed into Out		1.5	A
Operating Junction Temperature Range	T _{OPJ}	-40 to125	
Storage Temperature Range	T _{STG}	-40 to 150	
Lead Soldering Temperature for 10 seconds	T _{LEAD}	300	

The IC has a protection circuit against static electricity.



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ELECTRICAL CHARACTERISTICS ELECTRICAL CHARACTERISTICS

(TA=25 , Unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
General						
Supply Current (exclude driver)	I _{dd}	Sync = 5V	1.6	2	2.3	mA
V _{dd} turn on threshold	V _{onth}	V _{dd} = 5V	3.1	3.2	3.5	V
V _{dd} turn off threshold	V _{offth}	V _{dd} = 5V	2.9	3.0	3.3	V
Sync Reference (Sync)						
Supply Voltage	V _{dd}	Sync = 5V		5		V
Sync high threshold	V _{shth}	V _{dd} = 5V	2.3	2.5	2.7	V
Sync low threshold	V _{slth}	V _{dd} = 5V	0.6	0.7	0.8	V
MOSFET Gate Driver (Out)						
Output high Voltage	V _{oh}	V _{dd} = 5V	4.8	4.9	5.0	V
Output low Voltage	V _{ol}	V _{dd} = 5V	0.0	0.1	0.2	V
Propagation delay	T _d	V _{dd} = 5V	15	20	25	ns
Rise time	T _r	Load = 10nF to GND	30	50	70	ns
Fall time	T _f	Load = 10nF to GND	20	30	40	ns



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APPLICATION INFORMATION

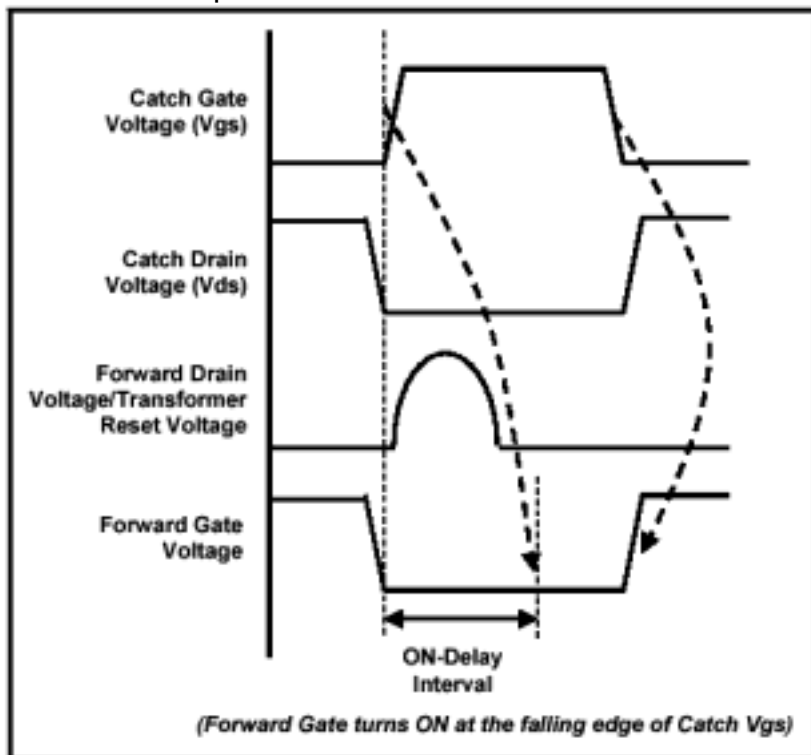
Vdd Decoupling Capacitor

The IC is somewhat sensitive to supply voltage ripple. If very large, or several large MOSFETs with significant C_{iss} are driven by the IC, then the ripple due gate drive energy transfer can create large ripple. Therefore it is recommended that a Vdd to Gnd 10 μ F high frequency decoupling ceramic capacitor be used. The SP6002 is designed to drive 30 nF in 25 nanoseconds. If higher drive capability is needed, then it is recommended that a totem P-Channel/N-Channel pair be used as a driver between the SP6002 and the MOSFET or parallel MOSFETs. If the additional driver is used, then it is recommended that the decoupling capacitor be placed in close proximity to the driver.

Adjusting ON Delay

The ON delay control imposes a minimum time after the catch MOSFET gate was turned off before the Forward MOSFET gate is turned on. This is particularly important for operation during discontinuous current operation.

The figure below shows the ON delay function during normal operation. The Forward MOSFET gate voltage turns on at the falling edge of the Catch gate voltage, V_{gs} . The next figure shows the ON delay function during light load or start-up. The Forward MOSFET gate voltage turns on after the ON-Delay interval is completed



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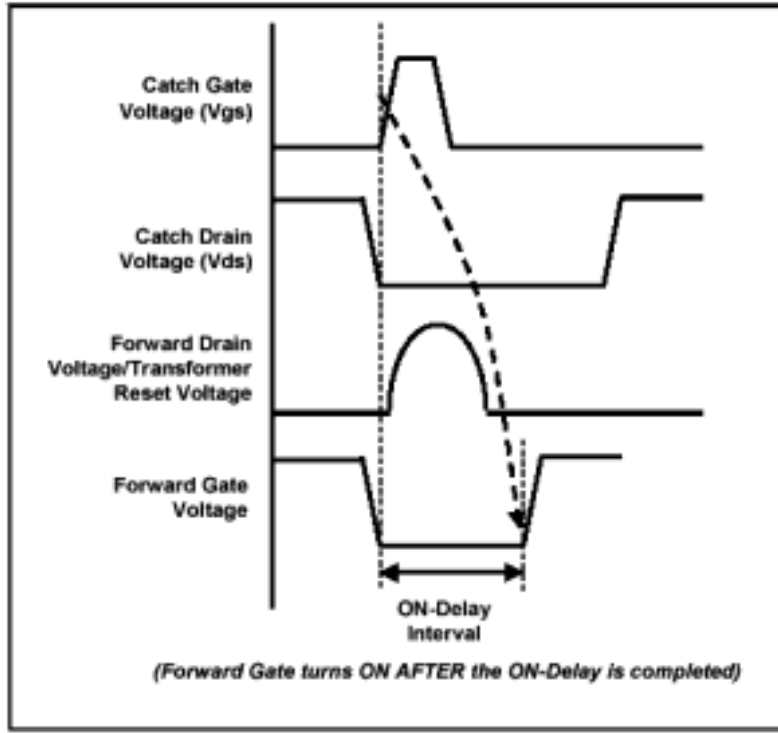
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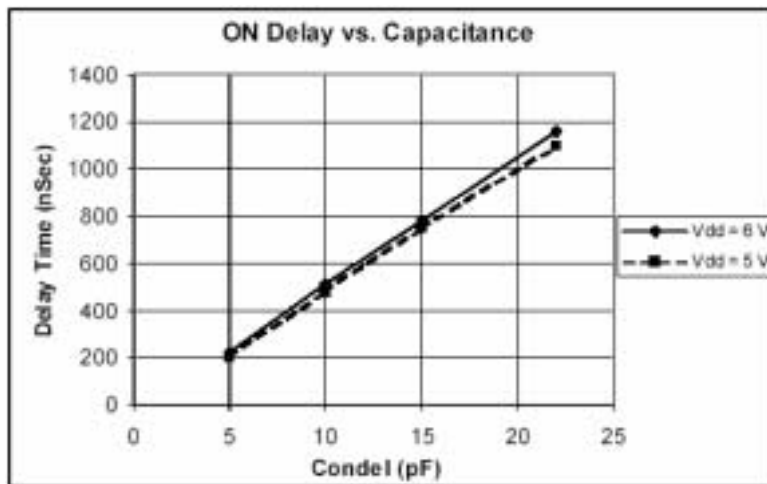


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The next figure shows the ON delay function during light load or start-up. The Forward MOSFET gate voltage turns on after the ON-Delay interval is completed.



The ON delay is adjusted by the value of capacitance connected from GND to Pin ON Delay on the SP6002. The required capacitor value is highly dependent on the transformer reset method. Forward converters can be reset by 1) diode method, 2) passive RC method, or 3) active method. The suggested starting value for the ON Delay Capacitor is 1/2 the Ramp Capacitor.



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Adjusting Tdvd timing

The Tdvd pin provides adjustment of the proprietary dv/dt filter circuit that differentiates between the real power and ring-back no-power transformer secondary voltage positive waveform. Under light or no load voltage positive waveform. Under light or no load, for that condition the transformer voltage “rings” back positive. The SP6002 detects positive transformer secondary voltage to establish power transmission, and determines the SR MOSFET turn ON time. However, it is not desirable to turn on the MOSFET during the “ring-back”. The dv/dt filter detects the true power pulse from the “ring-back” by measuring the voltage waveform dv/dt. A very fast dv/dt is interpreted as true power pulse. A slow dv/dt is interpreted as “ring-back”.

However the “normal” power pulse rise time may be well above or below the nominal dv/dt threshold setting., Pin(Tdvd), provides some adjustment for those cases. There are three possible connections. The first is nominal setting. For this condition, Pin(Tdvd) is left open or no connection.

For the case where the power pulse rise time is much slower than nominal, connect a 47 k ohm resistor from Pin(Tdvd) to Vdd.

For the case where the power pulse rise time is much faster than nominal, connect a 47 k ohm resistor from Pin(Tdvd) to GND.

The table below summarizes the typical rise time that can be achieved with the various connections to Pin(Tdvd).

Pin(dv/dt)Connect	Typical Rise Threshold (nanoseconds)
1K ohm to Vdd	25
Open	50
1K ohm to GND	100

Sync Pin

Pin (Sync), the Sync input terminal, is clamped internally to the Vdd supply if pulled to a voltage higher than Vdd. There fore a 1 K ohm resistor should be placed in series with the sync signal and Pin (Sync). The 1 K ohm resistor allows for sync voltages up to to 20V. The datasheet is misleading regarding this point as some early version of the IC included an internal resistor. For production devices that are now available, an external resistor must be used for sync voltages above Vdd. Your sync signal resistor divider will only be necessary if your sync voltage exceeds 20 volts.

Rapid Adj Pin

The Rapid Adjust circuit initiates a delay to assure that the drive circuit will not false trigger when there is a very fast reduction in pulse width required in the pulse width modulation. This can occur in regulators for very high di/dt load changes demanded by such loads as microprocessors. False triggering could result in a high cross conduction current for a few nanoseconds. The capacitor, Cra, connected to the Rapid Adj. pin sets the amount of filtering. For most applications, a value of 100 pF is appropriate.



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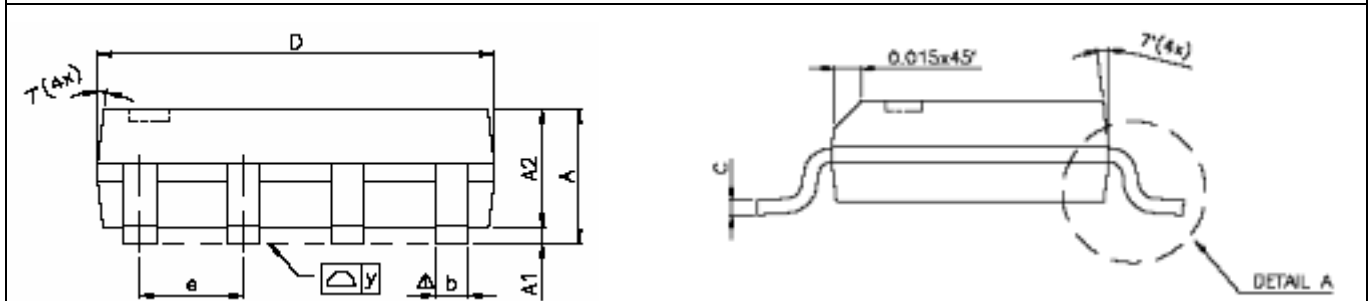
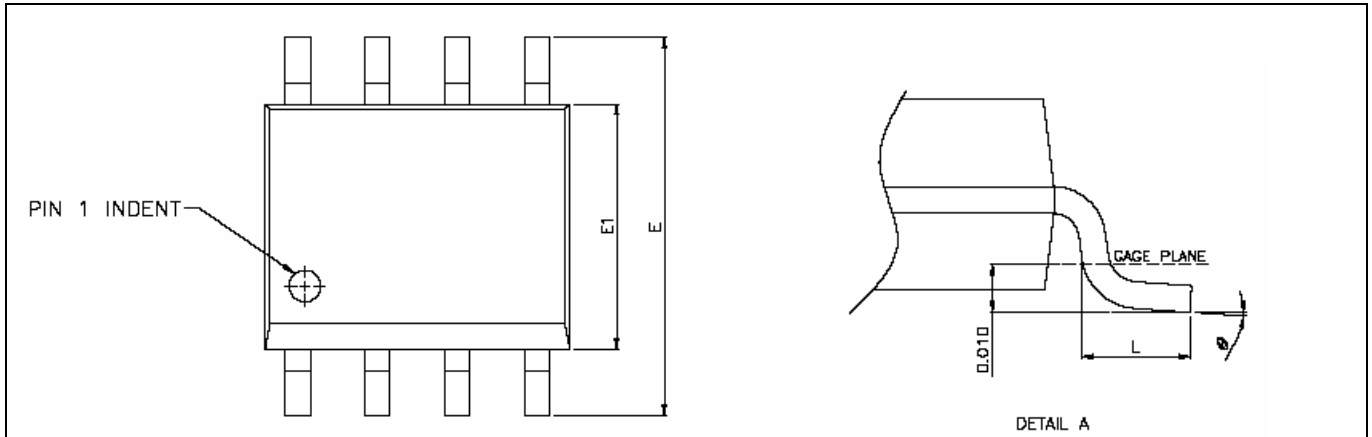
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SOP-8 PACKAGE OUTLINE



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.47	1.60	1.73	0.058	0.063	0.068
A1	0.10	—	0.25	0.004	—	0.010
A2	—	1.45	—	—	0.057	—
b	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.0098
D	4.80	4.85	4.95	0.189	0.191	0.195
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e	—	1.27	—	—	0.050	—
L	0.38	0.71	1.27	0.015	0.028	0.050
Δ y	—	—	0.076	—	—	0.003
θ	0°	—	8°	0°	—	8°



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