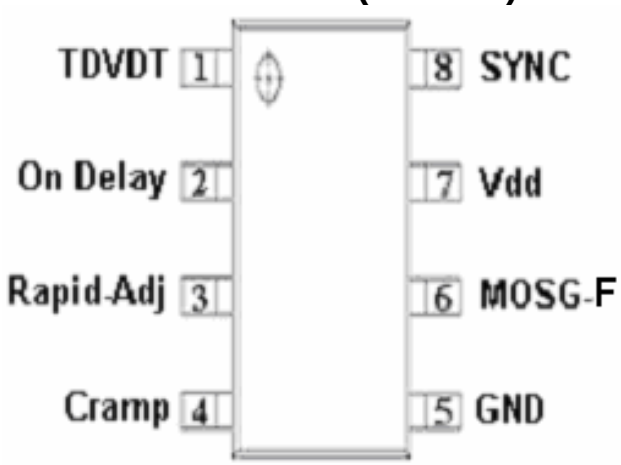
SP6003
Synchronous Rectifier MOSFET Driver

DESCRIPTION
The SP6003 synchronous rectifier driver IC is a prediction based Synchronous Rectifier. The prediction logic circuit uses previous cycle timing to turn OFF the SR in the present cycle to prevent SR reverse condition , while keep the MOSFET body diode conduction at a minimum.
The SR drivers are capable up to a peak current of 1.5A.

APPLICATIONS
- Isolated flyback topology power supplies
- Operates in either ac-dc or dc-dc power supplied
- Operates with any Logic Power MOSFETs

FEATURES
- Controls Synchronous Rectifier (SR) MOSFETs
- Flyback Converter Topology
- Prediction gate timing control
- Minimum MOSFET body diode conduction
- Drives up to Ciss =30nF
- Operating frequency up to 600Khz
- Synchronizes to transformer secondary voltage waveform

PIN CONFIGURATION(SOP-8P)


PART MARKING


A : Lot Code
B : Date Code

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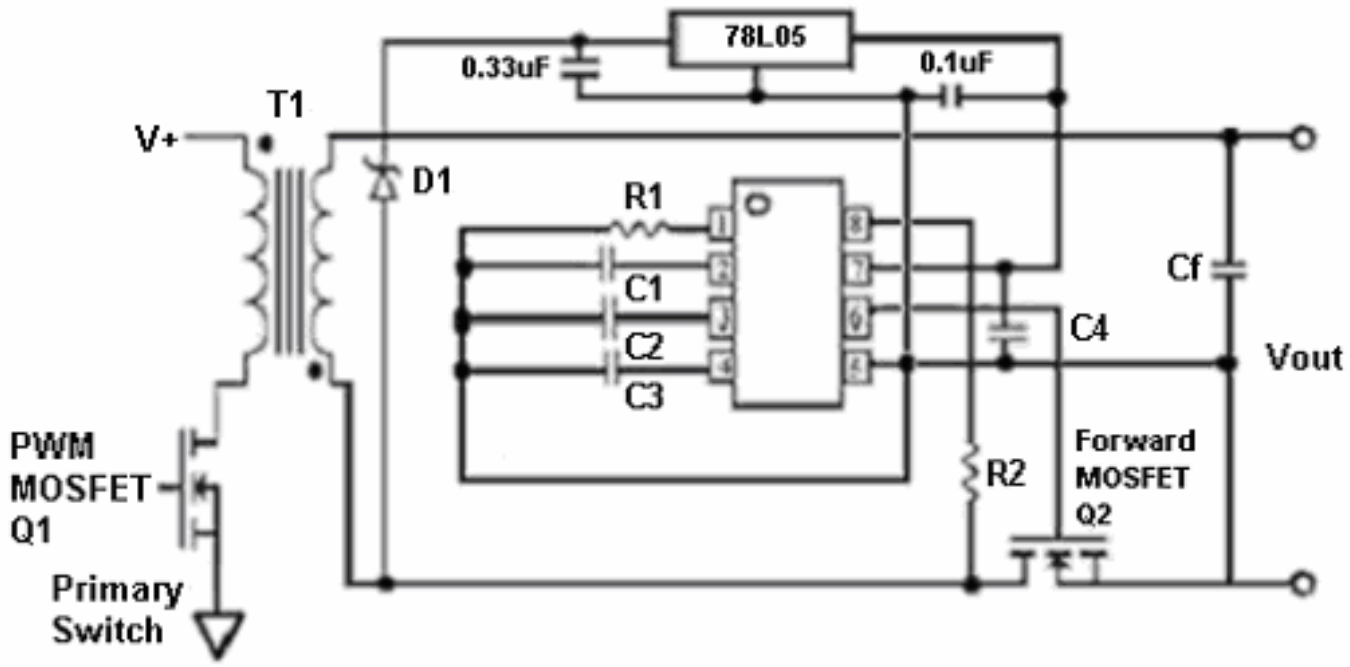
TYPICAL APPLCATION CIRCUIT



PIN DESCRIPTION

Pin	Symbol	Description
1	TDVDT	Discontinuous current filter timing adjust resistor connection
2	ON delay	Imposed delay between Catch Gate turn off and Forward Gate turn on
3	Rapid-Adj	Capacitor connection to adjust fast pulse width reduction response
4	Cramp	Catch MOSFET Ramp capacitor is connected from this terminal to Gnd
5	GND	Connect to the Gnd
6	MOSG-F	Catch MOSFET Gate Drive
7	Vdd	Supply voltage
8	Sync	Synchronizing signal from transformer

ORDERING INFORMATION

Part Number	Package	Part Marking
SP6003S8R	SOP- 8P	SP6003 I

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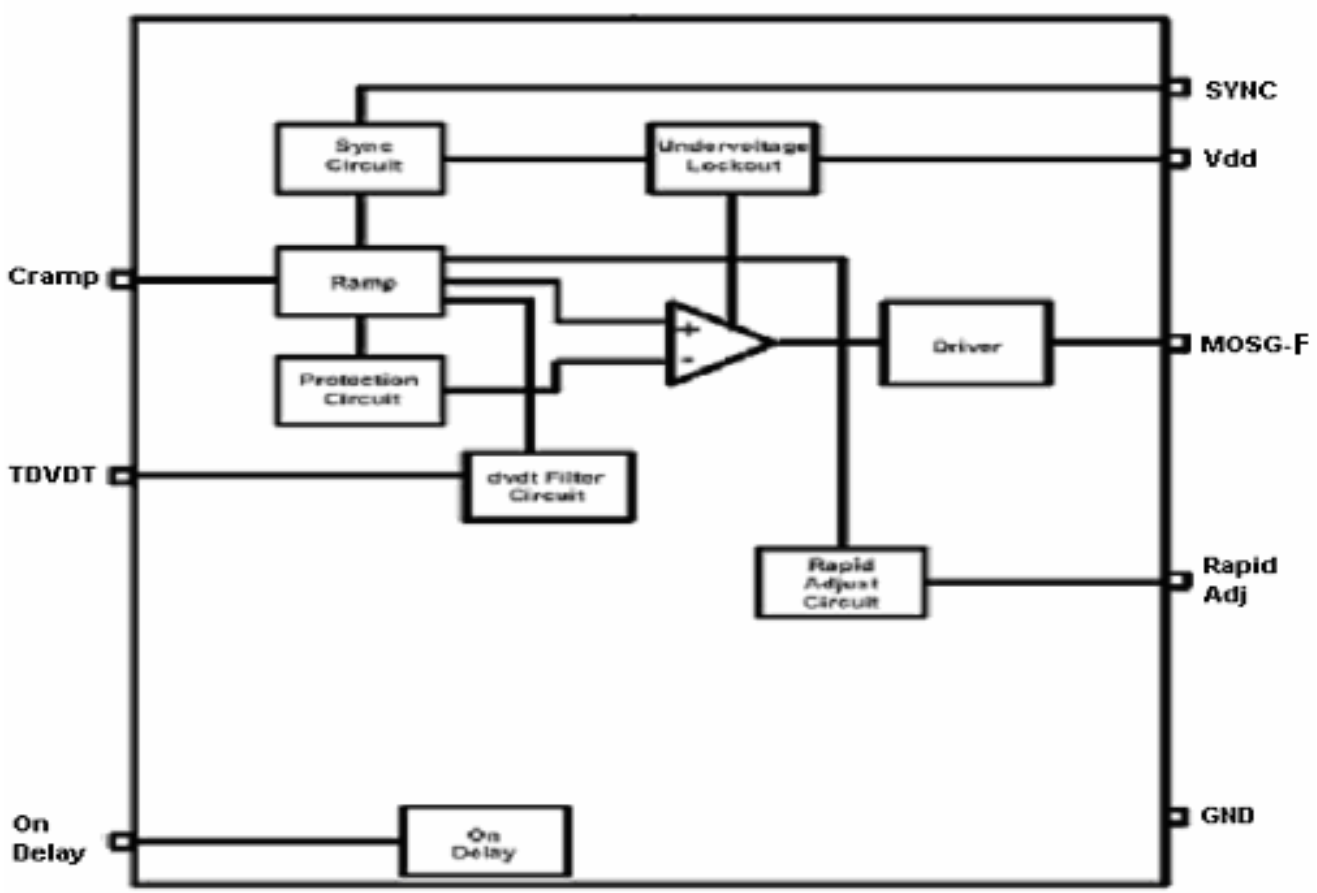
BLOCK DIAGRAM



ABSOULTE MAXIMUM RATINGS (TA=25℃ Unless otherwise specified)

Parameter	Symbol	Value	Unit
Supply Voltage Range	Vdd	7	V
Power Dissipation at 85℃	P_D	250	mW
De-rating Factor Above 85℃		45	℃/W
Voltage at all pin		7	V
Input Voltage , Sync		Vdd+0.5	V
Source Current (Peak) Pulsed from Out		1	A
Sink Current (Peak) Pulsed into Out		1.5	A
Operating Junction Temperature Range	T_{OPJ}	-40 to125	℃
Storage Temperature Range	T_{STG}	-40 to 150	℃
Lead Soldering Temperature for 10 seconds	T_{LEAD}	300	℃

The IC has a protection circuit against static electricity.

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ELECTRICAL CHARACTERISTICS

(TA=25℃ , Unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
General						
Supply Current (exclude driver)	Idd	Sync = 5V	1.6	2	2.3	mA
Vdd turn on threshold	Vonth	Vdd = 5V	3.1	3.2	3.5	V
Vdd turn off threshold	Voffth	Vdd = 5V	2.9	3.0	3.3	V
Sync Reference (Sync)						
Supply Voltage	Vdd	Sync = 5V		5		V
Sync high threshold	Vshth	Vdd = 5V	2.3	2.5	2.7	V
Sync low threshold	Vslth	Vdd = 5V	0.6	0.7	0.8	V
MOSFET Gate Driver (Out)						
Output high Voltage	Voh	Vdd = 5V	4.8	4.9	5.0	V
Output low Voltage	Vol	Vdd = 5V	0.0	0.1	0.2	V
Propagation delay	Td	Vdd = 5V	15	20	25	ns
Rise time	Tr	Load = 10nF to GND	30	50	70	ns
Fall time	Tf	Load = 10nF to GND	20	30	40	ns

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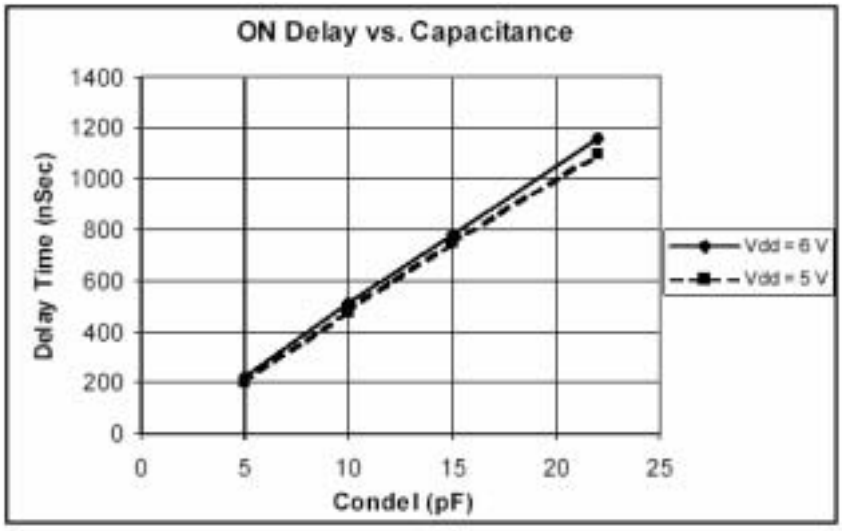
APPLICATION INFORMATION

Vdd Decoupling Capacitor

The IC is somewhat sensitive to supply voltage ripple. If very large, or several large MOSFETs with significant Ciss are driven by the IC, then the ripple due gate drive energy transfer can create large ripple. Therefore it is recommended that a Vdd to Gnd 10 uF high frequency decoupling ceramic capacitor be used. The SP6003 is designed to drive 30 nF in 25 nanoseconds. If higher drive capability is needed, then it is recommended that a totem P-Channel/N-Channel pair be used as a driver between the SP6003 and the MOSFET or parallel MOSFETs. If the additional driver is used, then it is recommended that the decoupling capacitor be place in close proximity to the driver.

Adjusting ON Delay

The ON delay is adjusted by the value of capacitance connected from GND to Pin ON Delay on the SP6003. The required capacitor value is highly dependent on the transformer reset method. Forward converters can be reset by 1) diode method, 2) passive RC method, or 3) active method. The suggested starting value for the ON Delay Capacitor is 1/2 the Ramp Capacitor.



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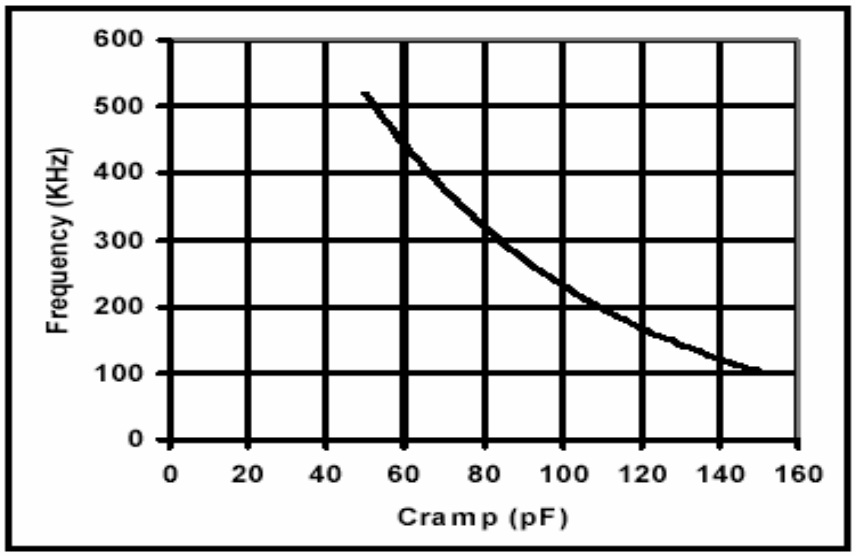
Ramp Capacitor Selection

Ramp capacitor selection is frequency dependent. Capacitance selection should be made in according to the plot below :



The ramp capacitor selection is dependant on the Range of the On and OFF times of the Catch synchronous MOSFET. In most application it is necessary to work to a narrow duty cycle. The ramp capacitor voltage charges from about 0.7 volts during the catch ON time. The charging current is 80 mA. For proper operation of the internal timing it is necessary to limit the ramp amplitude to 3.8 Volt. This voltage limit and the maximum Ramp on Time sets the minimum size capacitor needed. Since it is usually desirable to achieve proper operation down to essentially zero duty cycle, the capacitor minimum size can be represented as a function of frequency.

Cmin = Icharge*dT/dvV = Icharge/F/dV
Since Icharge= 80µA and dV=3.8-0.8
Cmin=2.66*10-5/F

A capacitor size should be selected that meets the above should be selected that meets the above criteria including the frequency tolerance and the capacitor tolerances over temperature. The criterion for the maximum suitable capacitance is less precise because it is more driven by noise constraints. If a larger capacitor is chosen, the ramp voltage becomes lower and there is more jitter on the pulse width due to noise. It is usually advantageous to operate with as high a ramp voltage as possible for this reason. The minimum ramp amplitude occurs at the maximum converter operating duty cycle because this is when the catch is conducting for the shortest period of time..

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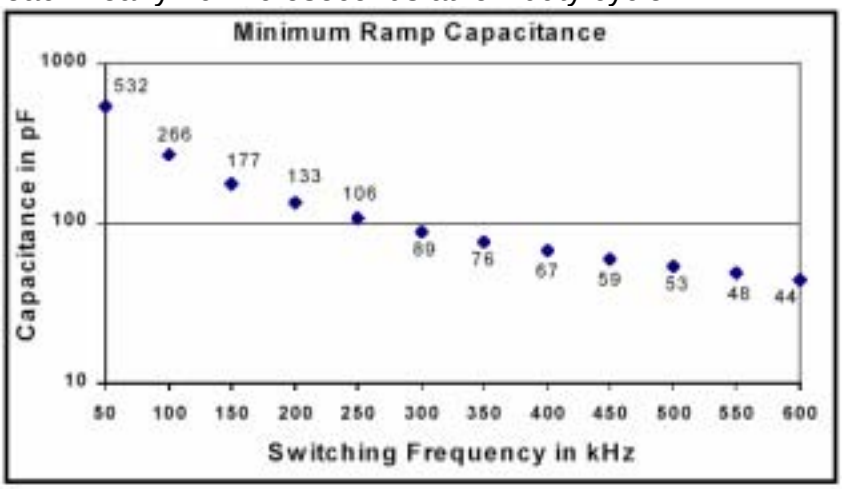
In a transformer isolated forward converters for example that operates to 50% maximum duty cycle, the minimum ramp amplitude would be 1/2 of the maximum possible ramp amplitude. In this case a maximum and a ramp capacitance of up to 4 times the minimum can still give adequate ramp amplitude. For converters that need to be able to operate to a wider duty cycle the maximum capacitance should be closer the minimum calculated above to prevent noise problems

For 200 kHz to 400 kHz operation, a ramp capacitor value of 150 pF is recommended. This allows the Catch ON time to reach 7.6 microseconds for narrow pulse widths (about 4.5 microseconds of Catch ON time at narrow duty cycle).

For operation from 100 kHz to 200 kHz, a larger ramp capacitor is needed. If the ramp capacitor is too small, then this will allow the internal ramp to saturate and not provide proper timing. For 100 kHz to 200 kHz, the recommended value for the ramp capacitor is 330 pF. This allows the Catch ON time to reach nearly 10 microseconds at low duty cycle.



Adjusting Tdvdt timing

The Tdvdt pin provides adjustment of the proprietary dv/dt filter circuit that differentiates between the real power and ring-back no-power transformer secondary voltage positive waveform. Under light or no load voltage positive waveform. Under light or no load ,for that condition the transformer voltage “rings” back positive. The SP6003 detects positive transformer secondary voltage to establish power transmission, and determines the SR MOSFET turn ON time. However, it is not desirable to turn on the MOSFET during the “ ring-back”. The dv/dt filter detects the true power pulse from the “ring-back by measuring the voltage waveform dv/dt. A very fast dv/dt is interpreted as true power pulse. A slow dv/dt is interpreted as “ring-back”.
However the “normal” power pulse rise time may be well above or below the nominal dv/dt threshold setting., Pin(Tdvdt), provides some adjustment for those cases. There are three possible connections.

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The first is nominal setting. For this condition, Pin(Tdvdt) is left open or no connection.
For the case where the power pulse rise time is much slower than nominal, connect a 47 k ohm resistor from Pin(Tdvdt) to Vdd.
For the case where the power pulse rise time is much faster than nominal, connect a 47 k ohm resistor from Pin(Tdvdt) to GND.
The table below summarizes the typical rise time that can be achieved with the various connections to Pin(Tdvdt).

Pin(dv/dt)Connect	Typical Rise Threshold
	(nanoseconds)
1K ohm to Vdd	25
Open	50
1K ohm to GND	100

Sync Pin

Pin (Sync), the Sync input terminal, is clamped internally to the Vdd supply if pulled to a voltage higher than Vdd. There fore a 1 K ohm resistor should be placed in series with the sync signal and Pin (Sync). The 1 K ohm resistor allows for sync voltages up to to 20V. The datasheet is misleading regarding this point as some early version of the IC included an internal resistor. For production devices that are now available, an external resistor must be used for sync voltages above Vdd. Your sync signal resistor divider will only be necessary if your sync voltage exceeds 20 volts.

Rapid Adj Pin

The Rapid Adjust circuit initiates a delay to assure that the drive circuit will not false trigger when there is a very fast reduction in pulse width required in the pulse width modulation. This can occur in regulators for very high di/dt load changes demanded by such loads as microprocessors. False triggering could result in a high cross conduction current for a few nanoseconds. The capacitor, Cra, connected to the Rapid Adj. pin sets the amount of filtering. For most applications, a value of 100 pF is appropriate.

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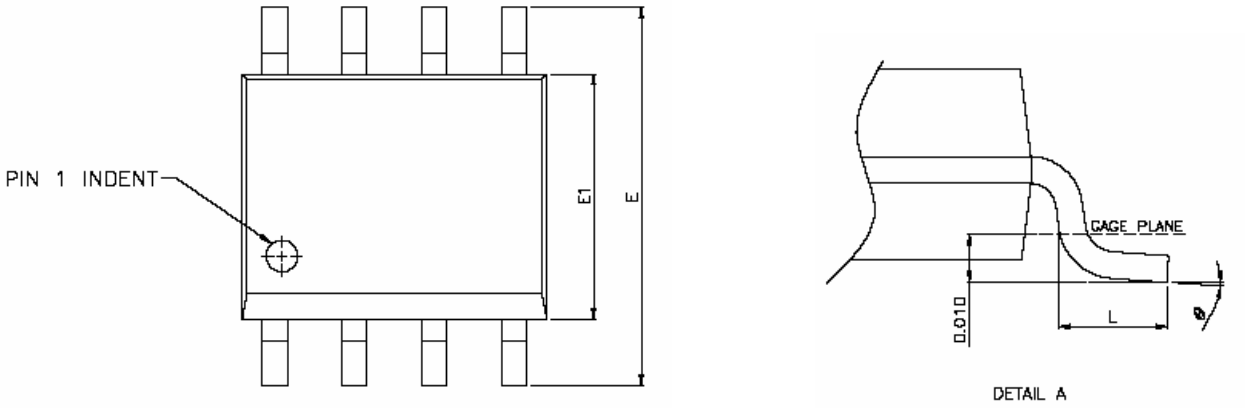
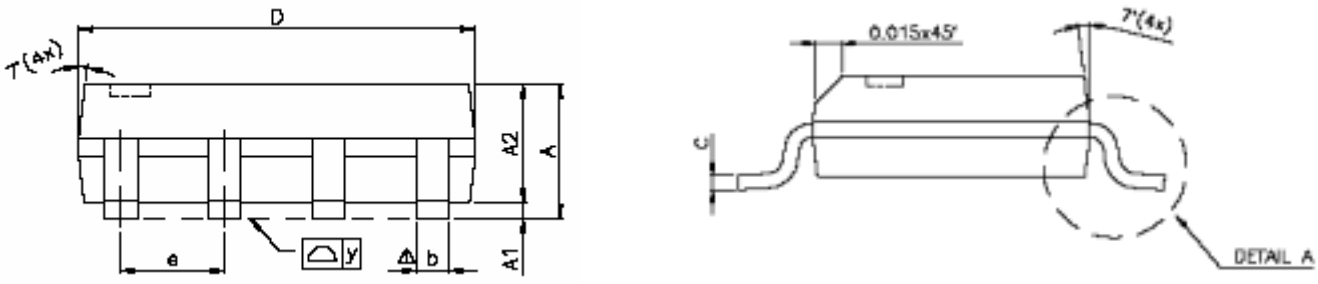
SOP- 8 PACKAGE OUTLINE





SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.47	1.60	1.73	0.058	0.063	0.068
A1	0.10	——	0.25	0.004	——	0.010
A2	——	1.45	——	——	0.057	——
b	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.0098
D	4.80	4.85	4.95	0.189	0.191	0.195
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e	——	1.27	——	——	0.050	——
L	0.38	0.71	1.27	0.015	0.028	0.050
2 y	——	——	0.076	——	——	0.003
θ	0°	——	8°	0°	——	8°

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