International
IOR Rectifier

APPLICATION NOTE AN-1018

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Using The IR40xx series SMPS IC's

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TOPICS COVERED

1) INTRODUCTION

The IR40xx series are small IC's which contain a MOSFET and a switched mode power supply control IC in a single package. The devices are designed primarily for use in Flyback converter topologies.

The control IC is designed to allow for two modes of operation:

i) Quasi-Resonant Mode - uses the primary inductance and an additional capacitor to provide a resonant signal used to control the switch on of the MOSFET at a point when the drain-source voltage is at a minimum, thereby reducing power dissipation.

ii) Pulse Ratio Control (PRC) Mode - This mode of operation controls the power by adjusting the MOSFET on time, and keeping the MOSFET off time fixed.

It is clear that both of these methods operate with a variable frequency. In the case of PRC mode the maximum frequency will occur when there is a light load at high line voltage, and the frequency will be approximately twice that at full load low line voltage. For Quasi-resonant mode again the maximum frequency would be highest at light load and high line voltage (but could be significantly higher than the minimum frequency if the load range is wide). Some devices are optimized particularly for use in Quasi-resonant mode and some are optimized for use in PRC mode .

Quasi-resonant mode works best with power supplies where the load does not have a wide current range. PRC mode would be best used where a low current standby mode may be required.

2) FEATURES

- Small 5 pin SIP or SMD package is suitable for low-height type power supplies.
- low operation circuit current before start-up. (100μA Max)
- Built-in oscillator for PRC operation at low frequency
- The oscillator is designed for 20kHz PRC operating frequency at light load (standby). (or 67kHz for PRC optimized device)
- Active low-pass filter for improved stability at light load.
- **Avalanche energy guaranteed MOSFET with high VDSS**.
- Built-in soft start circuit
- Regulated gate drive
- Adjustable switching speed by external components for EMI control
- Temperature compensated pulse-by-pulse overcurrent protection (OCP)
- Latched overvoltage protection (OVP)
- Latched thermal shut down protection (TSD)

3) BLOCK DIAGRAMS

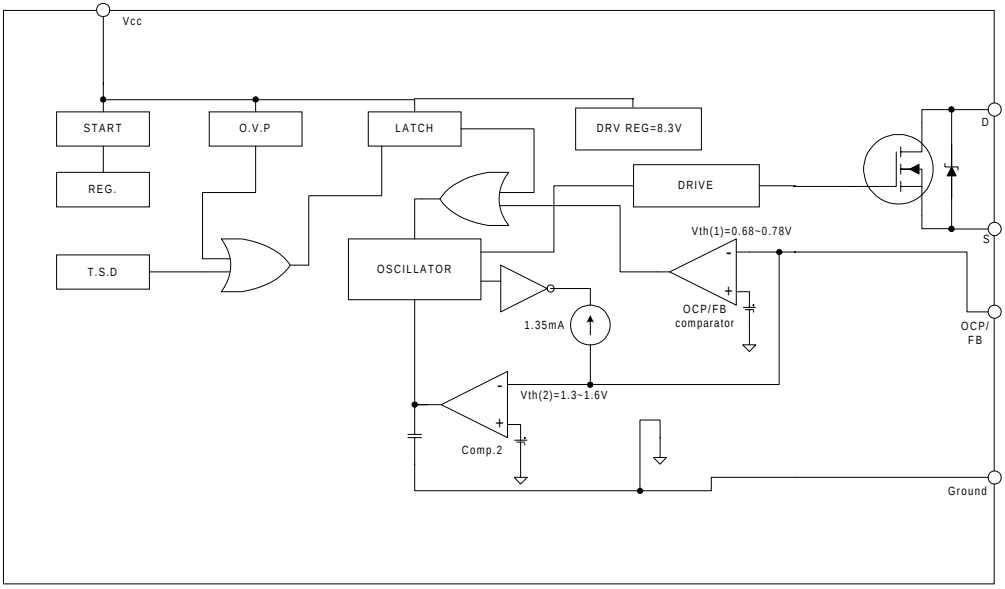


Fig 1) Block Diagram of Quasi-Resonant ISMPS IC

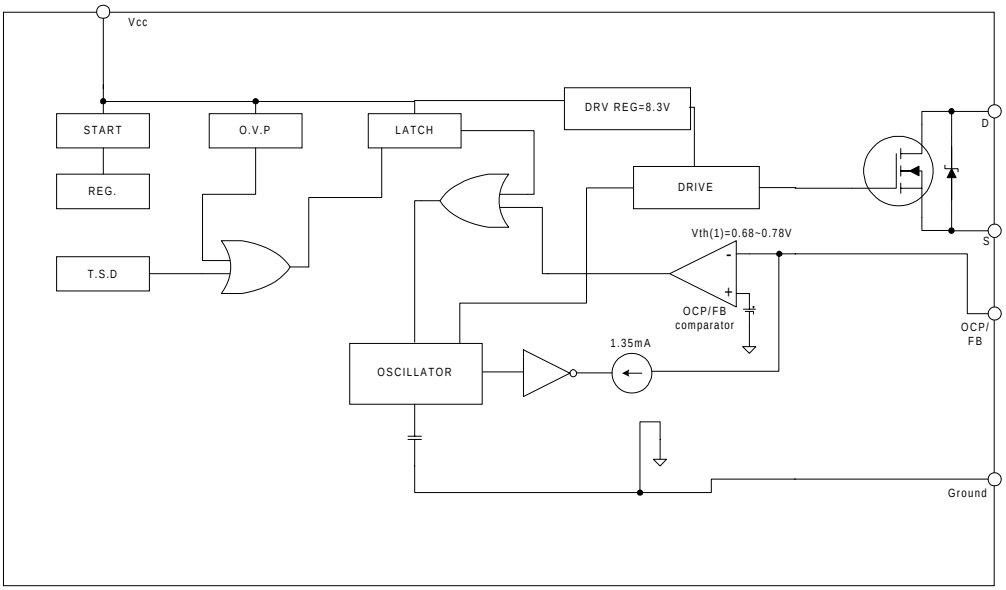


Fig 2) Block Diagram of PRC ISMPS IC

Pin Functions

Pin	Symbol	Functions
1	GND	Ground Terminal for Control IC
2	Vcc	Power Supply for Control IC
3	D	Drain Terminal of Power MOSFET
4	OCP/FB	Input for Overcurrent and Voltage feedback
5	S	Source Terminal of Power MOSFET

Other Functions

Symbol	Function
O.V.P.	Built-in overvoltage protection circuit
T.S.D.	Built-in thermal shutdown circuit

4) START UP CIRCUIT AND Vcc BIAS SUPPLY

The start-up circuit monitors the voltage at the Vcc pin, and starts and stops the operation of the control IC. The power supply (Vcc pin) of the control IC uses a circuit as shown in Fig.3).

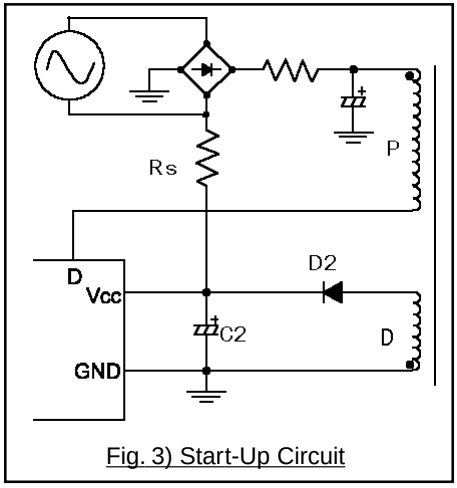


Fig. 3) Start-Up Circuit

At power on, C2 is charged through the start-up resistor Rs. The Rs value (due to the slight increase of the latch circuit holding current to 400µA Max at low temperature) should be determined so that 500µA and higher current shall flow at the minimum input voltage.

However, too large a value for Rs will lead to a lower current being available to charge C2 at low line input, and a longer time will be required to reach the start-up voltage. Thus, the Rs value should be examined as well as the C2 value that will be mentioned later. The Vcc voltage falls immediately after the control circuit starts its operation, but the drop in voltage can be reduced by increasing the C2 capacitance. However, if the C2 capacitance is too large, the time delay from power on to start-up becomes longer since it takes longer to charge the C2 capacitor. In a general power supply, C2 is 22~100µF, Rs is in the range 47KW~68KW (for universal input and 110V input) and 82KW~150KW approximately (for 220/230V input) for start-up.

As shown in Fig.4) , the circuit current is suppressed to 100µA Max (at Vcc=14V, Ta = 25 degrees C) until the control circuit starts its operation. Therefore we can now see that it is possible to use a start-up resistor with high resistance in order to keep the power loss in this resistor at around 25mW. When the Vcc voltage reaches 16V(TYP), the circuit comes out of undervoltage lockout, starts operation and the current consumption is increased to about 30mA. When the Vcc terminal voltage drops lower than 10V (TYP), the control operation is suspended by the UVLO (Undervoltage Lockout) function and returns to the start-up state.

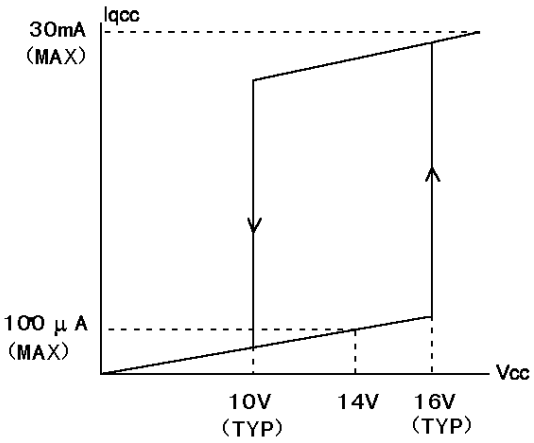


Fig. 4) Vcc Voltage/Current Characteristic

After the control circuit starts its operation, the IC's power is supplied by smoothing and rectifying the voltage output of the drive (or bias) winding D on the main flyback transformer. An example of the Vcc voltage waveform is shown in Fig.5). The drive winding voltage does not increase to the set voltage immediately after the control circuit starts its operation. Initially after the control circuit starts to operate the Vcc voltage starts falling. After a short delay the bias winding will start to take over and supply the Vcc current before the voltage drops to the UVLO- threshold voltage of 11V(MAX) (NOTE: the Vcc capacitor should be large enough to hold the voltage at Vcc above the UVLO- threshold until the bias winding starts to supply the circuit). The number of turns required for the bias winding is determined in order that the voltage on the Vcc capacitor (C2) will be above the UVLO- threshold [Vcc(OFF) 11V(MAX)] and be below the OVP operating voltage [Vcc (OVP) 20.5V (MIN)].
The standard voltage of the drive winding is approximately 18V.

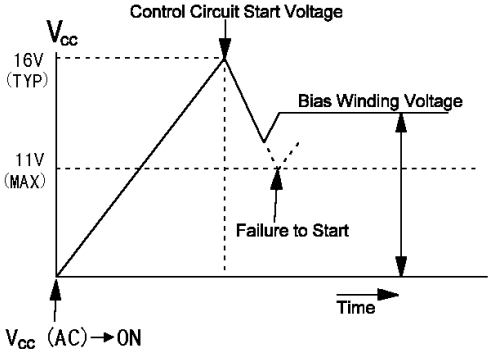


Fig. 5) Waveform of Vcc Voltage at Start-Up

In actual power supply circuits, the Vcc voltage may vary with changes the secondary side output current as shown in Fig. 6). This is because C2 is peak charged by the surge voltage generated instantaneously at MOSFET turnoff . In that case, adding a resister having several to several tens of ohms (R8) in series with the rectifier diode is effective in minimizing this phenomenon. The optimum resistance value for this additional resister should be determined in accordance with the specs of transformer that is actually used (the surge voltage is generated by the leakage inductance of the primary winding). Furthermore, the variation in Vcc voltage becomes worse due to the miss-matching of the primary-secondary coupling for the transformer and the coupling between the bias winding D and main output winding . Thus, in designing the transformer, the winding position of the bias winding D should also be considered carefully. Usually it is best to place the main output winding between the primary winding and the bias winding, for best coupling, and a split primary will help to reduce leakage inductance.

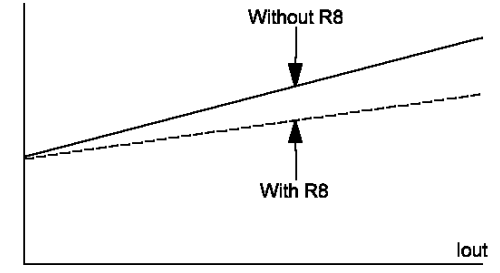


Fig. 6) Output Current Iout vs Vcc Voltage

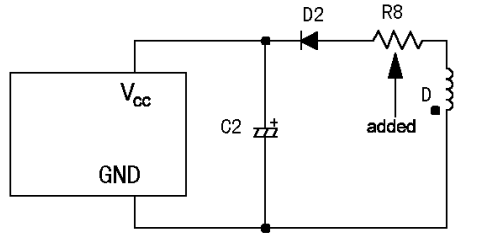


Fig. 7) Bias Supply Circuit with Minimum Output Current Dependency

5) Feedback & Control Circuit Operation

5.1) Oscillator and Primary Current Mode Control

The oscillator makes use of charging and discharging capacitor C1 incorporated in the IC and generates pulse signals to determine the OFF-time of the MOSFET. The control operation is made by the PRC operation (Pulse Ratio control) fixing the OFF-time of the MOSFET (at about 50µsec) and varying the ON-time.

Fig.8) shows how the oscillator works when the IC operates without voltage control feedback. When the MOSFET is on, the built-in capacitor C1 is charged at the constant voltage (about 5.6V). The drain current I_D flows through R5 creating a voltage drop VR5, this voltage has a saw-tooth waveform like that of the drain current I_D (which like the drain current has a gradient dependant on the input voltage and the primary inductance). The VR5 voltage is fed back into the OCP/FB pin to monitor the primary current (this forms the Primary Current Mode Control). When the voltage at the OCP/FB pin reaches the threshold voltage Vth (1) (nom= 0.73V), the comp.1 changes state, and the MOSFET is turned off. When the MOSFET is turned off, C1 charging is released and C1 begins discharging at a constant current rate .The C1 voltage starts falling at a gradient determined by the value of C1 and the constant current discharging circuit. When the voltage of C1 falls to around 1.2V, the oscillator output is reversed again and the MOSFET is turned on, C1 is quickly charged to around 5.6V and the MOSFET continues oscillating by repeating the above cycles. As described in the above, the time determined by the gradient of VR5 (I_D) is the On-time of the MOSFET. Also the fixed time determined by C1 and the constant current discharging circuit is the Off-time of the MOSFET. The fixed time is adjusted to be around 50µsec by the constant current discharging circuit.

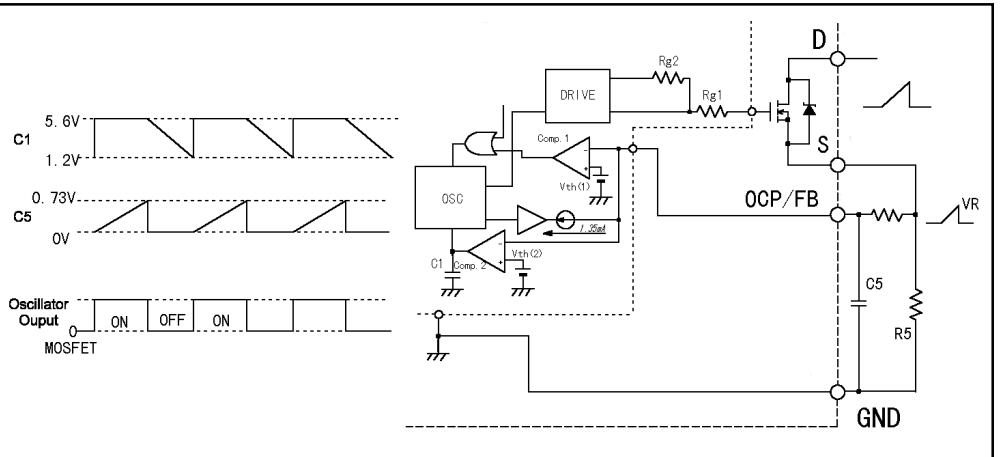


Fig. 8) Oscillator Operation of the Switched Mode Power Supply

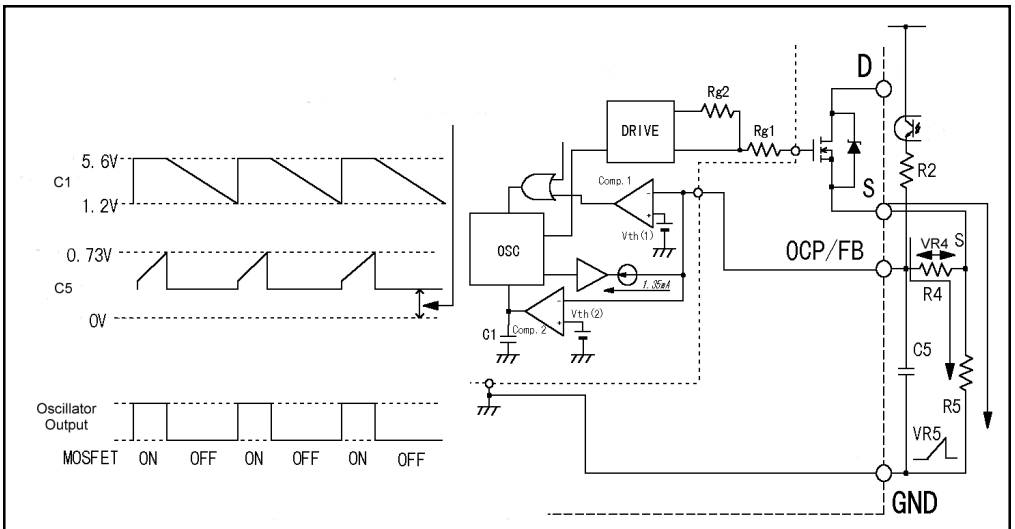


Fig 9) Oscillator Operation with Voltage Control Feedback

5.2) Secondary Voltage Mode Control

The control for the secondary side output is made by voltage mode control. An excess voltage at the output is designed to cause a current flow in the LED of an optocoupler. This leads to a feedback current (proportional to the excess output voltage) through the optocoupler's transistor, which in turn flows through R4 and R5 creating voltages VR4 and VR5. The VR5 voltage (peak value of I_D) required to reverse the Comp.1 is now controlled by VR4 (generated by the FB current). Therefore as can be seen in fig 10) the voltage (VR4) across R4 causes a DC offset voltage at the OCP/FB pin, which will reduce the ON time of the MOSFET by reducing the time taken for the voltage at the OCP/FB pin to reach the Vth (1) threshold of 0.73V. This results in a reduced energy stored in the flyback transformer. Generally the bias from VR4 is increased at light load, and the noise caused by the surge current at the MOSFET turn-on can result in malfunction of Comp.1. In order to avoid this problem, the impedance between OCP/FB and GND terminal needs to be reduced by an Active Low-Pass Filter circuit while the MOSFET is turned off. The active-low-pass filter circuit is made of a 1.35mA constant current bypass circuit between OCP/FB terminal and GND terminal, and it reduces the impedance of the OCP/FB terminal to around 1/2 until the MOSFET is turned on. Thus C5 absorbs the noise caused at the MOSFET turn-on.

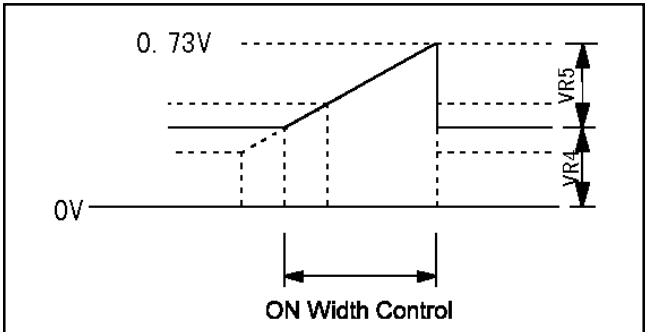


Fig 10) Effect of DC Bias From Voltage Control Feedback

5.3) Overcurrent Protection (OCP) Circuit

This is a pulse-by-pulse overcurrent protection circuit that detects the peak of the drain current of the MOSFET in every pulse and reverses the oscillator output. The overcurrent detection circuit is shown in Fig.9).

The MOSFET drain current is detected by putting the voltage drop of a series current sense resistor R5 connected between the source terminal of the MOSFET and the GND terminal into the OCP/FB terminal. The threshold voltage Vth (1) of OCP terminal is set at around 0.73V to GND. The external components, R4 and C5 are a filter circuit to avoid malfunction which may be caused by the surge voltage at the MOSFET turn-on (caused by the surge current through the current sense resistor due to discharging of the resonant capacitor, in quasi-resonant designs, and the parasitic winding capacitance of the primary winding.

The output characteristics of the secondary side at the time when the overcurrent protection circuit operates, due to the overload of the secondary side, becomes as shown in Fig 11). When the output voltage drops under the overloaded circumstances, the bias drive winding voltage also falls proportionally, and the Vcc terminal voltage falls below the UVLO- threshold voltage to stop the operation (this may not happen if the Vcc capacitor is too large, do not over smooth this voltage). In that case, as the circuit current drops simultaneously, the Vcc voltage rises to the start voltage and the circuit operates intermittently.

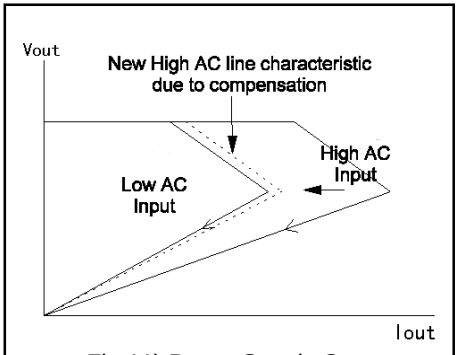


Fig 11) Power Supply Output Overload Characteristics

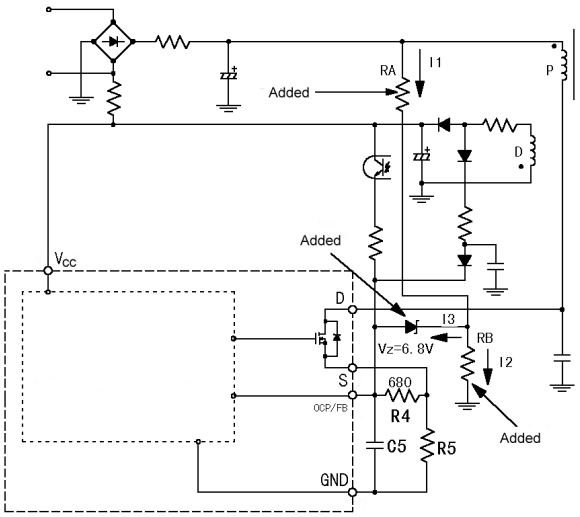
If the transformer has multiple output windings with insufficient coupling, even if the secondary output voltage drops in overload circumstances, the operation may not become intermittent because the primary winding voltage may only change by a small amount. First improve the coupling, and if this still does improve the overload operation, a secondary overload protection circuit may be required.

In the IR40xx series, the drain current of the MOSFET is detected for overcurrent protection. This causes a high output power with a high AC input voltage when the overcurrent protection limit is reached as shown in Fig.11). To reduce this effect a feed forward bias circuit consisting of two resistor and one zener diode can be added as shown in Fig.12). This improves the operation at high AC line input to the dotted line in Fig.11), and reduces the output power at overload.

The two advantages of this additional circuit are:

(1). When the input voltage is high, the average MOSFET drain current is reduced to a low level due to the OCP/FB pin offset voltage from the bias circuit. This results in a lower voltage stress on the MOSFET, as the primary voltage spike (due to the primary leakage inductance) is reduced by having a lower drain current, and therefore lower inductor current.

(2). The output components on the secondary side (rectifier and capacitor) are less stressed as the power is controlled to a certain degree.



$$RA = 680 \times \frac{\frac{VIN(DC)MAX - VIN(DC)MIN}{0.73}}{IDpeak(VinMIN) - IDpeak(VinMAX)} \Big/ IDpeak(VinMIN)$$

$$RB = \frac{RA \quad (6.8+0.73)}{VIN(DC)MIN - (6.8+0.73)}$$

IDpeak(VinMAX):
Drain current at full load, and max input voltage

IDpeak(VinMIN):
Drain current at full load, and min input voltage

VIN(DC)MAX: maximum DC bus voltage

VIN(DC)MIN: minimum DC bus voltage

Fig 12) OCP Feed Forward Compensation Circuit for Input Voltage

5.4) MOSFET Drive Circuit

The MOSFET gate drive circuit uses a zener diode ZD1 (V_{DRM}= 8.3V typ) to create a constant voltage gate drive as shown in Fig.13. This ensures that the MOSFET is always fully turned on.

The gate drive current at MOSFET turn-on is controlled by Rg1 + Rg2, so as to control the MOSFET turn-on rate thereby reducing switching noise. At turn off the MOSFET Gate is discharged through the resistor Rg1 to ensure a fast turn off, minimizing the switching losses.

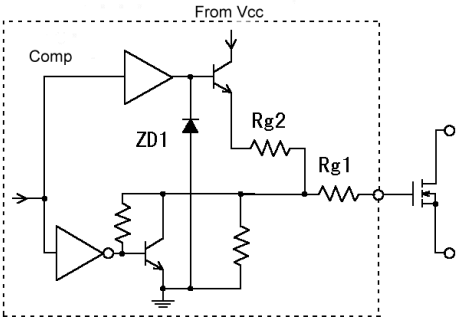


Fig 13) MOSFET Gate Drive Circuit

5.5) Latch Circuit

The latch circuit keeps the output from the oscillator low and stops operation of the power supply circuit when the overvoltage protection (OVP) or the thermal shutdown (TSD) circuits activate. The holding current for the latch circuit is 400µA maximum (Ta = 25°C) when the Vcc voltage is 8.5V. At low temperature 500µA of holding current will be required to flow from the start-up resistor into the Vcc pin. In order to avoid the possible malfunction caused by noise, etc., a delay time is provided by the latch timer circuit in the IC to activate latch circuit operation when the OVP or TSD circuit continuously operates for 8µsec and longer.

When the latch circuit is activated, the constant voltage regulator (Reg) circuit is also operating,

so the circuit current is at higher than the 500µA that can be supplied by the start-up resistor; therefore the Vcc voltage falls. When the Vcc voltage falls lower than the UVLO- threshold voltage (10V TYP) the regulator circuit stops and the Vcc voltage starts rising as the circuit current is below 400µA (Ta = 25°C). When the Vcc voltage reaches the UVLO+ start voltage (16V TYP), the regulator circuit operates, and the circuit current is increased again, causing the Vcc voltage to drop once more.

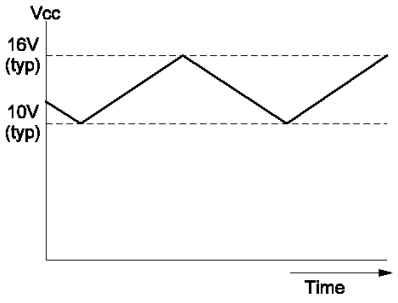


Fig.14) Vcc Voltage waveform with Latch Circuit Active

When the latch circuit is active, the Vcc voltage rises and falls within the range from 10V (TYP) to 16V (TYP) and is prevented from increasing abnormally. Fig.14 shows an example of the Vcc voltage waveform when the latch circuit is in operation. To reset the latch circuit Vcc must be taken below 6.5V, this is usually done by removing the main input power.

5.6) Thermal Shutdown Circuit

The circuit makes the latch circuit operate when the frame temperature of the IC exceeds 140? (MIN). The temperature is actually sensed by the control IC, but it also operates against overheat of the MOSFET since both the MOSFET and the control IC are mounted on the same substrate.

5.7) Overvoltage Protection Circuit

This circuit makes the latch circuit operate when the VIN voltage exceeds 22.5V (TYP), and it operates as the protection against the overvoltage at VIN terminal. The VIN terminal voltage is provided from the drive winding of the transformer, and the voltage is in proportion to the output voltage; then it also operates when the overvoltage in the secondary side is generated by the open voltage sense circuit or by some other events. In the above case, the secondary output voltage when the overvoltage protection circuit operates is obtained from:

$$V_{out\ (OVP)} \approx \frac{\text{Vout at normal Output Voltage Operation}}{\text{VCC Voltage at normal Operation}} \times 22.5V(TYP)$$

6) Quasi Resonant Operation Mode

In the IR40xx series, when the OCP/FB voltage is above the threshold voltage Vth (1) =0.73V and below the threshold voltage Vth (2), the internal comparator Comp.1 initiates PRC operation with a fixed OFF-time (TOFF = 50µsec). When it is above the threshold voltage Vth (2) = 1.45V (MAX. 6.0V), the internal Comparator Comp.2 switches the operation to Quasi-resonant mode. While the voltage is maintaining above the threshold voltage Vth (1), the MOSFET remains in OFF-state (NOTE: minimum quasi-resonant signal duration=1µsec). Hence quasi resonant operation turns on the MOSFET at 1/2 cycles of the resonant frequency (the bottom point of the voltage resonant wave after the transformer releases the energy).

An example of the power supply circuit for the quasi resonant operation is shown in Fig.15. When the resonant capacitor C3 is connected between the drain and the source it forms a resonant circuit with the primary inductance of the transformer. Adding a delay circuit consisting of C4, D3, D4, R5 between the drive winding D and the OCP/FB pin, produces the quasi resonant signals, at the MOSFET turnoff, which operate both Comp.1 and 2, and activate quasi resonant operation.

With the delay circuit, even when all the energy in the transformer is transferred to the secondary windings, the quasi resonant signals fed into the OCP/FB pin will not drop immediately. This is because C4 and C5 are discharged by the active low-pass filter (1.35mA current sink) and the compound impedance of R6 and R7. After the certain period, the voltage will drop to the threshold voltage Vth (1) and below. The delay time is set by observing the operating waveform, and

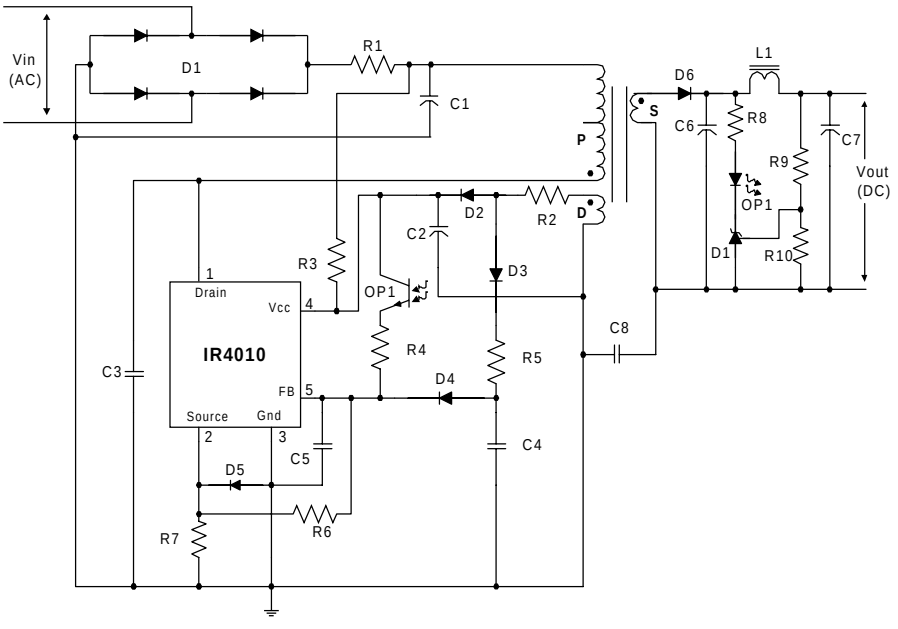


Fig.15) Example of an Application Circuit

the adjusting C4 so that the MOSFET turns on when the VDS of the MOSFET reaches the lowest point of the quasi-resonant signal (refer to Fig. 17). Thus, the delay time is determined by the discharging time of C4 and C5, even if C4 is not added, there will be some delay time. As the voltage imposed between OCP/FB pin and ground terminal is 6V (MAX), the quasi resonant signal applied must be below that voltage.

6.1) Calculating the Primary Inductance Lp of the Transformer

Designing a transformer for Quasi resonant operation is basically the same as designing for PRC type power supplies, However, due to the quasi resonant operation, and the duty varies in accordance with the TON is delayed; then it is required to compensate the duty. Accordingly the ON-duty calculated from the ratio between P winding Np and S winding Ns is set as D, the LP rating is obtained from:

$$LP = \frac{(VIN \cdot D)^2}{(\sqrt{\frac{2 \cdot Po \cdot fo}{\eta}} + VIN \cdot \pi \cdot fo \cdot D \cdot \sqrt{C4})^2}$$

Po: Maximum Output Power
fo: Minimum Oscillating Frequency
h : Power Supply Efficiency » 0.85~0.9(High Vout),0.75~0.85(Low Vout)
D: ON Duty at Minimum VIN(AC).
VIN: C1 Voltage at Minimum VIN(AC)

6.2) Delay Circuit

In the quasi resonant operation, the frequency is controlled in accordance with variations in input voltage and output load current. Therefore the oscillating frequency becomes the highest when the input voltage is at a maximum and the load is at a minimum. In that case, if the oscillating frequency is beyond the capacity of the internal oscillator, the operating conditions for quasi resonant operation will not to be satisfied.

As the minimum OFF-time determined by the internal oscillator is around 1.5µsec, the frequency which secures the OFF-time of 1.5µsec minimum should be used for the resonant frequency. Furthermore, the validity time of the quasi resonant signal should be a minimum of 1.0µsec since the internal oscillator is reset in a short interval. The validity time of the quasi resonant signal means the period when the quasi resonant signal exceeds the threshold voltage Vth (2) (1.45V) of the OCP/FB terminal as shown in Fig.16). In the IR40xx series, the control signal and the quasi resonant signal are applied to the same terminal; therefore the discharge time constant of capacitor C3 in Fig.16) that determines the delay time varies slightly due to the feedback and feedforward bias added to the OCP/FB terminal. As a result of this, at high input voltage and light load, the delay time will be slightly longer than expected. Consequently, switching loss is increased because the MOSFET is not turned on at the lowest point on the Vds waveform. Therefore the delay time has to be adjusted in order that the input power will be least with the conditions of the highest input voltage and the lowest load.

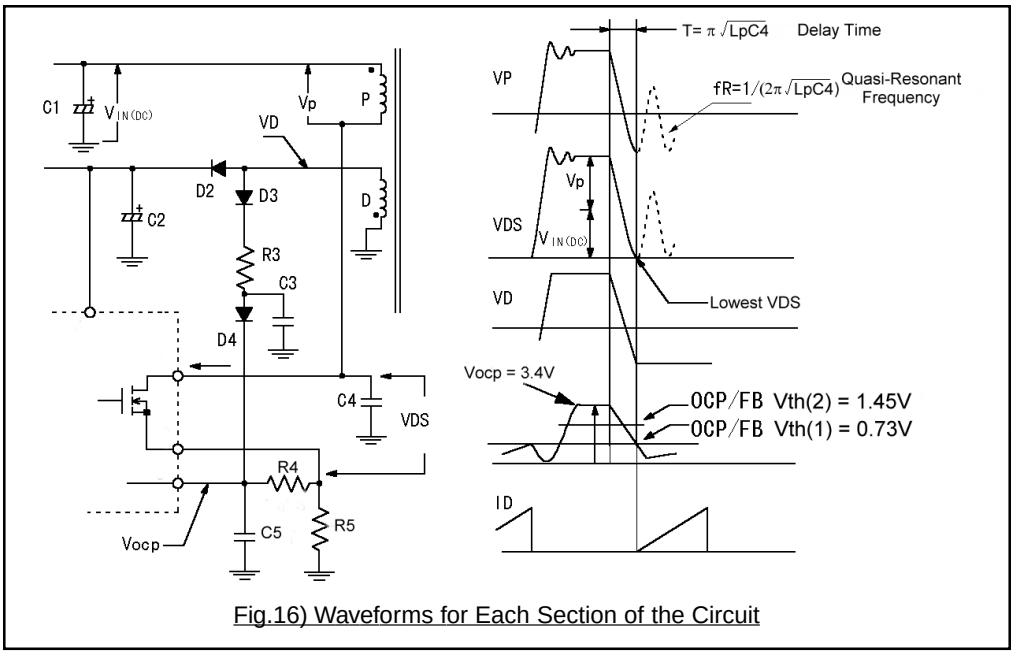


Fig.16) Waveforms for Each Section of the Circuit

6.3) How to obtain the constants of each part in Fig.16

The current (IS) for the quasi resonant signal is obtained from the compound impedance of R4 & OCP/FB terminal (internal impedance with 1.35mA constant current sink circuit) and the peak voltage of the quasi resonant signal (recommended value is 3.4V). The value of R3 is obtained from:

$$IS = 3.4 \div R4 + 1.35mA$$

$$R3 = (VD - 3.4 - 2VF) \div IS$$

$$R5 = \frac{VOCP}{ID(MAX)} = \frac{0.73(TYP)}{ID(MAX)}[\Omega]$$

VF:	Forward Voltage Drop of D3 and D4 (0.7V)
VD:	Drive Winding Voltage
ID(MAX):	Maximum Drain Current (Po = MAX, VIN(AC) = MIN)
VOCP:	OCP/FB pin voltage at the MOSFET turnoff

Resonant mode voltage and current waveforms are shown in Fig.16. The resonant frequency is obtained from:

Resonant Frequency $$f_R = \frac{1}{2\pi\sqrt{LpC4}}$$

For efficient quasi resonant operation, the MOSFET is required to turn on at 1/2 cycles of f_R. The ON delay time, T is obtained from:

TON Delay Time $$T = \pi\sqrt{LpC4}$$

6.4) Switching Between Quasi Resonant and PRC Operation

It is posssible to switch the operation of the IR40xx series quasi-resonant ISMPS IC's, so that they can operate in either Quasi-Resonant mode or PRC mode. This can be especially useful for power supplies with wide range output currents, where quasi-resonant mode can be used for near full load conditions, to reduce the power dissipation in the MOSFET, and PRC mode can be used for light load conditions, to prevent high operating frequencies, and again keep power dissipation down to a minimum.

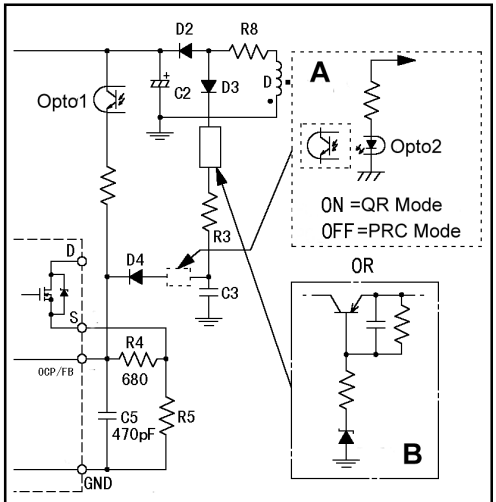


Fig.17) QR/PRC Mode Switching Circuit

Circuit A

As shown in Fig.17, the operating mode can be switched between Quasi resonant mode and PRC mode by adding Opto2 (which either enables or disables the feedback of the quasi resonant signal).

Circuit B

At light load the output voltage of secondary side will be reduced and it can be switched to PRC operation by adding the circuit B as shown in Fig.17. As the secondary output voltage drops , the drive winding voltage also drops accordingly causing the PNP transistor to turn off, thereby cutting the feedback of the quasi-resonant signal to the OCP/FB pin. Once the signal is cut, the operation is switched to PRC by the internal oscillator, and the operating frequency is reduced to 20-40kHz range approximately.

6.5) Variations of the Delay Circuit

- Circuit A
This circuit does not require lots of components, and the surge noise is reduced. But the loss from R3 is large, so the capacitance of C3 is limited. Then this type of the circuit is suitable for a power supply that has a higher voltage resonant frequency or narrow input (a single input).

- Circuit B
In comparison to the type A, a longer delay time can be set up and the surge noise is efficiently reduced. This is the basic circuit type which has the widest application in any power supplies.

- Circuit C(R3' = 1~2KO approx.)
In this circuit C3 is discharged by R3', so the variation of the delay time coming from FB constant sink current is less than that of type B. This circuit is suitable for a power supply with large load, input fluctuations and a power supply that has a wide adjustable delay time (for a universal input range TV). The value of R3 needs to be compensated because the current flowing through R3 is bypassed by R3'.

- Circuit D
The number of components is quite small and the circuit follows up to the highest frequency (around 300kHz), but the delay time is not adjustable. This circuit is suitable when the resonant frequency and the delay time are matched (pÖLp.C4»1.5µsec approx.) or when a slight increase of switching losses at MOSFET turn-on due to a time lag does not create any problems. In actual applications, it is suitable for a 110V power supply with small output or a power supply having a clamp snubber and universal input with high resonant frequency as well as small output power.

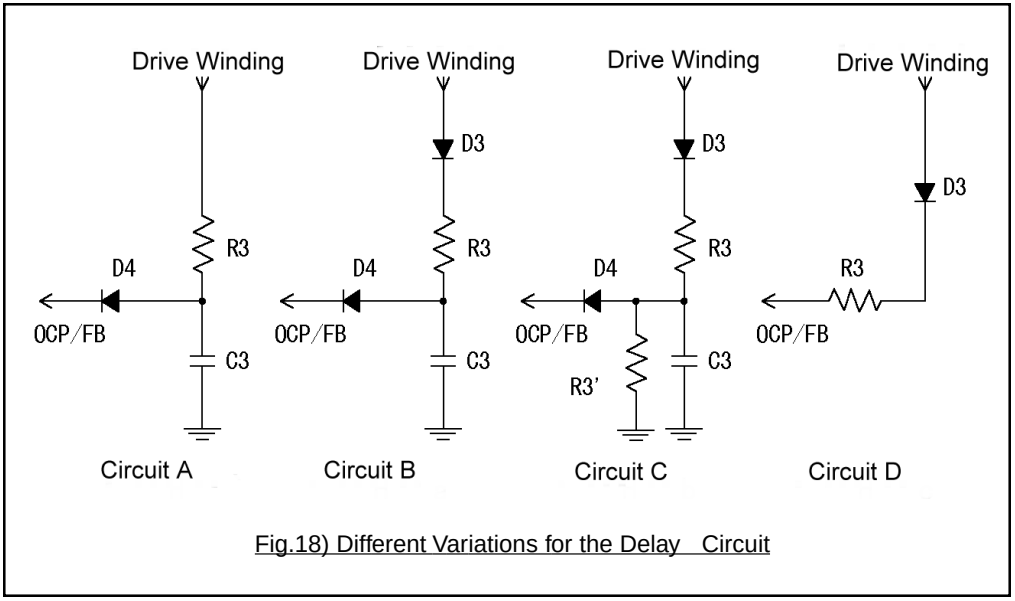


Fig.18) Different Variations for the Delay Circuit

7) Notes on Circuit Design

7.1) External Components

The current sense resistor connected between the source pin and the ground pin should be a low inductance part, with a high surge current capability. Due to the high frequency currents passing through the sense resistor, a part with reasonable inductance may cause unexpected voltage spike which lead to false triggering of the threshold within the IC. There are high frequency currents flowing in the transformer, therefore the skin effect must be taken into account. To maximize use of the conductor area, it is better to use multifilar windings (multiple strands of thin diameter wire) or Litz wire. All resonant and electrolytic filter capacitors should be rated for high ripple applications or for low impedance power supply applications.

7.2) Switching Speed Control

The switching noise caused by the current spike from discharging the resonant capacitor and the parasitic capacitance of the primary winding can be reduced by adding a ferrite bead (FB) to the source terminal . If only the ferrite bead is inserted, the switching speed is reduced not only at turn-on but also at turnoff, and will cause the switching loss to increase. In order to avoid that, adding a diode between GND and S is recommended as shown in Fig.19. This should be a high speed small signal switching diode with small junction capacitance, or a schottky barrier diode (11DQ03 etc) .

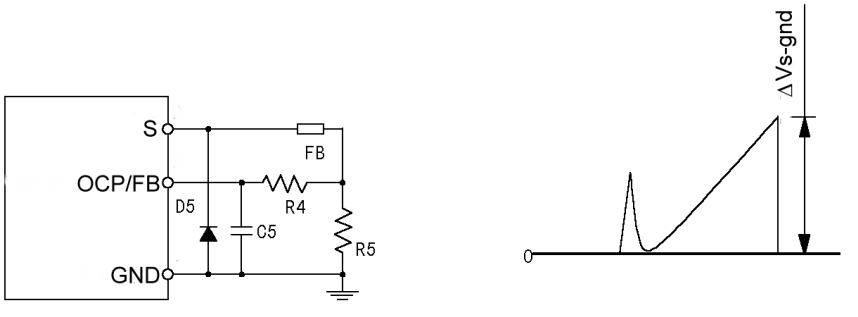


Fig.19) Switching Current Waveform

7.3) Maximum Switching Current

The voltage between the source and the GND terminal drops because the current sensing resistor and the ferrite bead for are added. Due to that voltage drop, the gate drive voltage of the MOSFET is reduced, and the maximum switching current for the operation of the MOSFET also decreases. Therefore, as shown in Fig.19, measure the voltage drop between the source and GND terminal, and derate the maximum switching current in accordance with the derating curve shown in the datasheet. Confirm that the voltage drop between the source and GND terminal and the maximum switching current are within the derating curve by measuring both at normal operation and at the operation of overcurrent protection.

7.4) Phase Compensation

In a general load specification, no primary side phase compensation is required, and the gain and phase adjustments to the precision shunt regulator circuit on the secondary side will be sufficient. If the phase compensation on the secondary side is not sufficient (the loading specification is unique or the ripple of the output filter capacitor is quite large), then it will be necessary to add the capacitor C6 (0.01 ~0.1µF. approx.) across the photo-transistor of the feedback optocoupler (Fig.20). With the addition of this capacitor, it also becomes necessary to add the diode D6 in series with the optocoupler to prevent reverse current flow through the capacitor.

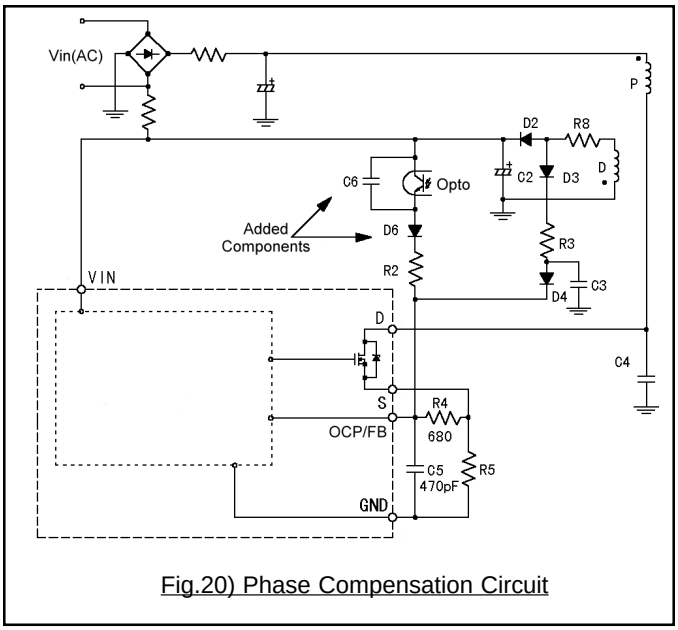


Fig.20) Phase Compensation Circuit

7.5) Operation at Light Load

The IR40xx series can have a zero ON width. Therefore at a light load, the class A operation will occur, MOSFET operates in the linear (or saturation) part of its characteristic. Typical waveforms can be seen in Fig.21. This is because the driver turns the gate drive off when the gate voltage is still rising due to a very narrow ON width. Then the voltage imposed on the transformer is controlled by the rise in the saturation voltage between the drain and source. The above condition is true for a light load condition when running in quasi-resonant mode at light load, but it may not cause any problems. Obviously at the higher frequencies with this condition the rise times are limited by the quasi-resonant capacitor and losses are increased, resulting in a reduced efficiency. This would be a good situation for switching to the PRC mode to keep the losses and the efficiencies at a reasonable level (especially with the latest energy efficiency requirements e.g. Blue Angel)

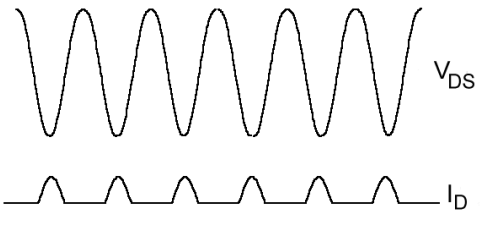


Fig.21) Class A Operation Waveforms

7.6) PCB Layout for a Quasi Resonant Switching Power Supply in using IR40xx Series

As shown in Fig.22, the track from the source pin through R5 to GND should be as short and thick as possible. The ground connections for the main supply capacitor (C1), the resonant capacitor (C4), the feedback filter capacitor (C5) and the IC ground should all be star point connected at the ground end of the source current sense resistor (R5). This will minimize the noise caused by ground currents. The recommended track width is 1mm/1A minimum. If C2 is located a distance form the IC, an additional decoupling capacitor C2' (0.01~0.1µF. approx.) should be connected near the IC.

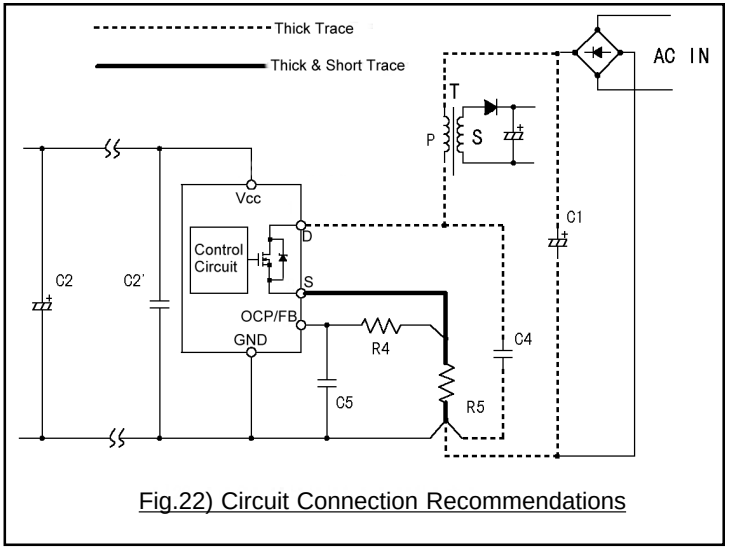


Fig.22) Circuit Connection Recommendations

If the PCB layout and mounting guidelines are not implemented properly noise and losses will be introduced which could lead to malfunction. Like the principle of "thicker and shorter", the line impedance should be lowered by making thicker traces where a high frequency current flows and making shorter wiring between components. As shown in Fig.23 where a high frequency current makes a loop, the pattern should be designed in order the area inside loop (the shaded area) will be minimized. Wherever possible larger tracks are preferable to minimize parasitic inductance, and assist in the thermal radiation, in some cases this will not be possible due to minimum clearances required for safety requirements. Keep high current carrying tracks away from the feedback or signal tracks to minimize coupling.

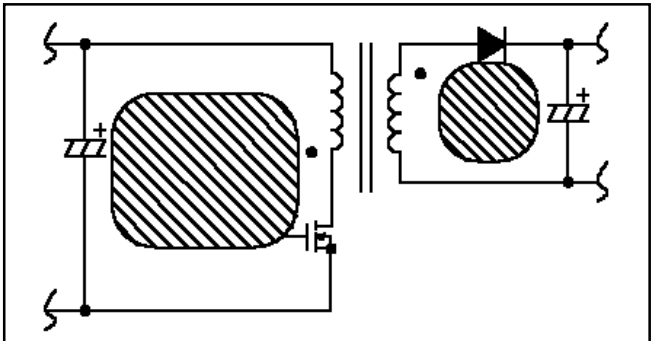


Fig.23) Example of High Frequency Current Loops