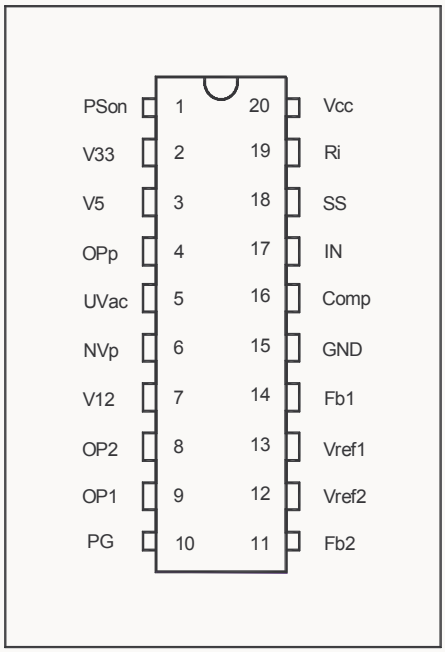
Using the SG6105 to Control a Half-Bridge ATX Switching Power Supply **SG6105**

ABSTRACT

This document relates to an ATX switching power supply using the SG6105 as the secondary-side controller in a half-bridge topology. The SG6105 can regulate an output voltage by providing PWM signals to drive a transformer. The SG6105 also serves as a supervisor to monitor and protect the 3.3V/±5V/±12V outputs. Two internal TL431 shunt regulators serve as the feedback regulators for the 5V standby voltage and the +3.3V main output. Many other protection and supervisor functions are also described for an ATX switching power supply.

PIN CONFIGURATION



FEATURE OVERVIEW

- Highly-Integrated
- Few External Components Required
- Over Voltage Protection (OVP) at 3.3V/5V/12V
- Under Voltage Protection (UVP) at 3.3V/±5V/±12V
- AC-Input Under Voltage Protection
- Anti-Lockout during Input Disturbances
- Short Circuit Protection
- Over Power Protection (OPP)
- Power-Down Warning Signal
- PSON Signal for Remote ON/OFF
- Power-Good Signal
- Delay Time for PSON and PG Signals
- 2 Shunt Regulators with 1% Tolerance
- Hiccup Mode Shutdown Protection
- Soft-Start
- Maximum 93% Duty Cycle

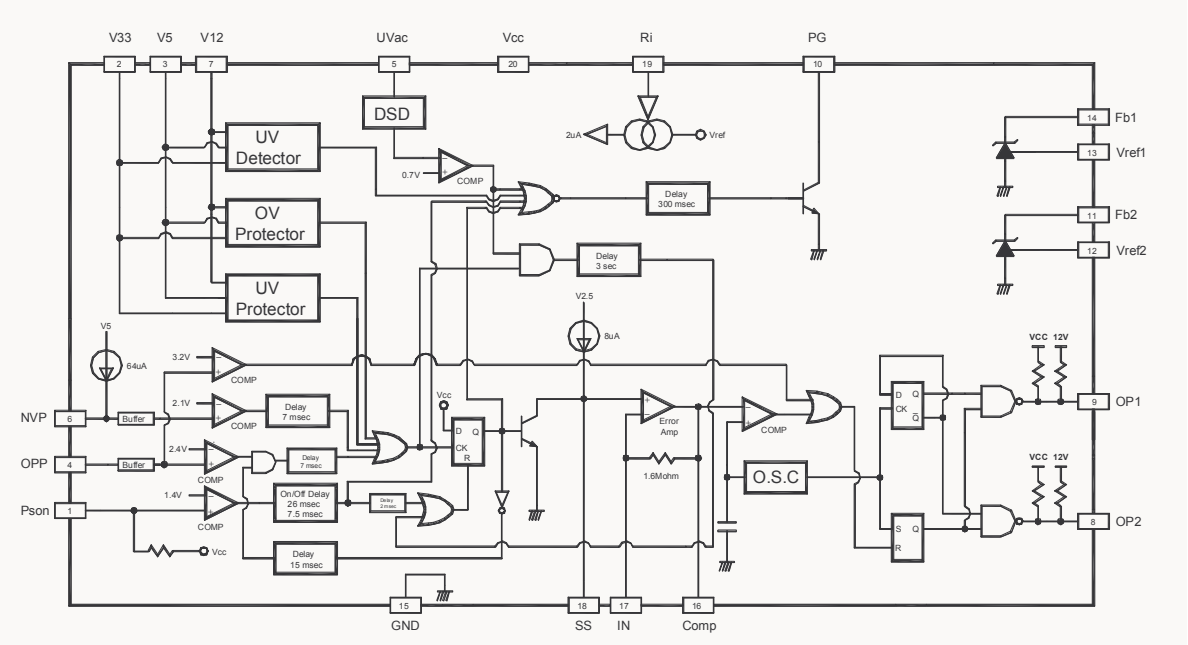


Figure 1. The SG6105 Block Diagram

DESCRIPTION

Fig. **2** shows a simplified schematic diagram of an ATX switching power supply using a half-bridge topology. The SG6105, a secondary controller, can regulate an output voltage of the power supply by providing PWM signals to drive a transformer. The SG6105 also serves as a supervisor to monitor and protect the 3.3V/±5V/±12V outputs. As shown in Fig. **3**, an additional AC/DC converter using flyback topology is required to provide a 5V standby working voltage to the SG6105 and a 12V signal to drive the gate transformer during start-up.

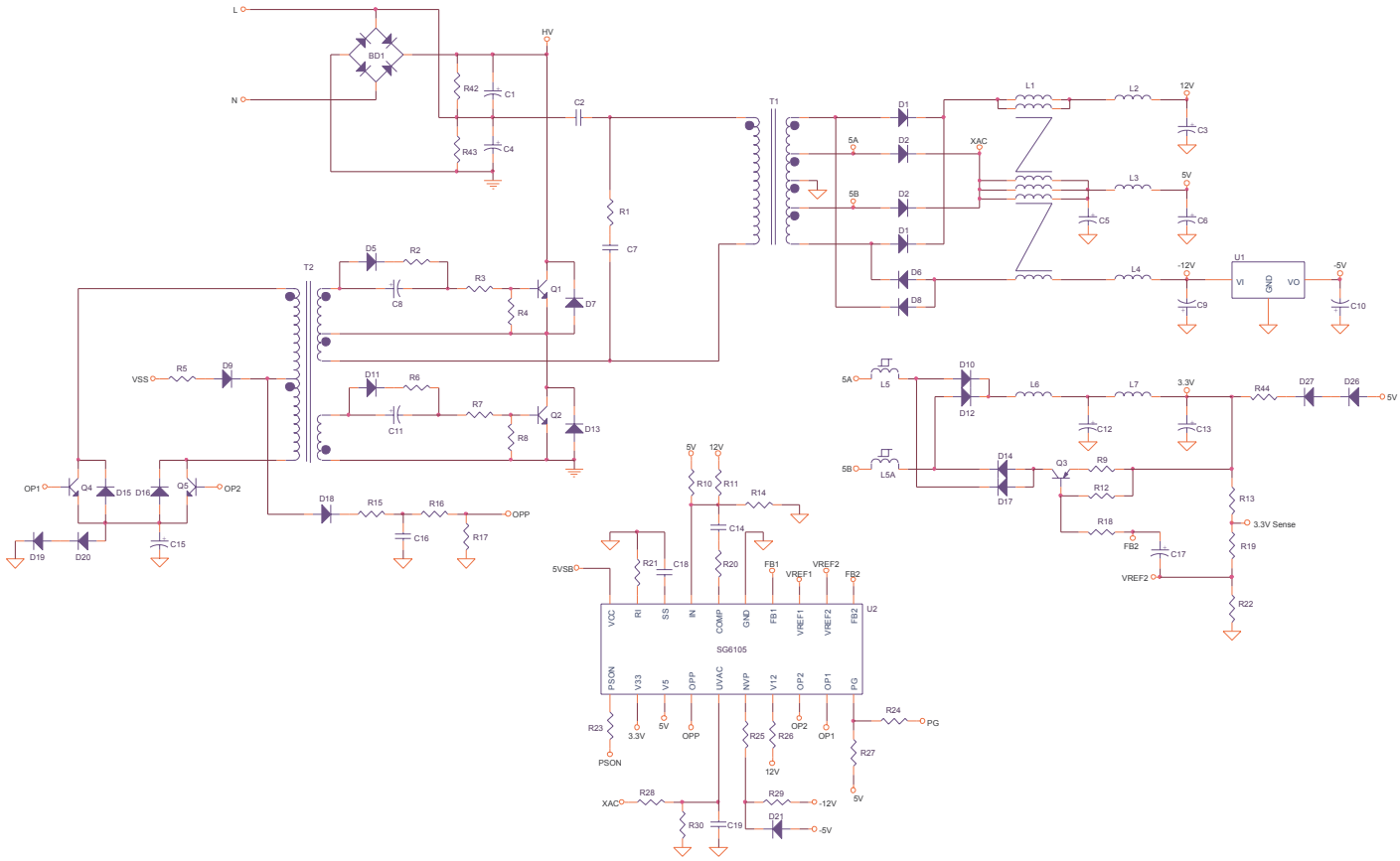


Figure 2. A Multi-Output ATX Switching Power Supply Circuit using the SG6105

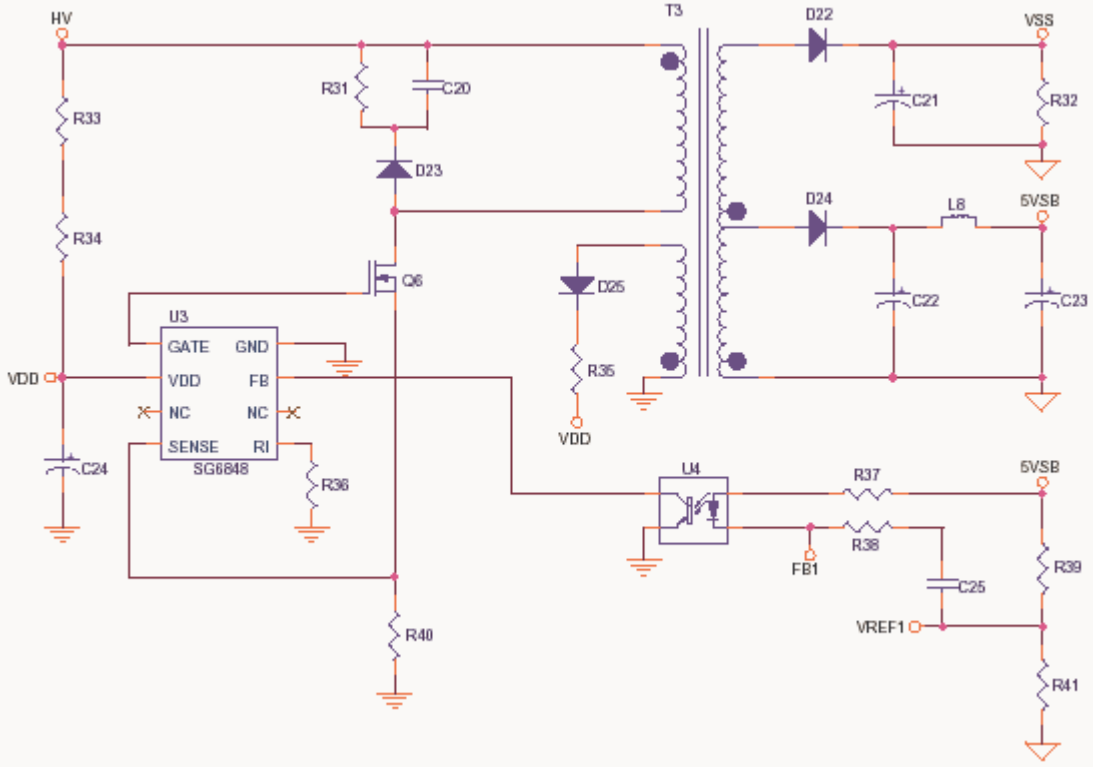


Figure 3. The 5V Standby Power Supply using the SG6848 and the Internal Shunt Regulator of the SG6105

PIN DESCRIPTIONS AND APPLICATION CIRCUITS

Pin 1 (PS_{ON})

The PS_{ON} logic input is an active-low signal that enables remote control from the CPU board. Connecting a 20kΩ pull-high resistor between Vcc and the PS_{ON} pin is highly suggested. Fig. 4 shows a typical timing diagram for the SG6105.

When PS_{ON} is pulled low, the soft start (SS) voltage will be enabled following a 26-millisecond delay, and the main power outputs (3.3V/±5V/±12V) will be powered up gradually. When PS_{ON} is pulled high, the main outputs will be turned off following a 35-millisecond delay, while the 5V standby power supply will continuously provide standby power to the CPU board and housekeeping power to the SG6105.

In applications where an active power factor correction (PFC) circuit is necessary, a turn-on delay for the standby power supply is recommended, so that the SG6105 will not be enabled until the primary bus voltage of the bulk capacitor is established.

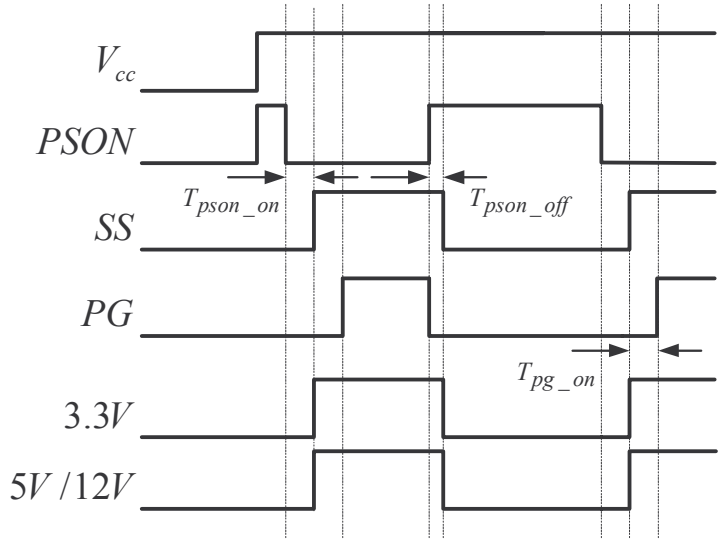


Figure 4. The SG6105 PSON Timing Diagram

Pin 2/ Pin 3/ Pin 7 (V_{33} / V_5 / V_{12})

The supervisor has inputs for the 3.3V/5V/12V power supply outputs. No additional resistors are required between these voltage outputs and the supervisor inputs. When the power supply outputs exceed their acceptable operating ranges, either under voltage protection (UVP) or over voltage protection (OVP) will be enabled. The power good signal will be pulled down and the outputs will be shut-off immediately.

Two operating modes for protection are available: latch mode and non-latch mode. In latch mode, the main output remains off even after the fault condition is cleared. To reset the latch condition, it is necessary to turn off the power source or re-cycle the PS_{ON} signal. The voltage divider ratios for the 3.3V/5V/12V supervisor inputs are 2/3/6, respectively.

One potential problem with latch-mode protection can occur during AC line disturbances. If the AC line voltage is lost for some interval, under voltage protection (UVP) may detect an under voltage condition, and the main outputs will be latched off while standby power is still live. If the hold-up time of the flyback standby power supply is longer than the line loss interval, the main outputs will remain latched off.

To solve this undesired lockout problem, an innovative technique (U.S. Patent 6,418,002: "Power Supply Supervisor with Line Voltage Detector") is built into the SG6105. The AC line voltage is sampled by pin 5 (UVAC) of the SG6105. During a line loss event, UVAC will be set before UVP will be enabled. If UVP detects a low voltage while UVAC is asserted, the SG6105 will enter hiccup mode instead of latch mode. The outputs will be turned off, and turned back on after a set time (typically three seconds). This anti-lockout function is particularly important during brownout situations.

Pin 4 (*OPP*)

The over power protection feature of the SG6105 is designed to protect the power supply from damage due to output power bursts and short circuits. Fig. 5 shows an applied PWM drive circuit with over power detection. Proportional driving operation enables the driving transformer to be used as a current transformer. This makes it possible for the current transformer to detect the primary current flow of the half-bridge power stage. With Q_1-ON/Q_2-OFF or Q_1-OFF/Q_2-ON, one of the half-bridge transistors will be turned on, and energy will be transferred from the primary side to the secondary side.

The reflected current from N_1 to N_2 is used to drive one of the power transistors. This can be calculated as:

$$I_{pri} \cdot \frac{N_2}{N_{1\ b}}$$

Let Z_b denote the equivalent impedance of the base circuit of the power transistor. The voltage across N_2 will be:

$$V_{N2} = I_{pri} \cdot \frac{N_2}{N_1} \cdot Z_b$$

First calculating the voltage across N_3, V_p can be expressed as:

$$V_{N3} = V_{N2} \cdot \frac{N_3}{N_2}$$

$$V_p = V_{N3} + 2V_{diode} = I_{pri} \cdot \frac{N_2}{N_1} \cdot Z_b \cdot \frac{N_3}{N_2} + 1.4V$$

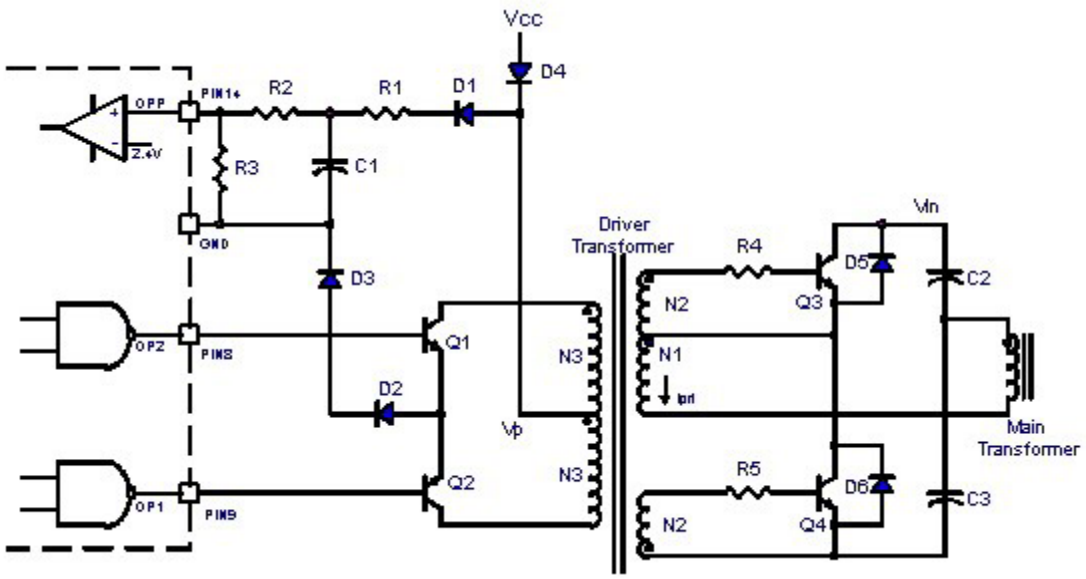


Figure 5. An Applied PWM Drive Circuit with OPP

The voltage V_p is fed into the OPP pin of the SG6105 through a voltage divider and a low pass filter. The normal operating level of V_p should be higher than the 12V output from the standby power supply, otherwise the OPP pin may be falsely triggered. There are two protection thresholds. When V_{OPP} exceeds 3.2V, the PWM cycle will be terminated immediately to provide short circuit protection.

The SG6105 attempts to establish a constant over power protection threshold for any level of AC input. At lower AC input voltages, the upper primary current limit should be larger to maintain a constant power limit. Since V_{OPP} is proportional to the primary current but not to the input power, additional compensation is necessary. In the SG6105, the threshold is determined by:

$$OPP\_Limit = (\frac{1}{3}V_{UVAC} + \frac{2}{3}V_{OPP}) \geq 2.4V$$

When the OPP pin exceeds 2.4V for longer than 7 milliseconds, the SG6105 will lock off the power supply. V_{UVAC} is the signal for AC input voltage detection. It will be described in the next section.

Pin 5 (*UVAC*)

Fig. 6 shows an AC detection circuit. During the turn-on interval of the half-bridge stage, the AC line voltage is coupled from the primary side to the secondary side through the main transformer. The voltage divider provides the necessary gain reduction, and a small capacitor is connected between UVAC and ground to filter out switching noise.

Once the voltage of UVAC drops below 0.7V for longer than some fixed interval, the power good signal will be pulled low to provide a power-down warning. Adjusting the turns-ratio of the main transformer or the ratio of the voltage divider will set the threshold for the power-down warning. The UVAC pin is also used to provide anti-lockout during line disturbances. See the section covering 'Pin 2/ Pin 3/ Pin 7' for a detailed description.

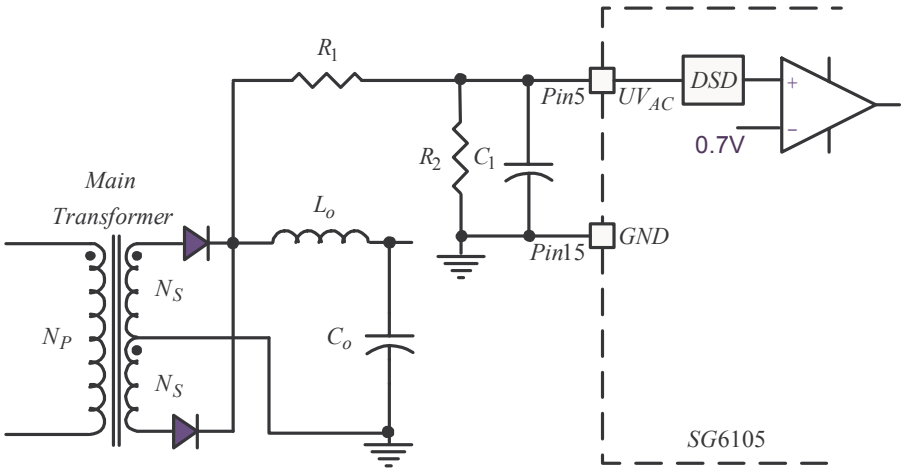


Figure 6. An AC Detection Circuit

Pin 6 (*NVP*)

The negative voltage protection (NVP) of the SG6105 provides under voltage protection for the negative voltage outputs (-5V/-12V). An under voltage condition indicates that the negative voltage output is undergoing either an overload or a short circuit. Fig. 7 shows an applied NVP circuit. When the voltage of the NVP pin exceeds 2.1V for longer than 7 milliseconds, the SG6105 will lock off the power supply.

A constant current source I_{NVP} and the resistor/diode network determine the protection threshold. The value of I_{NVP} is inversely proportional to the value of R_i. I_{NVP} is equal to 64μA if R_i is 75kΩ. In this applied circuit, the diode D_1 is reverse-biased. When the -5V output is within limits, and the -12V output is under voltage, the threshold is determined by:

$$2.1 = I_{NVP} \times (R_1 + R_2) + V_{-12V}$$

With the -12V output within limits and the -5V output under voltage, the diode D_1 will be forward-biased. The threshold is then determined by:

$$2.1 = I_{NVP} \times R_1 + (V_{-5V} - 0.7V)$$

With I_{NVP} equal to 64μA and the desired protection thresholds equal to –10V/–3.3V for the –12V/–5V outputs, the values of R_1/R_2 will be determined by the following equations:

$$2.1V = 64uA \times (R_1 + R_2) - 10V$$

$$2.1V = 64uA \times R_1 + (-3.3V - 0.7V)$$

Solving the above equations, we get R_1= 95.3kΩ and R_2= 93.7kΩ.

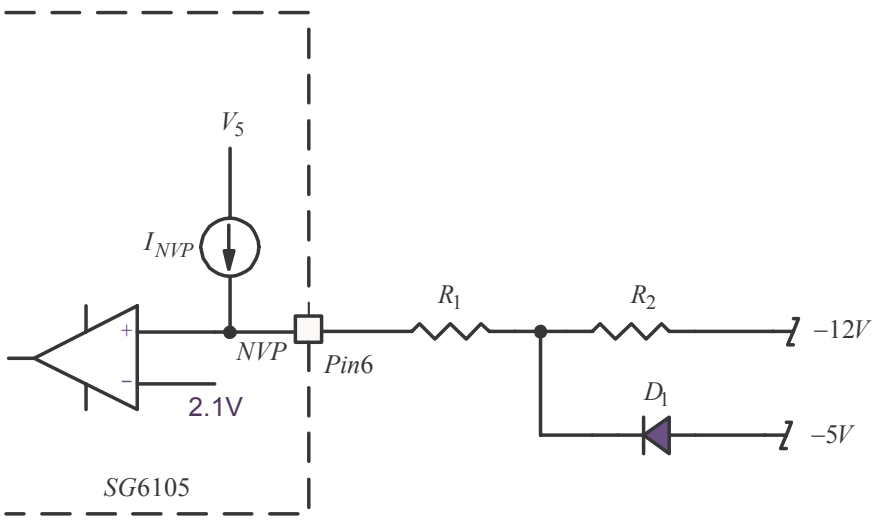


Figure 7. A Negative Voltage Protection Circuit

Pin 8/ Pin 9 (OP_1/OP_2)

Fig. 5 shows an applied circuit used to drive a PWM signal, and detect over power conditions. The drive transformer is also used as a current transformer, to detect the primary current flow of the half-bridge power stage. Fig. 8 shows the related timing diagram. V_{COMP} shows the output of the error amplifier compared with an internal sawtooth signal. This is used to determine the duty ratio of Q_1/Q_2.

With Q_1-ON/Q_2-OFF or Q_1-OFF/Q_2-ON, one of the half-bridge transistors is turned on and energy is transferred from the primary side to the secondary side. With Q_1 and Q_2 turned on simultaneously, the drive transformer is shorted through the N_3 winding. This turns the power transistors off. It is strongly recommended to minimize the leakage inductance of the driving transformer. This is necessary for the turn-off behavior of the power transistors to be fast and clean. This will enhance system efficiency and provide stronger protection.

D_2/D_3 is used to increase the base voltage level of Q_1/Q_2, so that Q_1/Q_2 can be easily turned off by the SG6105. The 12V Vcc signal generated by the standby power source is used to provide a start-up PWM pulse through D_4. To ensure safe operation during latch-off mode, OP_1 is internally pulled high to a 5V standby voltage through a 1.7 kΩ resistor. OP_2 is internally pulled high to a 12V level through a 4.7kΩ resistor.

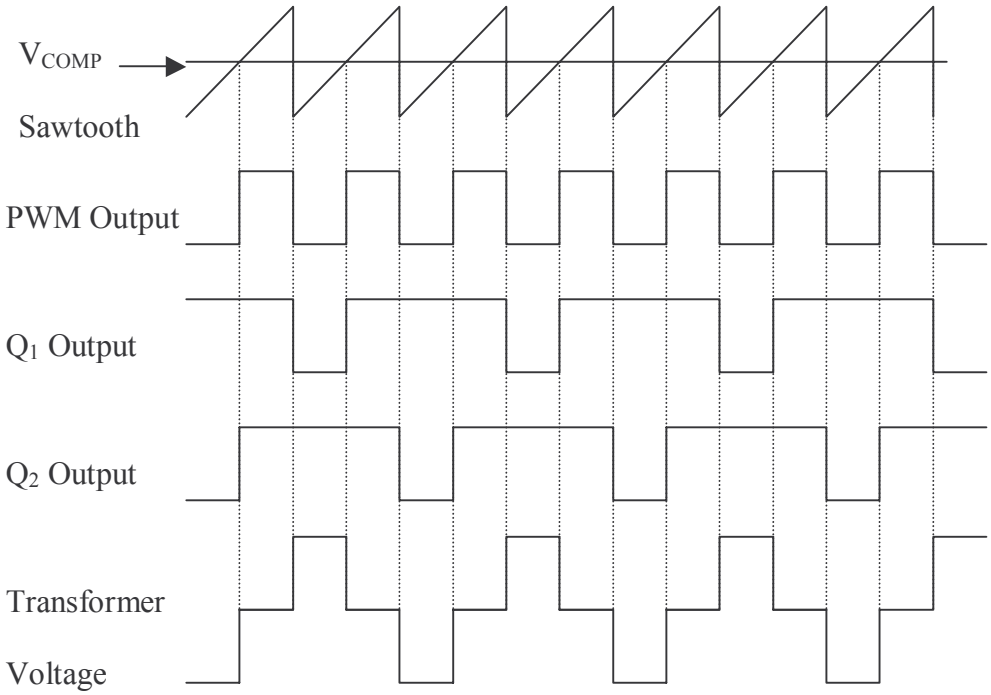


Figure 8. The SG6105 Timing Diagram

Pin 10 (*PG*)

The power good logic output is an active high signal. If the outputs are out of the desired range or the input AC voltage UVAC is too low, the PG signal will be pulled down. See Fig. 4 for the relative timing between PS_{ON} and PG. If PS_{ON} is pulled high to enable remote shutdown, PG will be pulled down immediately before the main outputs are turned off.

Pin 11/Pin 12/Pin 13/ Pin 14 ($FB_2 / V_{ref2} / FB_1 / V_{ref1}$)

The SG6105 has two built-in shunt regulators. The TL431 is an example of a typical shunt regulator. They are used for feedback control of the 3.3V magnetic amplifier and the 5V standby power supply. See Fig. 2 and Fig. 3 for the detailed application circuits.

Pin 15 (*GND*)

All voltages are measured with respect to the GND pin. A bypass capacitor connected between Vcc and the GND pin is recommended.

Pin 16/Pin 17 (*COMP*/*IN*)

Fig. **9** shows the suggested feedback compensation circuit for the main outputs. The 5V and the 12V outputs are used for feedback compensation. The positive input (pin 18) is used for the 2.5V reference voltage of the feedback circuit and the soft-start function. An internal 1.5MΩ resistor is connected between the inverting input and the output of the error amplifier. As shown in Fig. **8**, the output of the error amplifier is compared with an internal sawtooth signal to determine the PWM duty ratio.

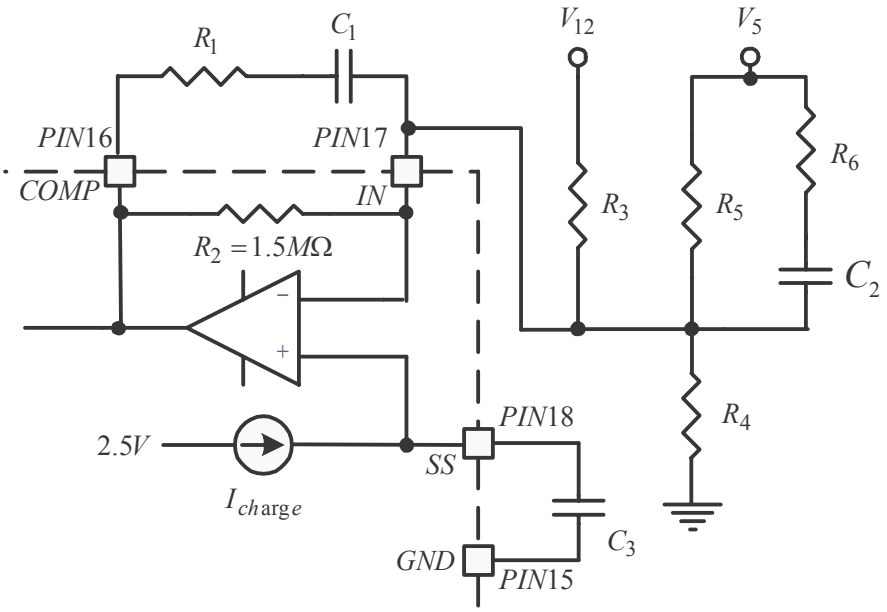


Figure 9. An Applied Feedback Compensation Circuit

Pin 18 Soft Start (*SS*)

One capacitor connected from the positive input of the error amplifier to the ground pin is used to program the soft start function. As shown in Fig. 9, a constant current source is used to charge the SS capacitor to 2.5V during start-up. The voltage of the SS pin is used as the reference for the error amplifier, so that the output voltage waveform will follow the waveform of SS exactly. A larger SS capacitor will increase the start-up time and reduce the stress on the switching devices. The SS capacitor will be discharged after the occurrence of a protection event or a remote shutdown. The resistor R_i can affect the constant current source. Please read the description of Pin 19(R_i) for further information.

Pin 19 (R_i)

The switching frequency of the SG6105 is determined by a single variable resistor. The resistor connected between the pin R_i and ground will generate a constant current source. This current charges an internal capacitor and hence determines the internal frequency. Increasing the resistance will decrease the current source and reduce the switching frequency. Unlike conventional R/C structures, the switching frequency of the SG6105 is nearly temperature independent, since the capacitor is built in. The oscillator frequency can be written as:

$$f_{OSC}(kHz) = \frac{4875}{R_i(k\Omega)}$$

Fig. 10 shows the characteristic curve of R_i versus switching frequency. A suggested R_i resistance reference setting is 75kΩ. This generates a 65kHz switching frequency. It is necessary to be aware that if R_i is modified to obtain a different switching frequency, the internal current sources of the SG6105 will change accordingly. This will affect the behavior of NVP and SS. For example, if R_i is changed from 75kΩ to 91kΩ, to obtain a lower switching frequency (65kHz to 54kHz), the current source of the NVP input will change from 64μA to 53μA, according to the following equation:

$$I_{NVP-NEW} = 64 \times (75k\Omega / 91k\Omega)$$

Meanwhile, the current source of the soft start pin will decrease in magnitude from 8μA to 6.6μA.

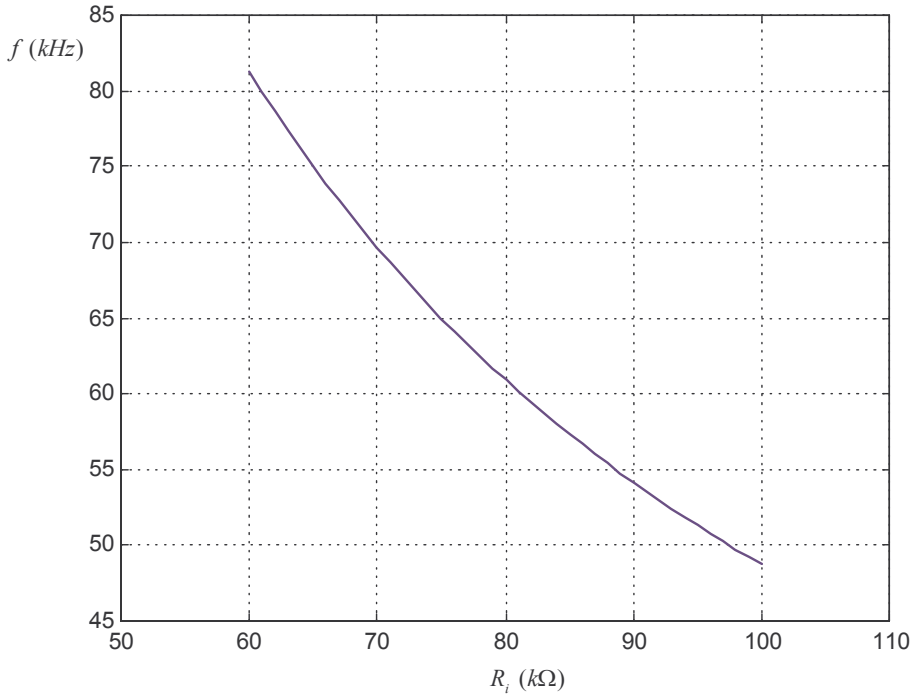


Figure 10. R_i Resistance vs. Oscillator Frequency

Pin 20 (V_{cc})

The SG6105 requires a working voltage between 4.5V and 5.5V. As shown in Fig. 3, another AC/DC converter using flyback topology is required. The flyback converter provides a standby 5V working voltage to the SG6105, and a 12V signal to drive the transformer gate during start-up. The SG6848, a low cost green-mode PWM controller, is suggested for the standby flyback converter. The built-in shunt regulator of the SG6105 can be used to regulate the 5V standby output.