AND8124/D

90 W, Universal Input, Single Stage, PFC Converter

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General Description

This application note describes the implementation of a 90 W, universal input Flyback Power−Factor−Correction (PFC) converter using On Semiconductor's NCP1651 controller.

The NCP1651 enables a low cost single−stage (with a low voltage isolated output) PFC converter as demonstrated in this application circuit, which is designed for 48 Vdc, at 1.9 A of output current. The NCP1651 is designed to operate in the fixed frequency, continuous mode (CCM), or discontinuous (DCM) mode of operation, in a flyback converter topology. The converter described in this application note has the following valuable features:

Features

- Wide Input voltage range (85 − 265 Vac)
- Galvanic isolation
- Primary side cycle−by−cycle and average current limit
- Secondary side power limiting
- High voltage start−up circuit

Detailed Circuit Description

Operational description and design equations are contained in the NCP1651 Data Sheet. This application note address specific design issues related to this converter design. Please refer to Figure 2 for component reference designators.

Voltage Regulation Loop

With a flyback topology, the output is isolated from the input by the power transformer. Output voltage regulation can be accomplished in two ways. The first, and the simplest method is by sensing the primary side voltage of the auxiliary winding. This eliminates the feedback isolation circuitry, at the expense of accuracy of voltage regulation and current sensing. The second method is to sense the secondary side voltage which is more complex, but provides better voltage regulation and transient response.

The NCP1651 demo board uses a quad operational amplifier on the secondary to perform multiple functions. One section of the amplifier is used as the error amplifier. A voltage divider comprised of R23, R24, R25 and R33 senses the output voltage and divides it down to 2.5 V. This signal is applied to the negative input of the error amplifier; the 2.5 V reference is applied to the non−inverting input of the error amplifier.

The output of the error amplifier provides a current sink that drives the LED of the optocoupler. The primary side optocoupler circuit sinks current from pin 8. This varies the voltage into the Voltage−to−Current converter that feeds the reference multiplier.

The loop operation is as follows: If the output voltage is less than its nominal value, the voltage at the output of the voltage divider (inverting input to the error amplifier) will be less than the reference signal at the non−inverting error amplifier input. This will cause the output of the error amplifier to increase. The increase in the output of the error amplifier will cause the optocoupler LED to conduct less current, which in turn will reduce the current in the optocoupler photo−transistor. This will increase the voltage at pin 8 of the chip, and in turn increase the output of the reference multiplier, causing an increase in the NCP1651 duty cycle.

The current shaping network is comprised of the ac error amplifier, buffer and current sense amplifier. This network will force the average input current to maintain a scaled replica of the current reference on pin 10. The increase of the reference voltage will cause the current shaping network to draw more input current, which translates into an increase in output current as it passes through the transformer. The increase in current will increase the output power and therefore, the output voltage. To calculate the loop stability, it is recommended that the On Semiconductor spread sheet be used. This is an easy and coinvent way to check the gain and phase of the control loop.

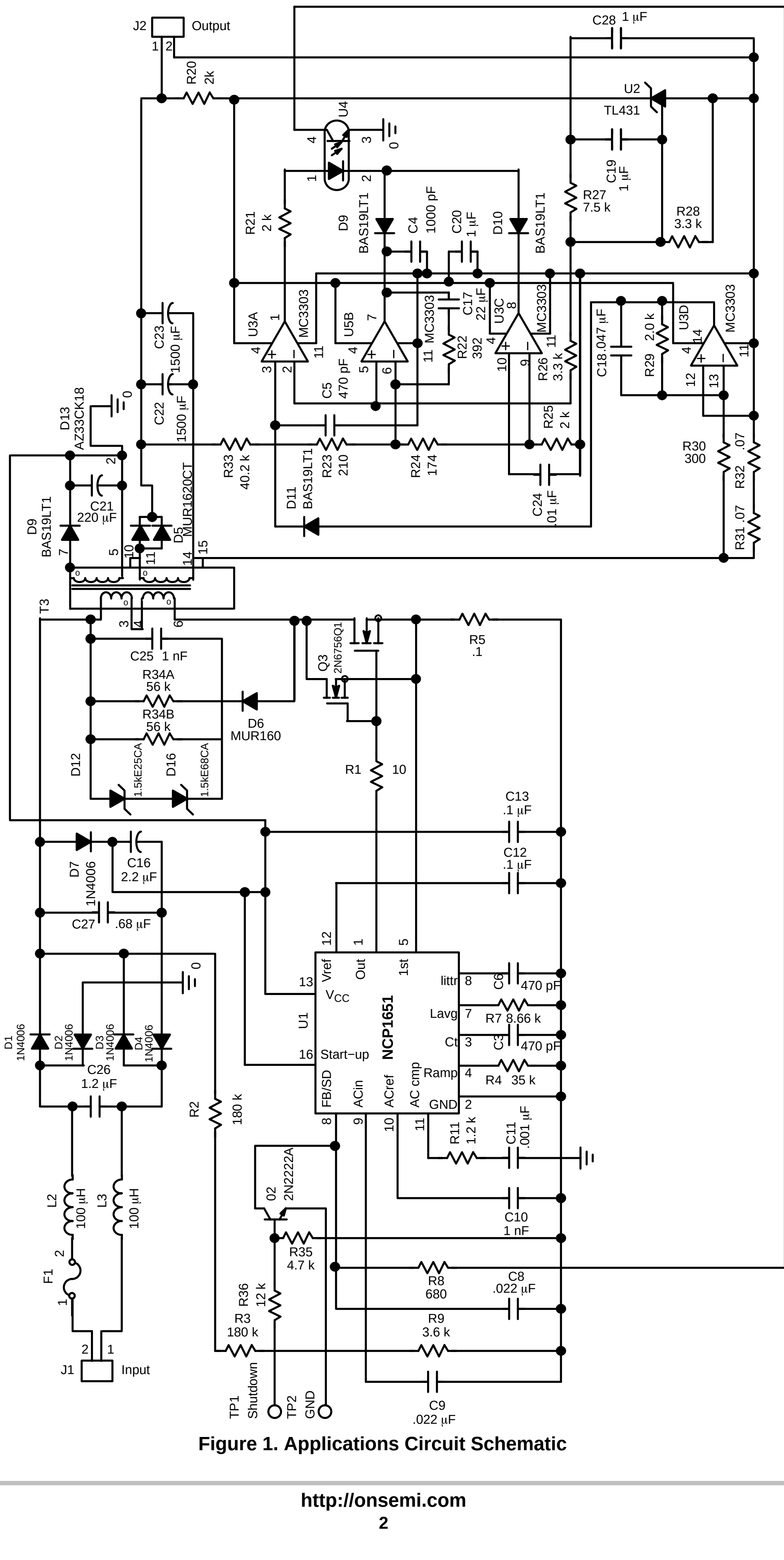

Figure 1. Applications Circuit Schematic

Overshoot/Undershoot Circuit

Two sections of the quad amplifier are used as comparators. One of these monitors the output for overvoltage condition and the other for undervoltage condition. The voltage divider requires four resistors (R33, R23, R24, and R25) in order to make the various ratios available for the two comparators as well as the error amplifier.

The undervoltage comparator provides the drive for the opto−coupler. Its output is normally in the saturated high state, which allows the flow of current into the opto−coupler to be determined by the error amplifier or overvoltage comparator. If an undervoltage condition occurs, the output of the UV comparator goes low, which reduces the drive current to the opto−coupler LED. This causes the NCP1651 to go into a high duty cycle state, and will increase the flow of current into the output until the output voltage is above the UV limit.

The over−voltage comparator's output is OR'ed with the output of the error amplifier. During an overvoltage event (e.g. a transient load dump), the output of this comparator will go to ground, and cause the maximum current to flow in the opto−coupler LED. This will pull pin 8 low and reduce the duty cycle to zero until the output voltage is below the OV limit. It should be noted that the purpose of the 680 Ω resistor (R8) in series with the opto−coupler photo transistor, is there to keep the voltage at pin 8 above the 0.5 V threshold during such events. This keeps the control chip operational and will allow immediate operation when the output voltage is again in its normal operating range. Without this resistor, the voltage on pin 8 would drop below 0.5 V, causing the NCP1651 to enter a low power shutdown mode of operation.

Current/Power Limit Circuit

The fourth section of the amplifier is biased as a differential amplifier. This section senses the DC output current, and provides a signal that is diode OR'ed into the feedback divider.

In the demo board the overload current limit was set to 125% of full load, or 2.375 A. Two resistors are used in series (to limit their maximum power dissipation) to sense the output current (R31 and R32). R29 and R30 set−the current sense amplifier gain.

Where the gain of the amplifier is:

$$G = (R29/R30) + 1 = 3000/300 + 1 = 11 \qquad \text{(eq. 1)}$$

The voltage to the input of the differential amplifier is:

$$2.375\ \text{A} \cdot 0.14\ \Omega = 0.33\ \text{V} \qquad \text{(eq. 2)}$$

The output voltage from the differential amplifier is:

$$V_O = 0.33 \cdot 11 = 3.63\ \text{V} \qquad \text{(eq. 3)}$$

When the output load current increases, the output of the current sense amplifier will also increase. When the amplifiers output voltage, minus a diode drop (D11), increases above the 2.5 V, it pulls up the feedback signal at the inverting input of the error amplifier (when the loop is in regulation the inverting input voltage is typically 2.5 V). This causes the error amplifier signal to go low, sinking more current through the LED in the opto−coupler. This in turn drives more current in opto−coupler transistor collector, pulling it low reducing the duty cycle, folding back the output voltage.

Output Voltage Ripple

The output voltage ripple on the secondary of the transformer has two components, the traditional high frequency ripple associated with a flyback converter, and the low frequency ripple associated with the line frequency (50 Hz or 60 Hz). In this application our goal was to have the output ripple 5% of the nominal output voltage, or 2.4 V pk−pk.

The High Frequency Ripple can be Calculated by:

$$\Delta V = \sqrt{\Delta V_{cap}{}^2 + \Delta V_{esr}{}^2} \qquad \text{(eq. 4)}$$

$$\Delta V_{cap} = i_{rms}\, dt / C_O \qquad \text{(eq. 5)}$$

The RMS current at the peak of the sinewave (phase angle 90°).

$$i_{rms} = \sqrt{(t_{off} / T) \cdot (((I_{pk}{}^2 + (I_{pk}\, I_{ped}) + I_{ped}{}^2) / 3\,)) - (t_{off} / 4T) \cdot (I_{pk} + I_{ped})^2)} \qquad \text{(eq. 6)}$$

$$i_{rms} = \sqrt{((3.85\ \mu / 10\ \mu)) \cdot (((13.38^2 + 13.38 \cdot 10.27 + 10.27^2) / 3) - 3.85\ \mu / 10\ \mu \cdot 4) \cdot (13.38 + 10.27)^2)} = 5.78 \qquad \text{(eq. 7)}$$

To meet the capacitors ripple current requirements and lower the equivalent esr, two 1500 μF capacitors were used in parallel.

$$\Delta V_{cap} = (5.78 \cdot 3.85\ \mu / 3000\ \mu) = 0.00742 \qquad \text{(eq. 8)}$$

Where:

- n =Transformer Turns Ratio
- Ipk =Peak Current Secondary (13.38)
- Iped =Pedestal Current Secondary (10.27)
- C_O =Output Capacitance (1500 μ each)
- esr =Output Capacitor Equivalent Series Resistance (0.03 Ω Each)
- T =Switching Interval

$$\Delta V_{esr} = I_{pksec} \cdot esr \qquad \text{(eq. 9)}$$

$$\Delta V_{esr} = 13.38\ \text{Apk} \cdot 0.015 = 0.20\ \text{V} \qquad \text{(eq. 10)}$$

$$\Delta V = \sqrt{0.00742^2 + 0.2^2 = 0.200} \qquad \text{(eq. 11)}$$

The Low Frequency Portion of the Ripple:

$$\Delta V = I_{pk}\, \Delta t / C_O \qquad \text{(eq. 12)}$$

$$I_{AVG} = P_O / V_O \qquad \text{(eq. 13)}$$

$$I_{pk} = I_{AVG} / 0.637 \qquad \text{(eq. 14)}$$

$$I_{pk} = P_O / V_O\, 0.637 = 90 / (48)(0.637) = 2.95 \qquad \text{(eq. 15)}$$

If we divided the output ripple into 10° increments over one cycle (180°) the sinusoidal ripple voltage with respect to phase angle is:

$$\Delta V = ((P_O / 0.637\,V_O) \cdot \sin(\theta) - 0.637)) / C_O \cdot 18 \cdot f_{line} \quad \text{(eq. 16)}$$

In Figure 2, the low frequency output voltage ripple are plotted with respect to phase angle.

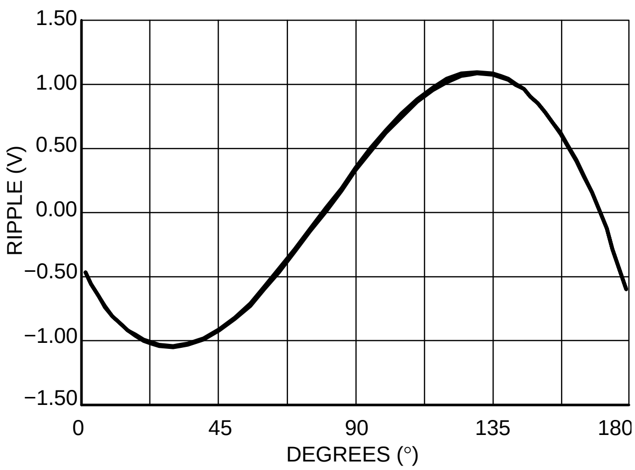

Figure 2. Calculated Output Ripple

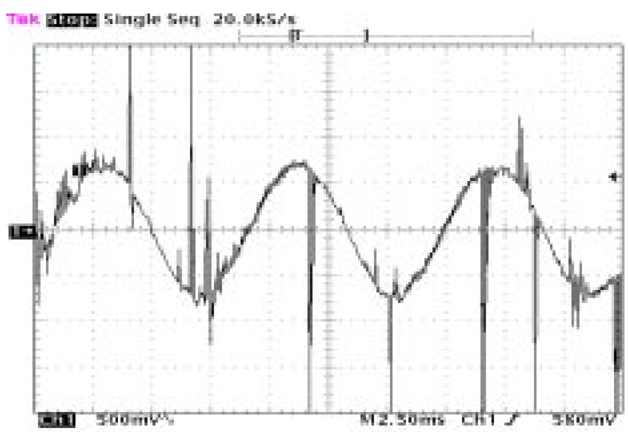

Figure 3. Measured Output Voltage Ripple

It can be seen from the calculations, and the scope waveform that as long as a capacitor with a low esr is used, that the output voltage ripple is dominated by the low frequency (120 Hz) ripple.

Hold−Up time

If the user would like to select C_O for Hold−Up time versus, voltage ripple:

$$P_{out} = \frac{1}{2}\ C_O\ V^2\ f \quad \text{(eq. 17)}$$

Rearranging the equation:

$$C_O = 2\ P_{out}\ th / V_{max}{}^2 - V_{min}{}^2 \quad \text{(eq. 18)}$$

th = One Cycle of the Line 16.67ms (60Hz)
V_{max} = 48 V
V_{min} = 36 V
P_{out} = 90 W

$$C_O = (2 \cdot 90 \cdot 16.67\text{ ms}) / (48^2 - 36^2) = 3000\ \mu F \quad \text{(eq. 19)}$$

It is a coincidence that the output capacitor calculated for voltage ripple and hold−up time are the same value.

MOSFET Turn−off Snubber

The MOSFET in our design has a VDS rating of 800 V, the peak voltage across the device at turn−off (including the leakage inductance spike) is:

$$V_{pk}Total = V_{inmax}\ 1.414 + ((V_O + V_f)n) + V_{spike} \quad \text{(eq. 20)}$$

Where:

V_{inmax} = 265 Vrms
V_O = the Output Voltage (48 V)
n = the Transformer Turns Ratio (4)
V_{spike} = Voltage Spike Due to Transformer Leakage Inductance

To provide a safe operating voltage for the MOSFET we have selected V_{spike} to be 130 V_{peak}, so when the MOSFET turns off, the maximum Drain to Source voltage is:

$$265 \cdot 1.414 + 48(4) + 130 = 697\ V \quad \text{(eq. 21)}$$

To minimize the effect of the leakage inductance spike, the coupling between the primary and secondary of the transformer needs to be as tight as possible. This can be accomplished, if your transformer requires a primary with multiple layers, by interleaving the primary and secondary windings. In our 48 Vdc application the transformer primary has 74 turns, and the secondary has 19 turns. The manufacture of the transformer, TDK, wound one layer of the primary with 45 turns, then the 19 turn secondary, and the remaining 29 turns of the primary. The results were a leakage inductance of approximately 9 μH. If we compare this to a transformer where the entire 74 turns were wound, in two layers, then the 19 turn secondary, the leakage inductance increased to 37 μH.

The energy stored in the transformer leakage:

$$E = \frac{1}{2} \cdot l_e \cdot I_{pk}{}^2 \quad \text{(eq. 22)}$$

Where:

l_e = Leakage Inductance (9 μH Measured)
I_{pk} = Peak Primary Current

A Second Relationship is:

$$E = \frac{1}{2} \cdot C \cdot V^2 \quad \text{(eq. 23)}$$

Where:
C= Snubber Capacitor
V= the Voltage Across the MOSFET

Combining Equations:

$$C = I_{pk}^2 \cdot I_e / ((V_O + V_f)n + V_{pk} + V_{spike})^2 - ((V_O + V_f)n + V_{pk})^2 \quad \text{(eq. 24)}$$

$$C_{snubber} = 3.8^2 \cdot 9\,\mu H / ((192 + 375 + 130)^2 - (192 + 375)^2 = 790\text{ pF} \quad \text{(eq. 25)}$$

During the MOSFET turn−off, the capacitor C25 is charge through the Diode D6. Prior to the next ton switching cycle the capacitor C25 must be fully discharged, so $R_{snubber}$ is selected to be:

$$R_{snubber} = ((V_O + V_f)n + V_{inmax} \cdot 1.414 + V_{spike})\; 0.63\,\tau / (V_{spike} * C_{snubber}) \quad \text{(eq. 26)}$$

$$((192 + 375 + 130)0.63(6.5\,\mu) / (130 * 790\text{ pF}) = 28\text{ k} \quad \text{(eq. 27)}$$

The power in the snubber is:

$$P = \frac{1}{2} C V^2 \quad \text{(eq. 28)}$$
$$= (0.5)790\text{ pF}(130^2)\ 100\text{ kHz} = 0.68\text{ W}$$

After installing the snubber in the NCP1651 Demo Board, and measuring the voltage spike, the snubber components where adjusted for maximum performance, C25 was increased to 1000 pF, and R34 was changed to 20 kΩ. The difference between the measured and calculated value can be attributed to the PWB board layout, and other parasitic components.

Evaluation Board Test Results

The results from the NCP1651 Demo Board show that using a flyback topology for a PFC converter can provide a low input Total Harmonic Distortion (THD), a high input power factor, and excellent steady state output voltage regulation.

The NCP1651 achieved a THD at 115 Vac input at full load of 3.12% with a PF of 0.998. The input THD to 6.8% THD at 230 Vac in, with a PF of 0.971.

The steady state output voltage regulation from 85 Vac to 230 Vac, and no load to full load is less than 0.02%, with an output voltage ripple meeting our design goal of 2.4 Vpk−pk, measured 2.0 V pk−pk.

Transient Response

Figures 4 through 7 show the output transient response for the 90 W converter. The test conditions for each Figure are listed below:

Table 1. Test Conditions

	V_{in}	ΔI_O
Figure 4	115 Vac	0.19 – 1.92 A
Figure 5	115 Vac	1.92 – 0.19 A
Figure 6	230 Vac	0.19 – 1.92 A
Figure 7	230 Vac	1.92 – 0.19 A

In Figure 4, the output voltage drops to 40 Vdc, and recovers in less than 160 ms. In Figure 6 the input voltage was increased to 230 Vac, and the load was switched from 10% to 100% load. The output voltage now drops only to 44 Vdc, and recovers in approximately 50 ms. The significant improvement in transient response performance is attributed to an increase in the DC gain and loop bandwidth at high line. As the input ac line voltage increases the control loop DC gain (Refer to www.onsemi.com for a copy of the excel design spreadsheet for details) increases from 42 dB at 115 Vac to 62 dB at 230 Vac and the control loop bandwidth increases from 2 Hz to 8 Hz. The result is that at high line, there is an improvement in transient response, but because there is less attenuation of the output 120 Hz ripple, it results in an increase in the input Total Harmonic Distortion (THD). The system designers will need to trade off their overall system performance THD, Power Factor, and transient response to optimize the control loop to meet their requirements.

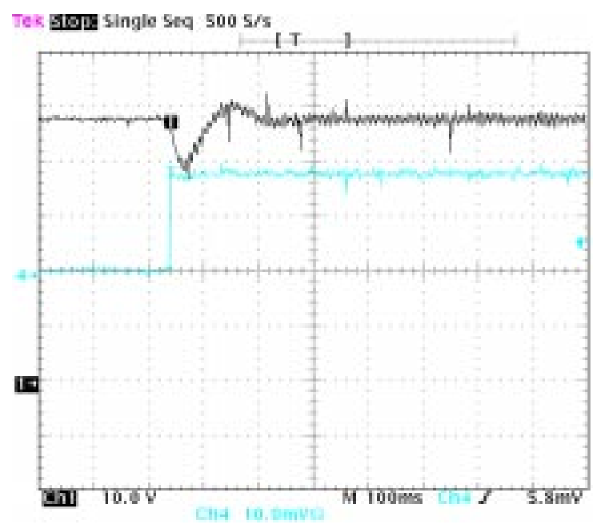

Figure 4. Figure 5

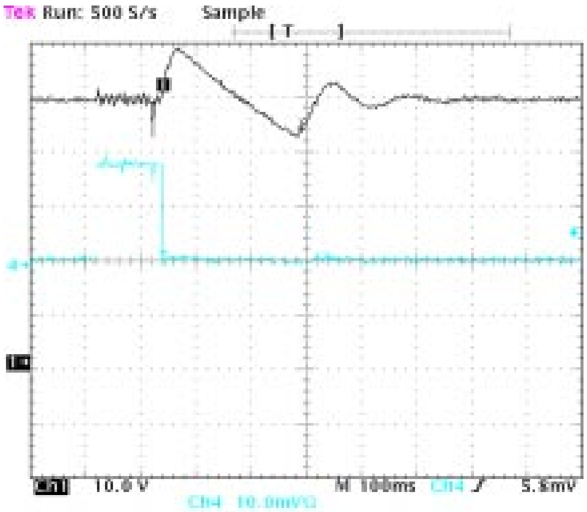

Figure 5. Figure 6

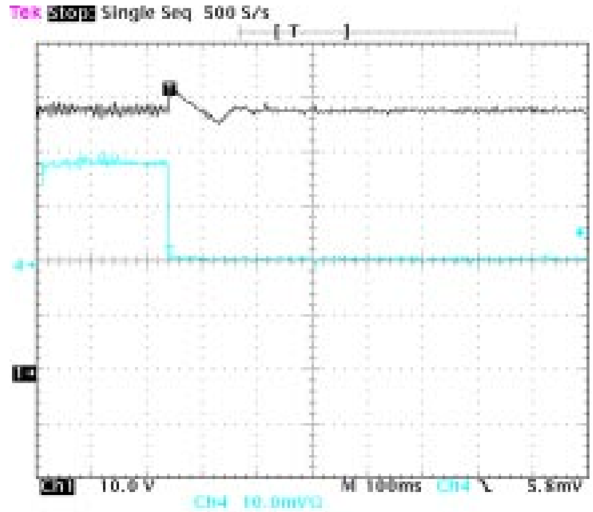

Figure 7. Figure 8

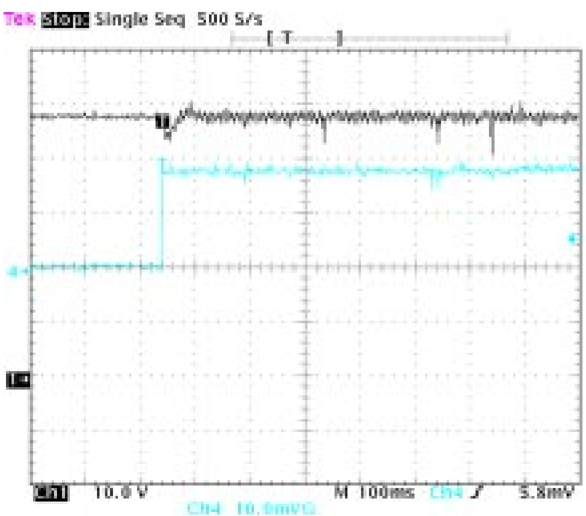

Figure 6. Figure 7

Power Dissipation Estimates

The NCP1651 Demo Board power dissipation (measured) at 115 Vrms, full load, is (106.27 – 47.95 •1.92) = 14.21 W. Following table provides the calculated and estimated power loss spread among different power train components.

Components		Pd average
D1−D4	Input Rectifier	1.65 W
Q1	MOSFET	4.1 W
D5	Output rectifier	1.7 W
T3	Flyback transformer	3.5 W (estimate)
R34	Snubber resistor	0.84 W
D12	Transient suppressor	2.0 W
	miscellaneous	0.41 W
Total		14.20 W

Demo Board Operating Instructions

Connect an Ac source, 85 − 265 Vac, 47 − 64 Hz to the input terminals J1. Connect a load to the output terminals J2, the PWB is market +, for the positive output, − for the return. Turn on the ac source, and the NCP1651 will automatically start, providing 48 Vdc to the load.

Shutdown Circuit

The shutdown circuit will inhibit the operation of the power converter and put the NCP1651 into a low power shutdown mode. To activate this circuit, apply 5 V to the red test point, with the black jack being “ground”. Be aware that the black jack is actually hot as it is connected to the output of the input bridge rectifiers. An isolated 5 V supply should be used.

If this circuit is not being used, it can be left open as there is enough resistance built in to the circuit to keep the transistor (Q2) in it's off state.

Table 2. Performance Data Regulation

Line/Load	No Load	45 W	90 W
85 Vrms	47.94	47.95	47.95
115 Vrm	47.94	47.95	47.95
230 Vrms	47.94	47.95	47.95
265 Vrms	47.94	47.94	47.95

Table 3. Harmonics & Distortion

	115 Vac 90 W		230 Vac 90 W	
	V harmon	A harm. %	V harm	A harm%
2nd	0.143	0.156	0.08	0.2
3rd	0.203	1.94	0.25	4.74
5th	0.13	0.6	0.12	2.88
7th	0.08	0.28	0.07	0.22
9th	0.04	0.19	0.09	0.76
11th	0.08	0.29	0.08	0.27
13th	0.16	0.32	0.06	0.33
15th	0.28	0.41	0.14	0.68
17th	0.4	0.41	0.28	0.95
19th	0.05	0.29	0.12	0.3
PF		0.998		0.971
THD(A)		3.12		6.8
Ifund		0.918		0.468

Table 4. Efficiency

	85 Vrms	115 Vrms	230 Vrms	265 Vrms
Pin @ No Load	1.5	1.52	1.51	1.59
Pin	109.42	106.27	105.35	105.25
Vo	47.95	47.95	47.95	47.95
Io	1.92	1.92	1.92	1.92
Efficiency	0.841	0.866	0.874	0.875

Table 5. Vendor Contact List

Vendor	U. S. Phone / Internet
ON Semiconductor	1−800−282−9855 www.onsemi.com/
TDK	1−847−803−6100 www.component.tdk.com/
Vishay	www.vishay.com/
Bussman (Cooper Ind.)	1−888−414−2645 www.cooperet.com/
Coiltronics (Cooper Ind.)	1−888−414−2645 www.cooperet.com/
Fairchild	www.fairchildsemi.com/
Panasonic	www.eddieray.com/panasonic/
Weidmuller	www.weidmuller.com/
Keystone	1−800−221−5510 www.keyelco.com/
HH Smith	1−888−847−6484 www.hhsmith.com/
Aavid Thermalloy	www.aavid.com/

Table 6. NCP1651 Application Circuit Parts List (Specifications:, 90 W, 85 vac to 265 vac Input Range, 48 V Output)

Ref Des	Description	Part Number	Manufacturer
C1	Cap, Ceramic, Chip, 1000 pF, 50 V	VJ0603Y102KXAAT	VISHAY
C3	Cap, Ceramic, Chip, 470 pF, 50 V	VJ0603Y471JXAAT	VISHAY
C5	Cap, Ceramic, Chip, 470 pF, 50 V	VJ0603Y471JXAAT	VISHAY
C6	Cap, Ceramic, Chip, 470 pF, 50 V	VJ0603Y471JXAAT	VISHAY
C8	Cap, Ceramic, Chip, .022 μF, 50 V	VJ0603Y223KXXAT	VISHAY
C9	Cap, Ceramic, Chip, 0.022uF, 50 V	VJ0603Y223KXXAT	VISHAY
C10, C11	Cap, Ceramic, chip, 0.001uF, 50 V	VJ0603Y102KXAAT	VISHAY
C12, C13	Cap, Ceramic, Chip, 0.1uF, 50 V	VJ0606Y104KXXAT	VISHAY
C16	2.2uF, alum elect, 450 V (0.394dia x 0.492H) (.394dia x .492H)	ECA−2WHG2R2 EKA00DC122P00	Panasonic (Digi – P5873) Vishay Sprague (20)
C17	Cap, Ceramic, Chip, 22uF, 10v	C3225X5R0J226MT	TDK
C18	Cap, Ceramic, Chip, .047uF, 50 V	VJ0603Y473KXXAT	VISHAY
C19	Cap, Ceramic, Chip, .01uF, 50 V	VJ0603Y103KXAAT	VJ0603Y103KXAAT
C20	Cap, Ceramic, Chip, 1uF, 25v	C3216X7R1E105KT	TDK
C21	220uF, alum elect, 25 V	ECA1EM331	Panasonic
C22, 23	1800uF, alum elect, 63 V (2.2A rms min) 1500uF, alum elect, 63 V	EEU−FC1J182 EKB00JL415J00	Panasonic (Digi – P11283) Vishay Sprague (20)
C24	Cap, Ceramic, Chip, .01uF, 50 V	VJ0603Y103KXAAT	VISHAY
C25	Cap,Ceramic, .001uF, 1KV	ECK−03A102KBP	Panasonic
C26	1.2uF, 275 vac, X cap	F1778−512K2KCT0	VISHAY
C27	Cap, polypropylene, .68uF, 400 VDC	MKP1841−468−405	Vishey − Sprague
C28	Cap, Ceramic, Chip, 1uF, 25v	VJ1206V105ZXXAT	VISHAY
D1 – D4	Diode, rectifier, 800 V, 1 A	1N4006	ON Semiconductor
D5	Diode, ultrafast, 200 V, 16 A	MUR1620CT	ON Semiconductor
D6	Diode, ultrafast, 600 V, 1 A	MUR160	ON Semiconductor
D7	Diode, rectifier, 800 V, 1 A	1N4006	ON Semiconductor
D8 – D11	Diode, switching, 120 v, 200 mA, SOT−23	BAS19LT1	ON Semiconductor
D12	TVS, 214 V, 5 W	1.5KE250A	ON Semiconductor
D13	Zener Diode, 18 V, 0.3 W	AZ23CK18	VISHAY
D16	Zener Diode 68 V	1.5kE68CA	ON Semiconductor
F1	Fuse, 2 A, 250 Vac	1025TD2A	Bussman
L2	2.5 A sat, 100 uH inductor, diff mode	TSL1315−101K2R5	TDK
L3	2.5 A sat, 100 uH inductor, diff mode	TSL1315−101K2R5	TDK
Q1	FET, 11 a, 800 v, .45 Ω, N−channel	SPA11N80C3	Infineon
Q2	Bipolar, npn, 30 V, SOT−23	MMBT2222ALT1	ON Semiconductor
R1	Resistor, SMT1206, 10	CRCW1206100JRE4	Vishey
R2	Resistor, axial lead, 180k, ¼ W	CMF−55−180K00FKRE	Vishey
R3	Resistor, axial lead, 180k, ¼ W	CMF−55−180K00FKRE	Vishey
R4	Resistor, SMT1206, 35k	CRCW120635KOJNTA	Vishey
R5	Resistor, SMT, 0.12 Ω, 1 W	WSL2512 .12Ω 1%	Vishey Dale
R7	Resistor, SMT1206, 8.66 k	CRCW12068661F	Vishey
R8	Resistor, SMT1206, 680	CRCW12066800F	Vishey

Table 6. NCP1651 Application Circuit Parts List (Specifications:, 90 W, 85 vac to 265 vac Input Range, 48 V Output)

Ref Des	Description	Part Number	Manufacturer
R9	Resistor, axial lead, 3.6k, ¼ W	CMF−55−3K600FKBF	Vishey
R11	Resistor, SMT1206, 1.2k	CRC12061K20JNTA	Vishey
R20	Resistor, SMT1206, 2.0k	CRC12062K00JNTA	Vishey
R21	Resistor, SMT1206, 2.0k	CRC12062K00JNTA	Vishey
R22	Resistor, SMT1206, 5.1k	CRC12052K10JNTA	Vishey
R23	Resistor, SMT1206, 210, 1%	CRCW12062100F	Vishey
R24	Resistor, SMT1206, 174, 1%	CRCW12061740F	Vishey
R25	Resistor, SMT1206, 2.05k, 1%	CRCW12062051F	Vishey
R26	Resistor, SMT1206, 3.3k	CRC12063K30JNTA	Vishey
R27	Resistor, SMT1206, 7.5k	CRC12067K50JNTA	Vishey
R28	Resistor, SMT1206, 3.3k	CRC12063K30JNTA	Vishey
R29	Resistor, SMT1206, 3.01k, 1%	CRCW12063011F	Vishey
R30	Resistor, SMT1206, 301, 1%	CRCW12063010F	Vishey
R31	1w, .07 Ω resistor	WSL251R0700FTB	Vishey
R32	1w, .07 Ω resistor	WSL251R0700FTB	Vishey
R33	Resistor, SMT1206, 40.2k, 1%	CRCW120640022F	Vishey
R34	Resistor, axial lead, 20k, 2W		
R35	Resistor, SMT1206, 4.7k	CRCW12064K70NTA	Vishey
R36	Resistor, SMT1206, 12k	CRCW120612K0JNTA	Vishey
R37	Resistor, SMT1206, 100k	CRCR1206100K0JNTA	Vishey
T1	Transformer, Flyback	SRW35EC−UxxH013	TDK
U1	PFC Controller	NCP1651	ON Semiconductor
U2	2.5 V programmable ref, SOIC	TL431ACD	ON Semiconductor
U3	Quad Op A	MC3303D	ON Semiconductor
U4	Optocoupler, 1:1 CTR, 4 pin	SFH615AA−X007	Vishay

Hardware

H1	Printed Circuit Board		
H2	Connector	171602	Weidmuller (Digi 281−1435−ND)
H3	Connector	171602	Weidmuller (Digi 281−1435−ND)
H4	Standoff, 4−40, alum, hex, .500 inches	8403	HH Smith (Newark 67F4111)
H5	Standoff, 4−40, alum, hex, .500 inches	8403	HH Smith (Newark 67F4111)
H6	Standoff, 4−40, alum, hex, .500 inches	8403	HH Smith (Newark 67F4111)
H7	Standoff, 4−40, alum, hex, .500 inches	8403	HH Smith (Newark 67F4111)
H8	Heatsink, TO−220	590302B03600	Aavid Thermalloy
H9	Heatsink, TO−220	590302B03600	Aavid Thermalloy
H10	Test point, red	5005	Keystone (Digi 5005K−ND)
H11	Test point, black	5006	Keystone (Digi 5006K−ND)

NOTES:

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