Subsequently the PFC gate drive is initiated, eliminating the necessary dead time needed for the DCM mode. This forces the output to run away until the $V_{CC}$ OVP shuts down the PFC. This situation is corrected by adding an offset voltage to the current sense signal, which forces the duty cycle to zero at light loads. This offset prevents the PFC from operating in the DCM and forces pulse-skipping from CCM to no-duty, avoiding DMC operation. External filtering to the current sense signal helps to smooth out the sense signal, expanding the operating range slightly into the DCM range, but this should be done carefully, as this filtering also reduces the bandwidth of the signal feeding the pulse-by-pulse current limit signal. Figure 9 displays a typical circuit for adding offset to $I_{SENSE}$ at light loads.

## PFC Start-Up and Soft Start

During steady state operation VEAO draws 35µA. At start-up the internal current mirror which sinks this current is defeated until $V_{CC}$ reaches 12V. This forces the PFC error voltage to $V_{CC}$ at the time that the IC is enabled. With leading edge modulation $V_{CC}$ on the VEAO pin forces zero duty on the PFC output. When selecting external compensation components and $V_{CC}$ supply circuits VEAO must not be prevented from reaching 6V prior to $V_{CC}$ reaching 12V in the turn-on sequence. This will guarantee that the PFC stage will enter soft-start. Once $V_{CC}$ reaches 12V the 35µA VEAO current sink is enabled. VEAO compensation components are then discharged by way of the 35µA current sink until the steady state operating point is reached. See Figure 8.

## PFC Soft Recovery Following $V_{CC}$ OVP

The FAN4803 assumes that $V_{CC}$ is generated from a source that is proportional to the PFC output voltage. Once that source reaches 16.2V the internal current sink tied to the VEAO pin is disabled just as in the soft start turn-on sequence. Once disabled, the VEAO pin charges HIGH by way of the external components until the PFC duty cycle goes to zero, disabling the PFC. The $V_{CC}$ OVP resets once the $V_{CC}$ discharges below 16.2V, enabling the VEAO current sink and discharging the VEAO compensation components until the steady state operating point is reached. It should be noted that, as shown in Figure 8, once the VEAO pin exceeds 6.5V, the internal ramp is defeated. Because of this, an external Zener can be installed to reduce the maximum voltage to which the VEAO pin may rise in a shutdown condition. Clamping the VEAO pin externally to 7.4V will reduce the time required for the VEAO pin to recover to its steady state value.

## UVLO

Once $V_{CC}$ reaches 12V both the PFC and PWM are enabled. The UVLO threshold is 9.1V providing 2.9V of hysteresis.

## Generating $V_{CC}$

An internal clamp limits overvoltage to $V_{CC}$. This clamp circuit ensures that the $V_{CC}$ OVP circuitry of the FAN4803 will function properly over tolerance and temperature while protecting the part from voltage transients. This circuit allows the FAN4803 to deliver 15V nominal gate drive at PWM OUT and PFC OUT, sufficient to drive low-cost IGBTs.

It is important to limit the current through the Zener to avoid overheating or destroying it. This can be done with a single resistor in series with the $V_{CC}$ pin, returned to a bias supply of typically 14V to 18V. The resistor value must be chosen to meet the operating current requirement of the FAN4803 itself (4.0mA max) plus the current required by the two gate driver outputs.

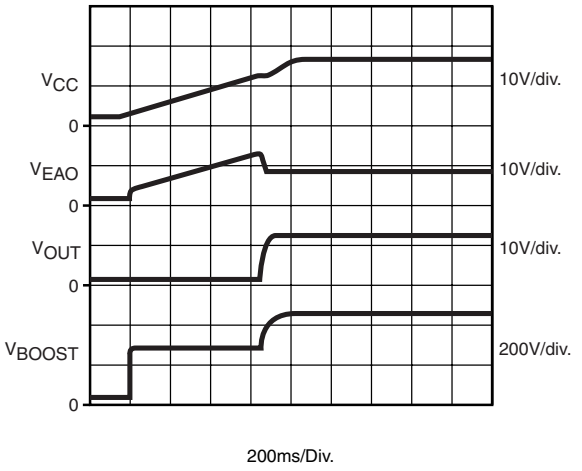


**Figure 8. PFC Soft Start**

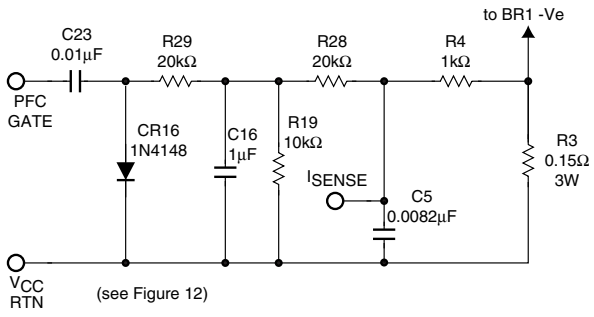


**Figure 9. $I_{SENSE}$ Offset for Light Load Conditions**