SIEMENS

Requirements for Power MOSFETs Connected in Parallel

1 Introduction and Objectives

For the field of applications for power FETs to be expanded, e.g. in arc welding equipment, as a substitute switching relay, in uninterruptible power supplies and in motor controllers, it must be possible to connect several FETs in parallel. To ensure reliable and trouble-free parallel operation, the parameters which affect the switching behavior of the power FET must be analyzed. In this context, the main interest is in the effects of the parasitic network and device parameters on the switching process. The operating behavior of power FETs based on the same types of transistor connected in parallel is determined by the structure of the network, the driver circuit and the tolerances of the device, including its connection.

This paper indicates what requirements must be met by the driver circuit, the circuit arrangement and the power FET including the device connection, in order to ensure problem-free parallel operation. In analyzing the operating behavior, a distinction is made between dynamic and steady state operation. Because of the short switching times, more demanding requirements must be met in experimental recording of the transient processes $i(t)$ and $v(t)$.

2 Static Behavior

The basic circuit used in investigating the switching characteristics of parallel-connected power FETs is shown in **Figure 1**. In this, six FETs arranged in a ring, with common supply of their gates and a common ground connection point, are operated in parallel. The load inductance L_B is so large that the load current i_B remains virtually constant during the switching and commutating phases. For low voltage applications ($V_D \leq 100$ V) a Schottky diode is used as the freewheeling diode, and for high voltage applications ($V_D \leq 800$ V) a FRED (fast recovery epitaxial diode) FET diode is used. The branch currents are measured using respectively 100 mΩ and 10 mΩ cage shunts with high load limit integrals ($\int t^2 dt$) and high-frequency transmission characteristics (pulse frequency $f_T \approx 150$ MHz) in the drain circuit.

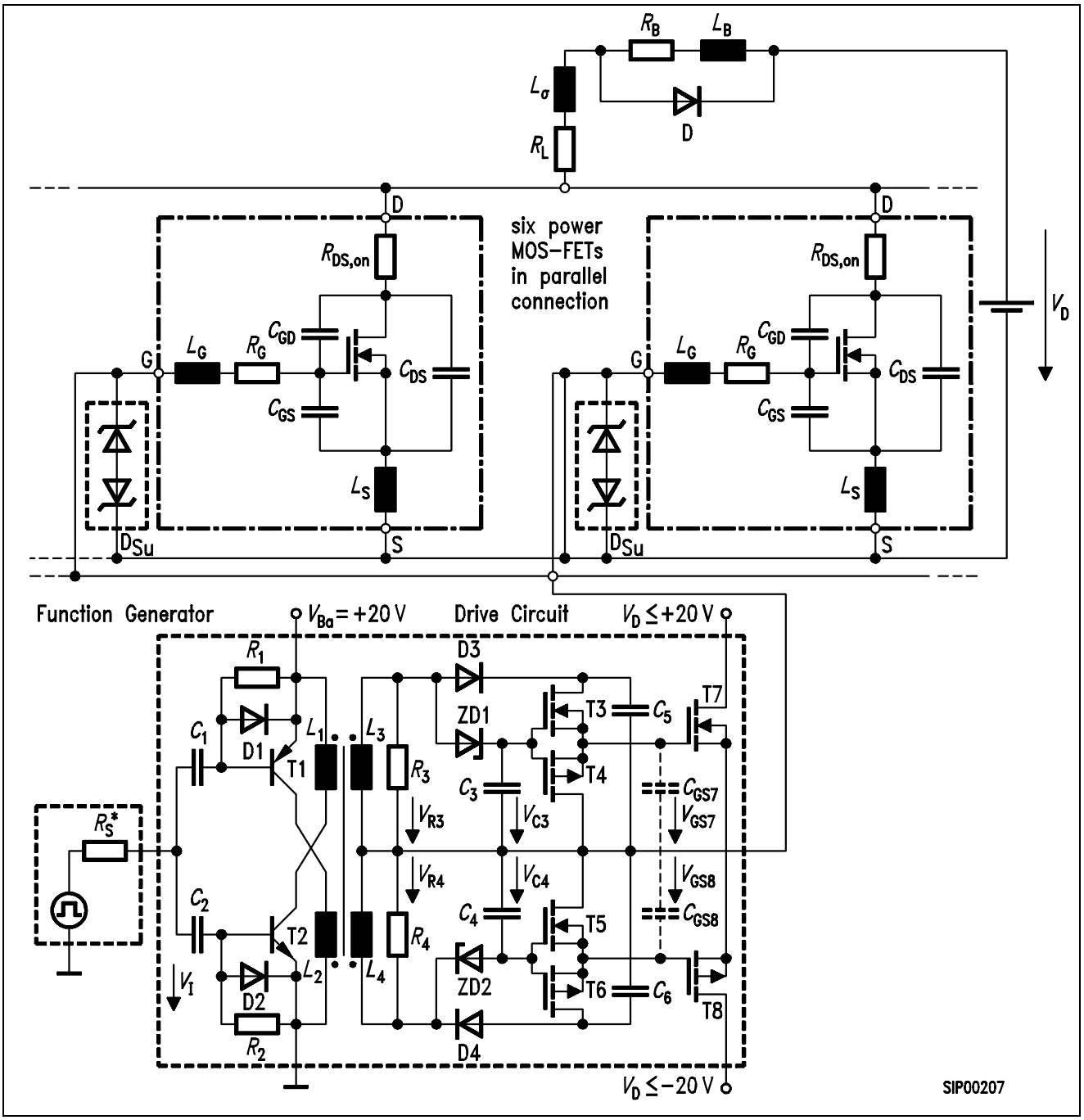

Figure 1
A Network with Parallel-connected FETs, Including the Main Parasitic Components

The current split in the steady “on state” is determined by the “on” resistance and the transconductance g_{fs}. The “on” resistance for a power FET is made up of a number of sub-resistances in series, with the resistance of the epitaxial layer dominating for transistors with a breakdown voltage V_{Br} > 150 V.

This resistance increases according to

$R_{epi} \sim (U_{Br})^{\beta}$, β = 2.5 … 2.7, and has a positive temperature coefficient:

$$R_{DS} = R_{DSon,\ 25\ °C}\left(\frac{1+\alpha}{100}\right)^{Tj-25}$$, with α = 6 … 9.

This means that a thermal “runaway” of individual FETs connected in parallel cannot occur. Instead the steady state current split adjusts itself as determined by the “on” resistances $R_{DSon} = f(V_{DS}, V_{GS}, I_D, \vartheta)$ of the individual transistors. Under constant drive conditions and if the cooling of all the parallel connected FETs is the same, the static current split is symmetric. **Figure 3a** shows the static current split when four high-voltage FETs (V_{DS} = 1000 V) are connected in parallel. Apart from the effect of epitaxial resistance differences on the static current split, the value of the transconductance is an important parameter. To clarify the effect of this in extreme cases, the transconductances for three power FETs which have very different current carrying capacities are indicated on the graph of $v_{GS} = f(I_D)$ in **Figure 2**. From this it is possible to determine directly the branch currents in the parallel-connected FETs. **Figure 3b** shows the measured values for the current split between the FET types shown alongside in **Figure 2**.

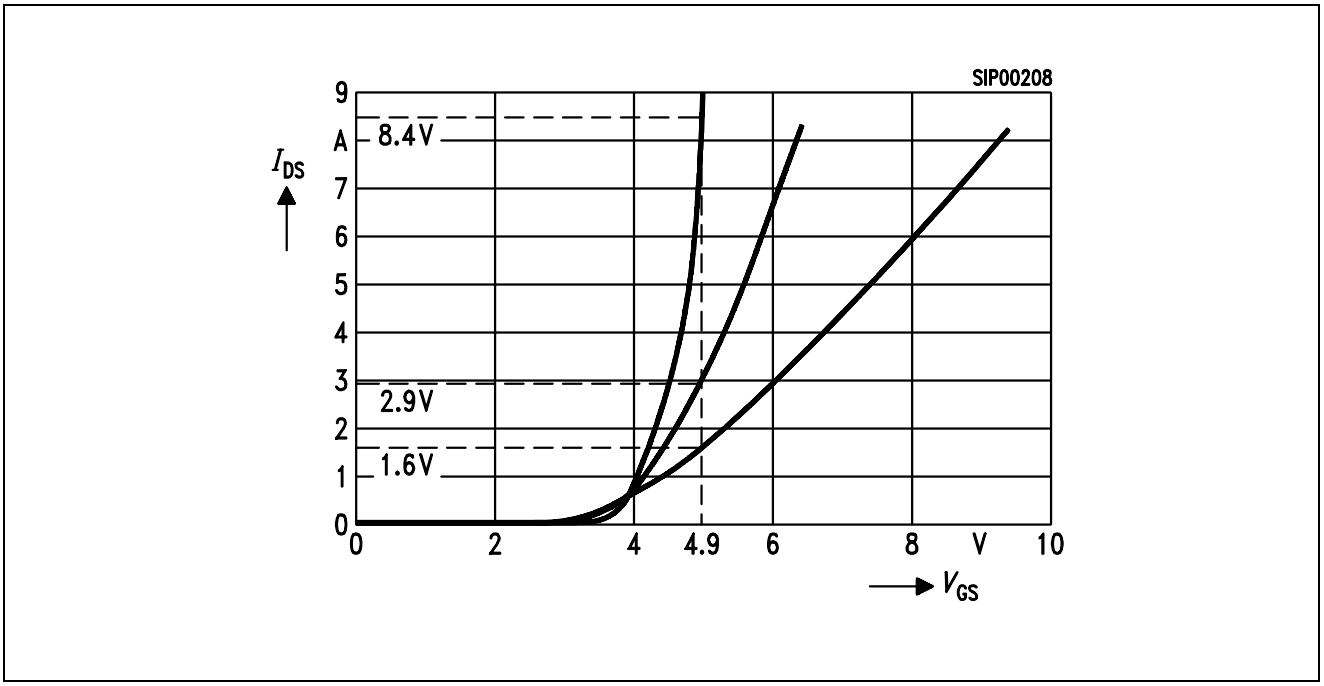

Figure 2
Transconductance g_{fs} (characteristic curve $I_{DS} = f(v_{GS})$) for different FET Types (Measured Curves)

While the measured values in **Figure 3b** agree very well with the current values taken from **Figure 2**, there are differences in the values for the dynamic current split (**Figure 4a** and **Figure 4b**). The dynamic current split is affected by a range of additional electrical variables.

As **Figure 2** shows, the effect of g_{fs} on the static current split is considerable. For this reason it is advisable that FETs connected in parallel should all be of the same type. The close tolerance limits on g_{fs} make it unnecessary to select them according to their transconductances.

3 Transient Behavior

Whereas the current split for power FETs is completely uncritical in steady-state operation, the switching behavior is considerably affected by a range of network and device parameters. In particular, these are:

- tolerances for the device parameters,
  - threshold voltage V_{th},
  - transconductance g_{fs}
  - input capacitances C_{GD} and C_{GS};
- asymmetries in the driver circuits,
  - charging current for the FET input capacitances,
  - driver signal;
- differences in the network parameters,
  - differing values for the resistances R_S and for wiring-dependent stray inductances L_G in the driver circuit,
  - differences in the stray inductances L_σ and L_S due to asymmetric layout of the power FETs.

For an analysis of the switching behavior it is important to know how heavily each of the individual parameters affects the switching process. For this reason, the effect of the electrical parameters mentioned above on the switching behavior for parallel connections will now be indicated.

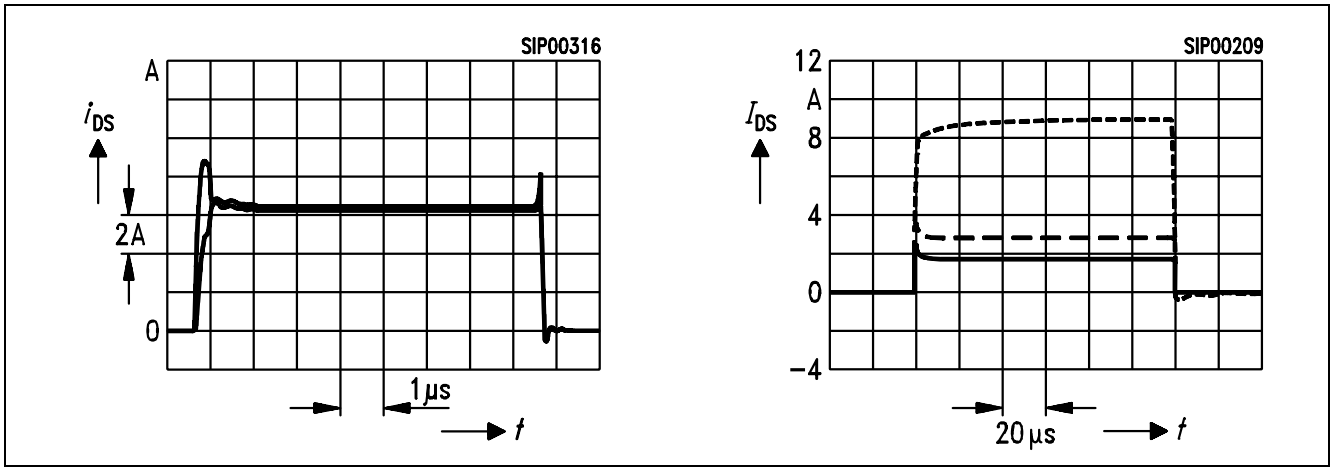

Figure 3
Drain Current Waveforms (Oscillogram) for
a) Differing "on" Resistances (High-voltage FET Types with Different Manufacturing Dates)
b) Different Transconductances, g_{fs}

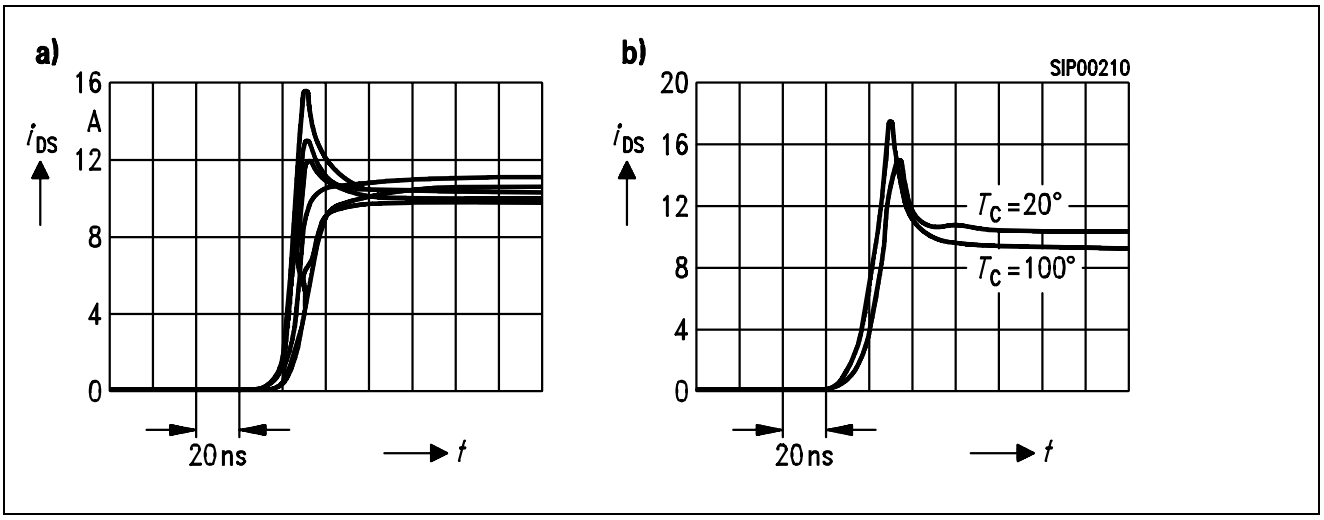

Figure 4
Drain Current Waveforms (Oscillogram) during Switch-on for Different FET Threshold Voltages
a) Six FETs Connected in Parallel
b) Two FETs in Parallel, showing the Effect of the Package Temperature T_c on the Threshold Voltage

3.1 Threshold Voltage

For power FETs, the threshold voltage V_{th} lies between 2.5 V and 4 V. This means that the maximum tolerance is 1.5 V. As a result of these differences, the FET with the lowest threshold voltage will be carrying the highest current during the switching processes. **Figure 4a** shows a switch-on process using six parallel-connected FETs which have slightly

different threshold voltages. An extreme case with two parallel-connected FETs is shown in **Figure 4b**. Account must also be taken of the fact that the threshold voltage V_{th} is strongly temperature dependent, and falls as the temperature rises. **Figure 4b** shows the effect of temperature on the threshold voltage (20 °C and 100 °C). An uneven temperature distribution across parallel-connected FETs will result in the current split during the switch-on process being less favorable.

3.2 Transconductance

Variations in the transconductance g_{fs} imply an unequal split of the dynamic and static currents. To show the extreme cases, **Figure 3** is for a combination of different types of FET which have the same current carrying capacity but very different transconductances. The dynamic current split for switch-on is shown in **Figure 5a**, and for switch-off in **Figure 5b**. As a result of the greater input capacitance of the FET with the higher transconductance, the threshold voltage is not reached until a later point in time during switch-on, so that current transfer is delayed; on the other hand, during switch-off this FET remains conductive for longer, and has to take over the complete current load during this time (assuming identical conditions in the driver circuit!). The static current split is – as **Figure 2** shows – easy to construct if the exact graph of transconductance is known for each of the FETs (the effect of temperature and the tolerances must be taken into account in doing this). It should be noted in addition that it is the FET with the highest transconductance which characterizes the switching process.

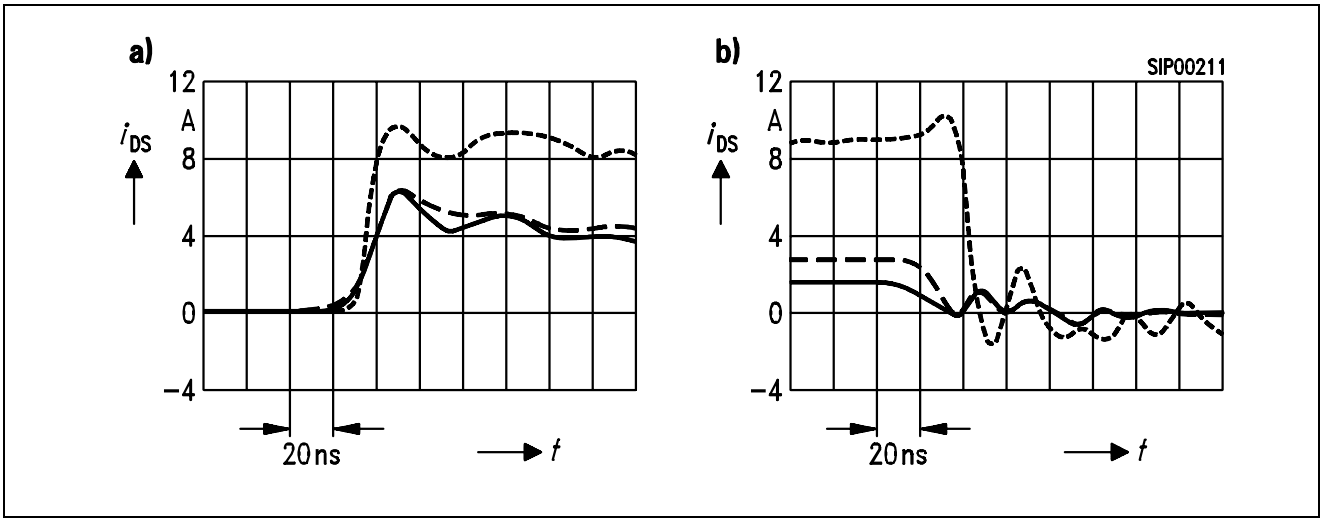

Figure 5
Drain Current Waveforms (Oscillogram) for Different FET Conductances
a) Switch-on Process
b) Switch-off Process

3.3 Input Capacitances

If the driver circuit is subject to fixed conditions (R_{st}, i_{st} = const.) then differences between the input capacitances lead to an unequal split of the load current during the switching process. Extreme situations arise when FETs with different current carrying capacities are compared.

From the gate charging curve it is possible to read off the total charge which must be fed to each of the FETs as a result of the differing input capacitances. In the case of a “hard switch” with a low-impedance output stage in the driver circuit, differences in the input capacitances have – as shown in **Figure 6** – no serious effect on the current split. A very unequal split of the current during the switching process results from differences in the input capacitances if the output stage of the driver circuit has a high impedance. **Figure 7** shows the dynamic current split during switch-on and switch-off processes for three FETs connected in parallel when they are of the same type but have input capacitances of different values. The output resistance of the driver circuit used for **Figure 7** is 110 Ω.

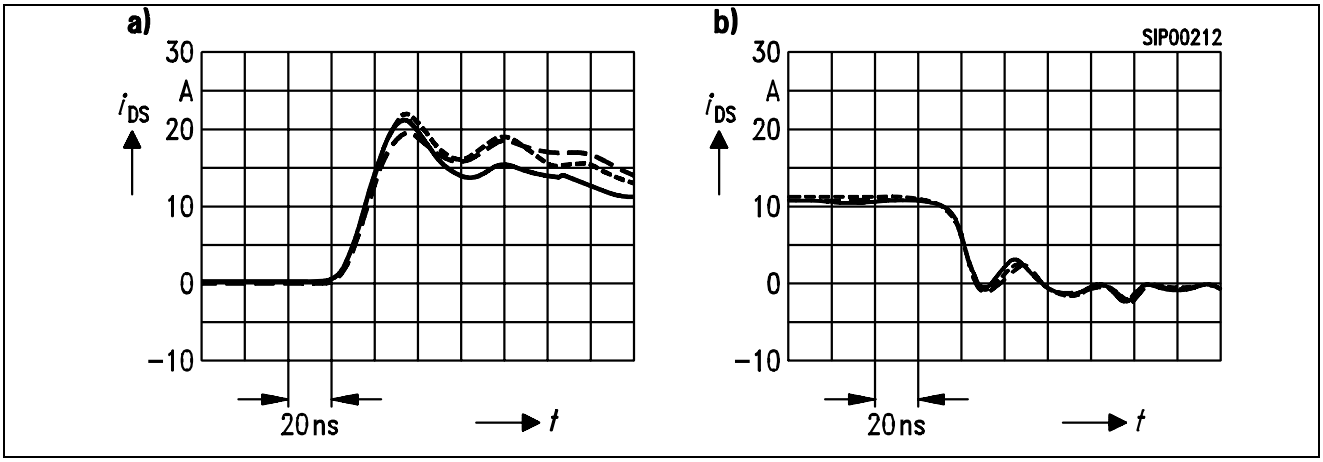

Figure 6
Drain Current Waveforms for three FETs of the same Type Connected in Parallel during "Hard Driving" (Oscillogram)
a) Switch-on Process
b) Switch-off Process

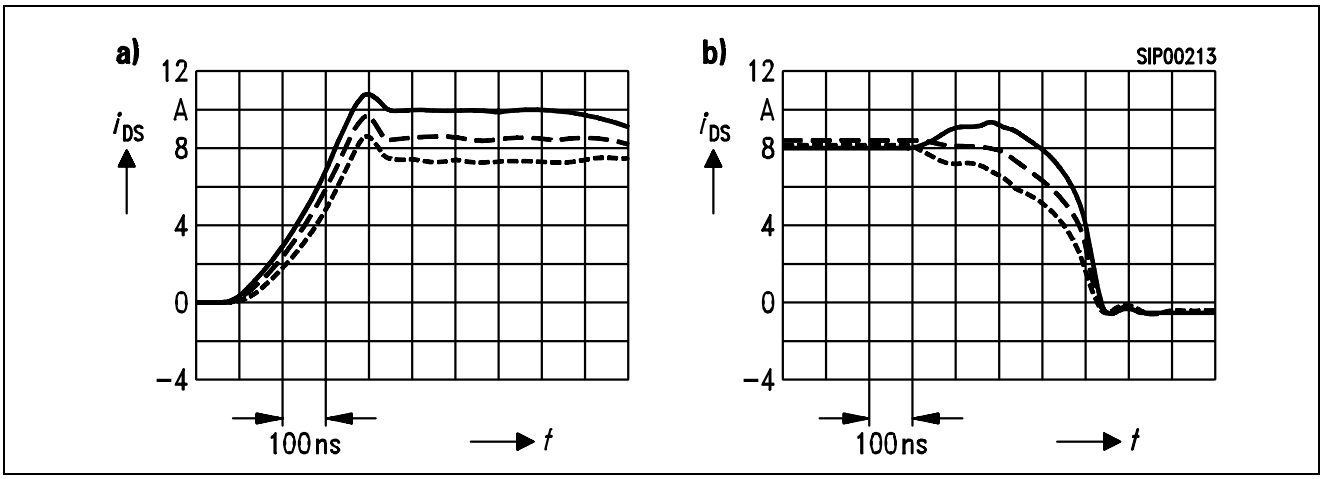

Figure 7
Oscillogram of the Drain Current Waveform for three Parallel-connected FETs of the Same Type with Differing Input Capacitances
a) Switch-on Process
b) Switch-off Process with Negative Gate-source Voltage

3.4 Control Circuit Output Resistance

The output resistance R_{st} of the driver circuit is responsible, together with the stray inductance L_σ, for the switching speed, but in addition for reliable and problem-free process during switch-off. The voltage change dv_{DS}/dt during switch-off is transmitted to the input via the C_{GD} capacitance so that – if the driver circuit output resistance is not sufficiently small – the gate-source voltage can reach values which switch the FET on again in an uncontrolled way, or can even reach levels which damage the FET input. **Figure 8** shows the gate-source voltage waveform when conditions in the driver circuit are constant but there are differences in the voltage amplitudes due to different stray inductances L_σ in the output circuit.

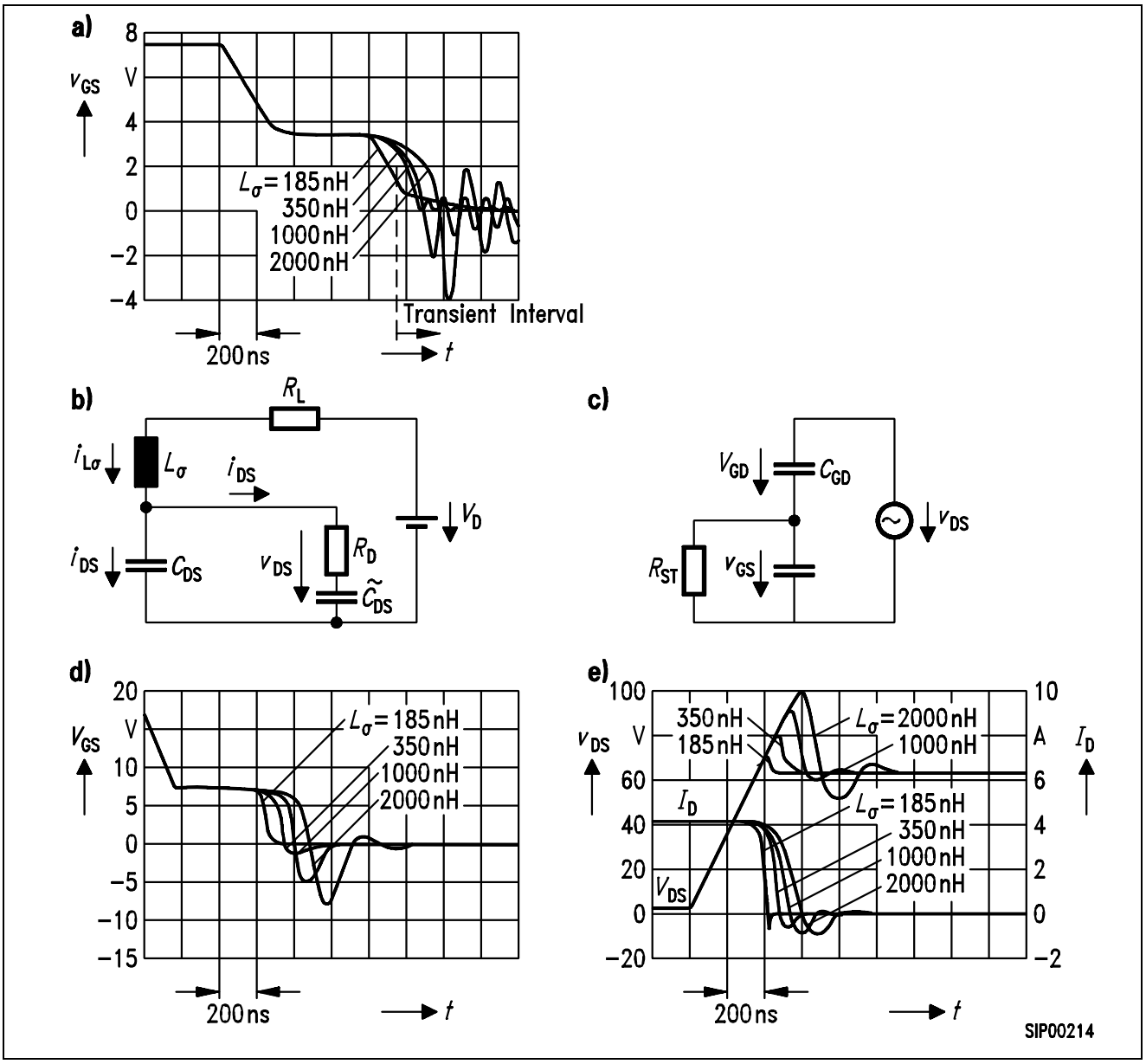

Figure 8
Transient Behavior

a) **Gate-source Voltage Waveform (Oscillogram) during Switch-off for Various Stray Inductances L_σ (FET Type: IRF130; R_{st} = 50 Ω)**

b) **Network for the Output Circuit (Subsystem 1) which Applies for the Transient Response Noted (Oscillator)**

c) **Network for the Input Circuit (Subsystem 2, Feedback to the Input Circuit)**

d) **Calculated Waveform of $v_{GS}(t)$ during Switch-off for Various Values of the Stray Inductance L_σ, and with V_D, I_D, R_{st} = const. (FET Type: IRF130, R_{st} = 50 Ω)**

e) **Calculated Waveform s of $v_{DS}(t)$ and $i_D(t)$ during Switch-off for Various Values of the Stray Inductance L_σ, and with V_D, I_D, R_{st} = const. (FET Type: IRF130, R_{st} = 50 Ω)**

This transient behavior (**Figure 8a**) can be calculated by approximating as follows for a FET with an external RC circuit. The equivalent circuit diagram for the output circuit over this switching period is shown in **Figure 8b**, and for the input circuit in **Figure 8c** (R_{ges} is the total resistance of the driver circuit).

From subsystem 1, $v_{DS}(t)$ and i_{L_σ} are calculated, together with the branch currents $\tilde{i}_{DS}$ and i_{DS}; and from subsystem 2 the feedback to the input, $v_{GS}(t)$.

For subsystem 1:

$$V_D = R_1 \times i_{L_\sigma} + L_\sigma \times \mathrm{d}\, i_{L_\sigma} / \mathrm{d}t + (i/C_{DS}) \int i_{DS}\, \mathrm{d}t; \qquad \textbf{equation 1}$$

$$i_{L_\sigma} = i_{DS} + \tilde{i}_{DS}; \qquad \textbf{equation 2}$$

$$v_{DS} = R_{DS} \times \tilde{i}_{DS} + (1/\tilde{C}_{DS}) \int \tilde{i}_{DS}\, \mathrm{d}t = (1/C_{DS}) \int i_{DS}\, \mathrm{d}t. \qquad \textbf{equation 3}$$

From this can be derived the differential equation (DE) for $\tilde{i}_{DS}(t)$:

$$L_\sigma \times C_{DS}^2 \times R_{DS} \times \mathrm{d}^3 \tilde{i}_{DS}/\mathrm{d}t^3 + \left[R_L \times R_{DS} \times C_{DS}^2 + L_\sigma \times C_{DS}(1 + C_{DS} / \tilde{C}_{DS}) \right] \mathrm{d}^2 \tilde{i}_{DS}/\mathrm{d}t^2$$
$$+ \left[R_{DS} \times C_{DS} + R_L \times C_{DS}(1 + C_{DS} / \tilde{C}_{DS}) \right] \mathrm{d}\, \tilde{i}_{DS}/\mathrm{d}t + (C_{DS} / \tilde{C}_{DS})\, \tilde{i}_{DS} = 0 \qquad \textbf{equation 4}$$

Using the solution for the current $\tilde{i}_{DS}(t)$, equation (3) can be used to determine the drain-source voltage waveform, $v_{DS}(t)$.

For subsystem 2:

$$\left[1/(R_{st} \times C_{GD})\right] v_{GS} + \left[(C_{GD} + C_{GS}) / C_{GD}\right] \mathrm{d}v_{GS} / \mathrm{d}t = \mathrm{d}v_{DS} / \mathrm{d}t; \qquad \textbf{equation 5}$$

From the time-varying disturbance term $v_{DS}(t)$, the waveform of $v_{GS}(t)$ can be obtained:

$$v_{GS}(t) = \left\{ \int_0^t \left[C_{GD} / (C_{GS} + C_{GD}) \right] (\mathrm{d}v_{DS}(s) / \mathrm{d}t) \exp(\eta\, s) \mathrm{d}s + V_{th} \right\} \exp(\eta\, t) \qquad \textbf{equation 6}$$

where

$\eta = 1/[R_{st}(C_{GS} + C_{GD})]$.

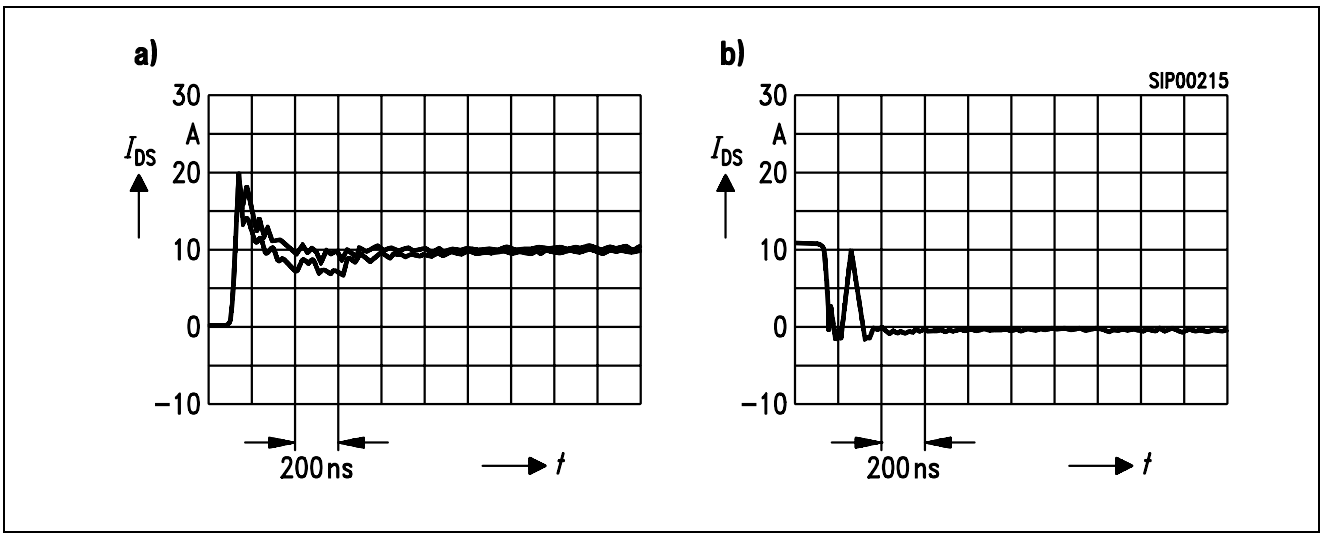

Figure 9
Oscillogram of the Drain Current Waveform for three FETs of the Same Type During Switch-on/-off Using a Unipolar Driver Impulse (V_{GS} = + 15 V)
a) Switch-on Process
b) Switch-off Process with a Brief Uncontrolled Switch-on Again

Equation (6) shows that the voltage fed back to the input increases as the resistance R_{st} increases. If the input circuit is open ($R_{st} \rightarrow \infty$), then the voltage is split as determined by the capacitances. For the steady-state situation, the ratio of this split is typically 1/5 . . . 1/6. In the transient state, the ratio can be less favorable, because $C_{GD} = f(v_{GD})$.

The transient behavior waveforms calculated according to equation (6) are shown in **Figure 8d** for various values of the stray inductance, L_σ.

Figure 9 shows the case when the voltage fed back causes an uncontrolled switch-on of the power FET. To prevent this, and to reduce the switch-off time, it is recommended that the FET is driven using bipolar impulses.

3.5 Parasitic Network Parameters

The dominant parameters, which determine the switching behavior for rapid switching cycles, are the parasitic network parameters L_σ, L_G, L_S, R_L and R_{st}, which result from the circuit arrangement (assumption: constant conditions in the driver circuit, specific FET types). At this point, an indication will be given of how these parameters affect the switching behavior of parallel-connected power FETs.

To clarify the effects of unequal stray inductances, L_G, in the driver circuit – i.e. an asymmetrical circuit arrangement – the FETs were arranged in a row so that the lengths of their gate wiring differed. As **Figure 10** shows, this leads to an asymmetrical split in the current during the switching process. As the stray inductance increases, so the times to switch on and off rise.

The asymmetry in the current split becomes more marked if the stray inductance L_S is also increased by long lengths of wiring. During the current commutation phase, a voltage is induced in the stray inductance L_S, and this opposes the applied gate-source voltage, thus lengthening the switching times.

Because of the induced counter-voltage for parallel FETs which open or close earlier, the stray inductance L_S is the dominant variable for high-frequency oscillations in the voltage range $V_{th} \leq v_{GS} \leq \pm 2$ V.

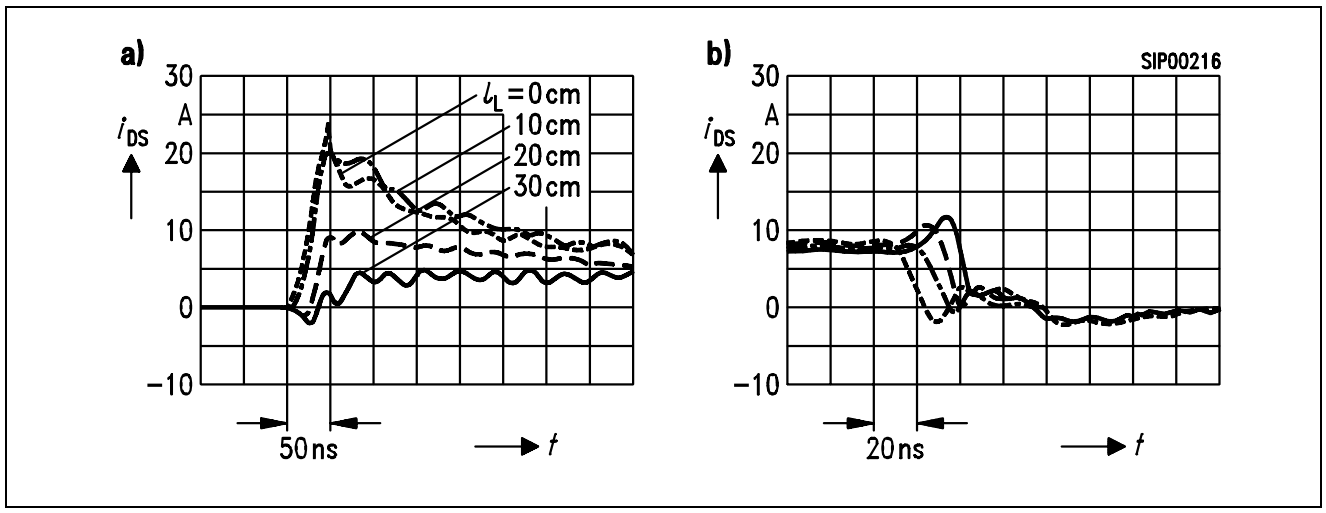

Figure 10
Oscillogram of the Drain Current Waveform with Different Lengths of Wiring in the Gate Circuit (L_σ differs) and a Bipolar Driver Impulse ($V_{GS} = \pm 15$ V)
a) Switch-on Process
b) Switch-off Process

The "fictitious" resistance R^*_S in the source circuit, due to the stray inductance L_S, can be deduced for the case when $L_\sigma = 0$ from the differential equation for the gate-source voltage, as follows:

$$C_{GS} \times L_S \times d^2 v_{GS} / dt^2 + (R_S \times C_{GS} + L_S \times g_{fs}) dv_{GS} / dt + v_{GS} = V_{st}$$ **equation 7**

Using the basic equation $dv_{GS}/dt = i_{GS}/C_{GS}$ it can be seen that, in addition to the resistance R_{st} in the driver circuit, another fictitious resistance $R^*_S = L_S \times g_{fs}/C_{GS}$ comes into effect. A rough estimate shows that even a small stray inductance L_S can have a major effect (e.g : g_{fs} = 6 Ω^{-1}...10 Ω^{-1}, C_{GS} = 3 nF ... 4 nF and L_S = 10 nH gives R^*_S = 15 Ω ... 32 Ω).

Figure 11 shows that the FET with the smallest stray inductances, L_G and L_S, briefly carries almost the entire load current during switch-on, until the FETs connected in parallel with it take over their branch current one by one. On the other hand, during switch-off the FET with the largest stray inductance carries the current for longest.

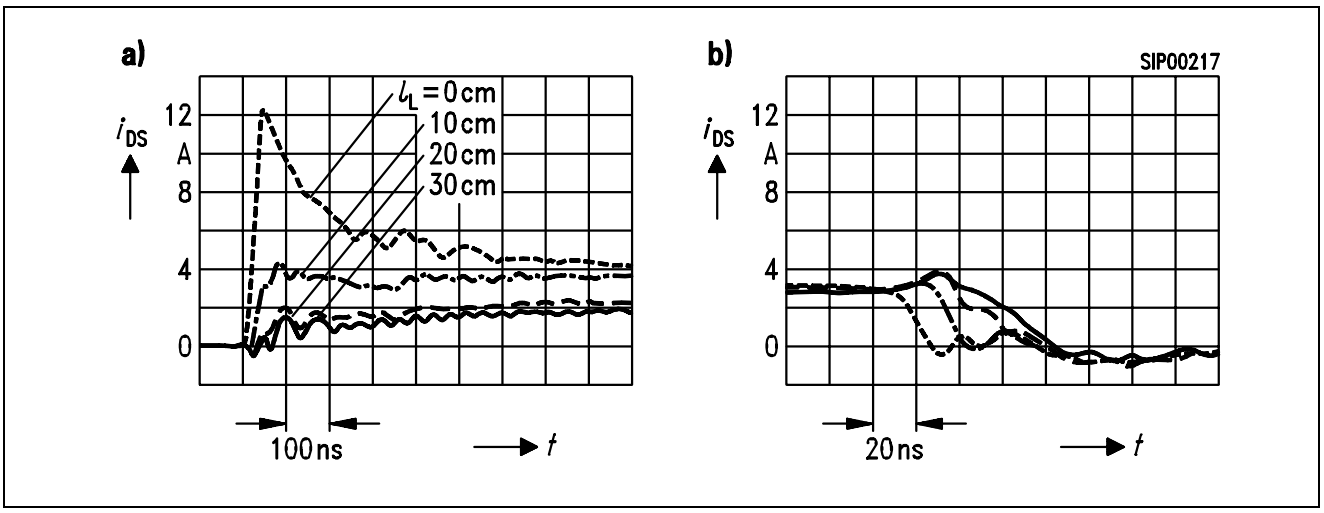

Figure 11
Oscillogram of Drain Current Waveform with Different Length of Wiring in the Source Circuit (L_S differs) and V_{GS} = ± 15 V
a) Switch-on Process
b) Switch-off Process

Whereas the stray inductances L_G and L_S can with no great difficulty be reduced to a tolerable level by careful circuit layout, doing so takes most effort in the case of L_σ, because L_σ represents the total stray inductance of the load circuit, in which greater wiring lengths are often necessary. For a constant signal source voltage, it is the stray inductance L_σ (assuming L_S = 5 nH ... 20 nH) together with the resistance R_{st} which characterizes the switching behavior. A high driver current i_{st} ($R_{st} \rightarrow 0$) implies a high di_D/dt in the output circuit, so that a large voltage is induced in the stray inductance L_σ, which results in a rapid change in the drain-source voltage, dv_{DS}/dt. The consequence of this is that the full driver current is no longer available for building up the gate-source voltage, and hence to invert the FET channel, but instead the C_{GD} capacitance discharges (i_{GD} = $C_{GD} \times$ dv_D/dt). This implies an increase in the switching time. During switch-on, the stray inductance L_σ acts as a switching load. During switch-off, on the other hand, the voltage induced in L_σ adds to the drain source voltage, and thus endangers the voltage bearing capacity of the power FET. Although power FETs can withstand brief overloads in the “avalanche” region it is precisely during very fast switching processes that a drain-source protection circuit is essential. **Figure 12** shows the effect of the stray inductance L_σ on the switch-on and switch-off processes. This makes it clear that as the stray inductance L_σ increases the channel build-up is reduced, so that during switch-on the greatest current flows in the parallel circuit with the lowest stray inductance. On the other hand, during switch-off it is the FET with the lowest stray inductance L_σ which switches off first.

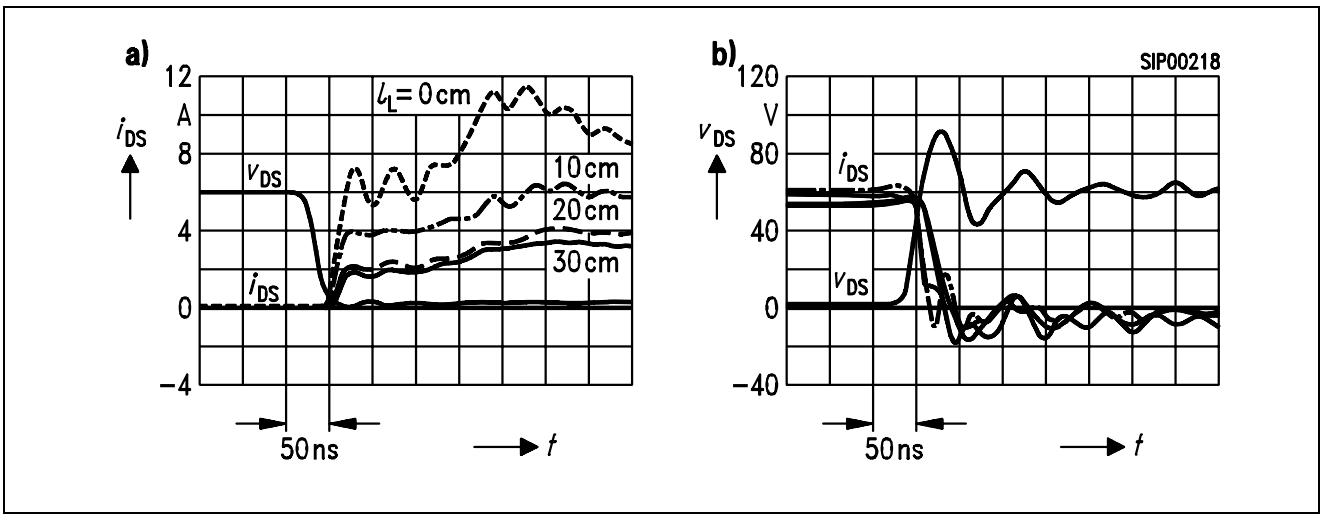

Figure 12
Oscillogram of the Drain Current and Drain-source Voltage Waveforms for Different Lengths of Wiring for the Drain (variable L_σ) and V_{GS} = ± 15 V
a) Switch-on Process
b) Switch-off Process

4 Requirements Imposed on the Driver Circuit, the Network Layout and Device Circuit

From the influencing parameters mentioned above (**Figures 4** to **12**), which determine the switching behavior, it is possible to deduce the following requirements which must be met to ensure reliable and problem-free parallel process:

Control Circuit

- Sufficiently high gate-source voltage to minimize the “saturation losses”; in this connection, note that $R_{DS,on} = f(v_{GS}, I_D, V_{DS}, \vartheta)$.
- A driver current which allows appropriately rapid switching; the driver circuit should only be loaded with pulsed current.
- Low enough impedance to protect the gate oxide from overvoltages, arising in the output circuit as a result of the switching process and fed back to the input via the C_{GD} capacitance.

Network

- The power FETs should have a highly-symmetrical arrangement, so that their gate, source and drain connections have the same lengths from their respective common points; all wiring lengths should be kept to a minimum; account should be taken of the fact that during switching of power FETs 500 A/µs ... 1000 A/µs can easily be reached; at 1000 A/µs a line inductance of as little as 0.1 µH is thus sufficient to induce a voltage of 100 V.
- Printed ring-shaped surfaces for source and drain, for which high current levels must be taken into account.

- Arrange the conductive tracks and FETs to avoid creating additional parasitic capacitances.
  Suggestion for implementation of parallel-connection as per **Figure 13**.
- Minimize the source stray inductance to the parasitic bond inductance.
  Suggestion for implementation of the layout concept as per **Figure 14**.
- Minimize the parasitic stray inductances for the gate (minimum possible enclosed areas in the driver circuit wiring).
  Suggestion for implementation of the circuit as per **Figure 15**.
- To reduce the stray inductance L_σ, good arrangement of the freewheeling diode (assuming a suitable freewheeling diode), and short wiring leads in the load circuit.
  Suggestion for implementation of the circuit as per **Figure 16**.
- Mount all FETs on a heat sink.
- Make use of any wiring inductances which cannot be eliminated (switching load reduction!).
- Sufficiently low-resistance and powerful driver circuit, with a bipolar output impulse.

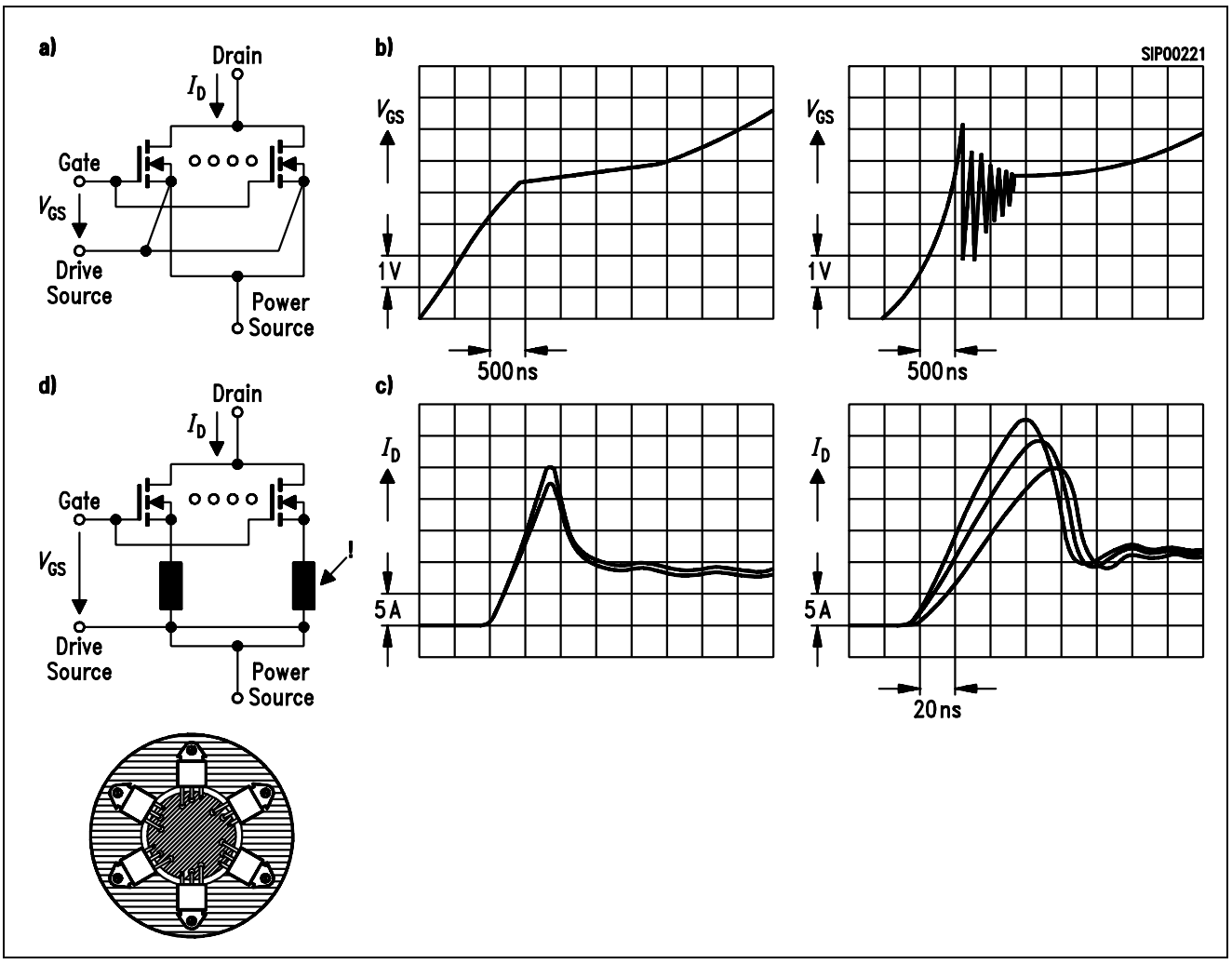

Figure 13
The Electrical Values of a Module with Hybrid Chip Design (Fig. a and d top, Fig. b and c left) Compared to those of the Discrete Parallel Circuit (bottom and right) of Discrete Transistors.
A Module with Hybrid Chip Design
a) is not Influenced by Negative Feedback
b) has no Oscillator Effects during the Dynamic Intervals
c) has a Symmetric, Static and Dynamic Current Distribution (the left Figure shows two of the six Waveforms)
d) does not cause Problems for Mounting

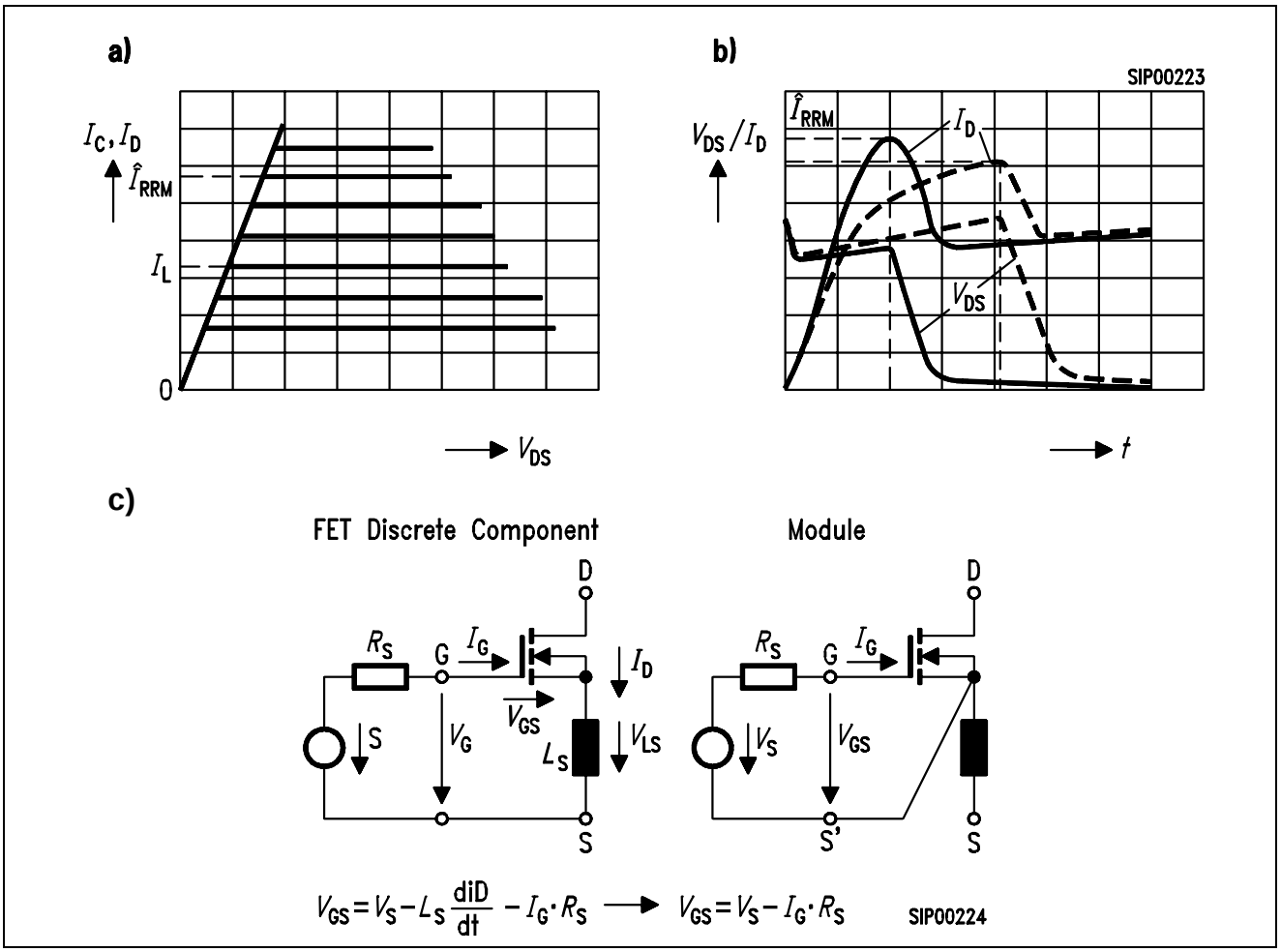

Figure 14
Transient Response of Current with Sufficient Effective Gate-Source-Voltage $V_{GS(t)}$ (a) and a Gate-Source-Voltage that is too low (b). Influence of Parasitic Source Inductance L_S on the Switching Process; no Negative Feedback Effect of the Module (c).

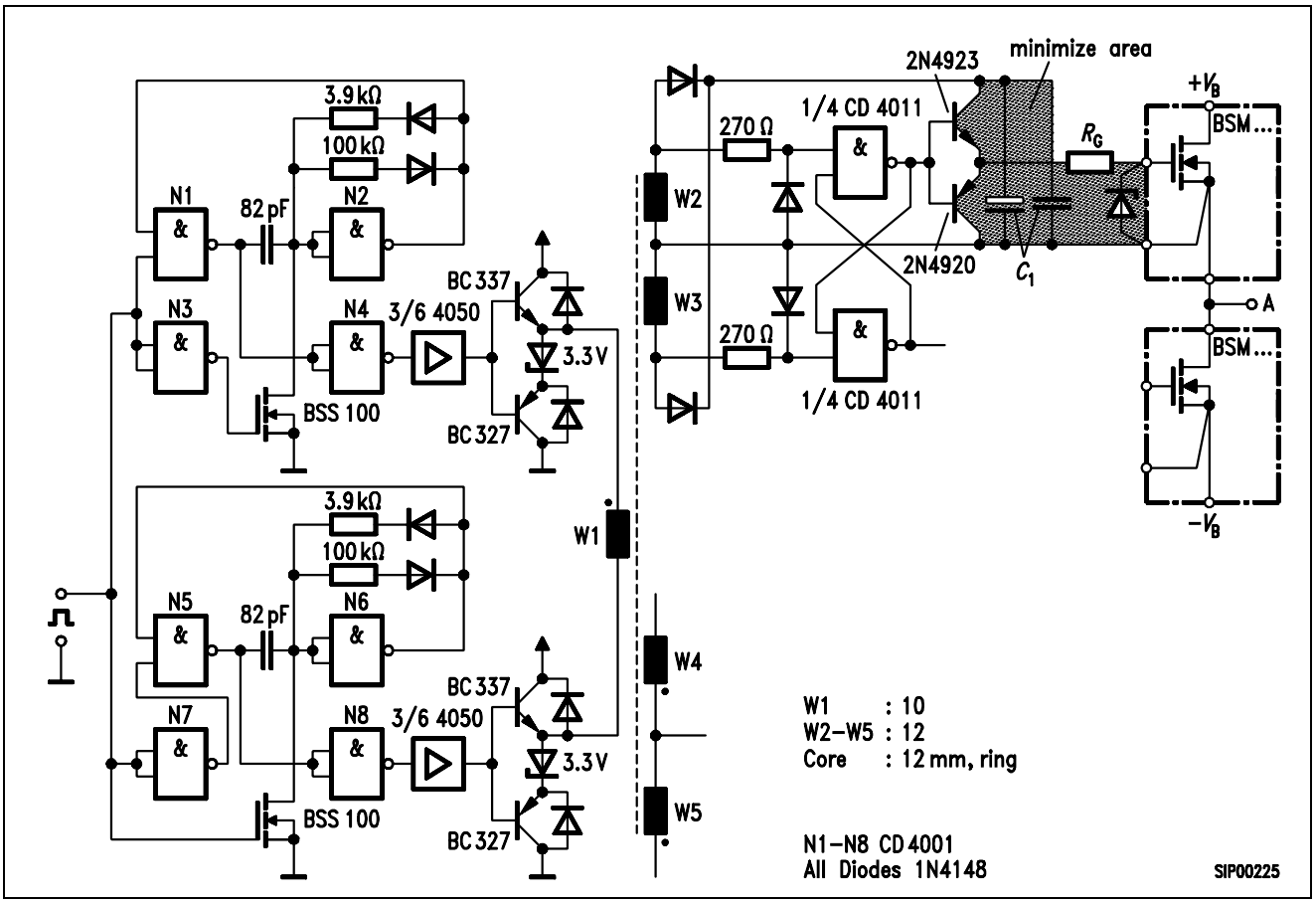

Figure 15
Tested Control Circuit suitable for Sequential Circuit and Half-bridge Design

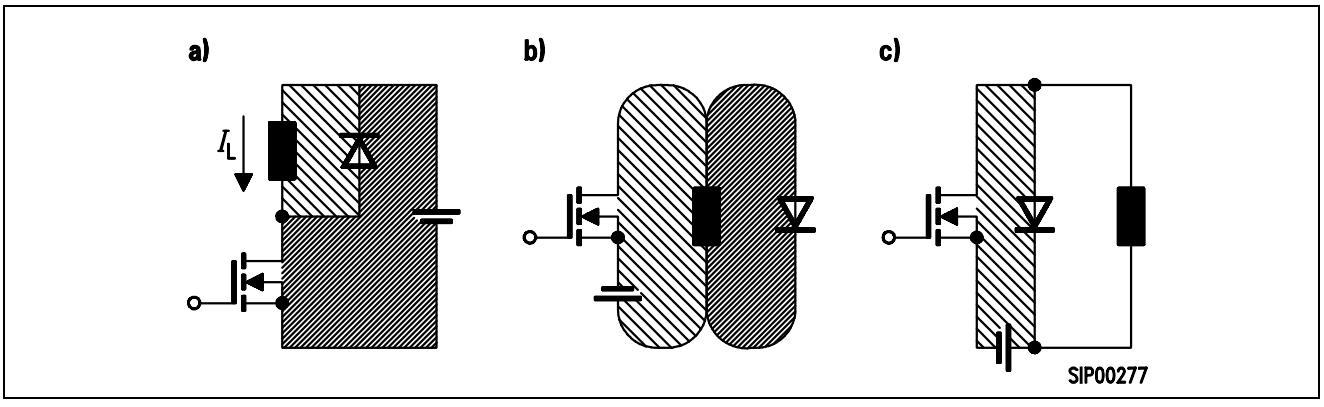

Figure 16
Possibility to Minimize the Parasitic Inductance in the Load Circuit
a) d. c. Chopper without Minimizing the Area (L great)
b) Separating and Freewheeling Circuit
c) Minimizing the Parasitic Inductance of Communication Circuit

Device Circuit

- Even though the driver circuit has a low-impedance output stage, provide input protection circuitry (suppresser diodes).
- Because of the unavoidable stray inductance L_σ, the FET will be briefly driven into "avalanche" breakdown during switch-off when the current commutation transductance is high; the energy stored in the stray inductance L_σ ($0.5 \times L_\sigma \times i_D^2$) must be small enough to avoid overloading the FET thermally.
- Small "reverse recovery" storage charge, Q_{rr}, for the freewheeling diode; in this connection it should be noted that the "recovery" current amplitude rises exponentially as the switching time increases.

5 Current Balancing

If all the points itemized above are taken into account, power MOSFETs can be parallel-connected without problem. One very good approach is that of "hard" switching, because in this case the device tolerances have no notable effect on the switching process (assuming a suitably developed arrangement of the hardware).

Because of the finite stray inductance L_S in the source circuit, it is possible for the voltage induced in L_S – namely $v_{LS} = L_S \times d(i_D + i_S)/dt$ – to produce an oscillatory tendency when there is an under-shoot or over-shoot of the threshold voltage V_{th}, which will be be damped by a low resistance (up to 8 Ω) in the gate circuit of each parallel branch.

Another good method of current balancing is to use ferrite beads in the source circuit. Although this does increase the dynamic loss of power, it does balance the current split, because the highest reverse voltage is induced in the FET with the largest current flow, and hence the switching time is reduced.

Figure 17a to **Figure 17c** show the current and voltage waveforms for six parallel-connected FETs during switch-on and switch-off, as oscillograms for three methods of current balancing; namely, when balancing is effected by the frequently-quoted method of putting a balancing resistance in the driver circuit (**Figure 17a**), or by a ferrite bead in the source circuit (**Figure 17b**). **Figure 17c** shows the behavior with no additional devices when "hard" drive is used. It should be noted in this connection that the last-named method results in very good dynamic behavior during switching processes.

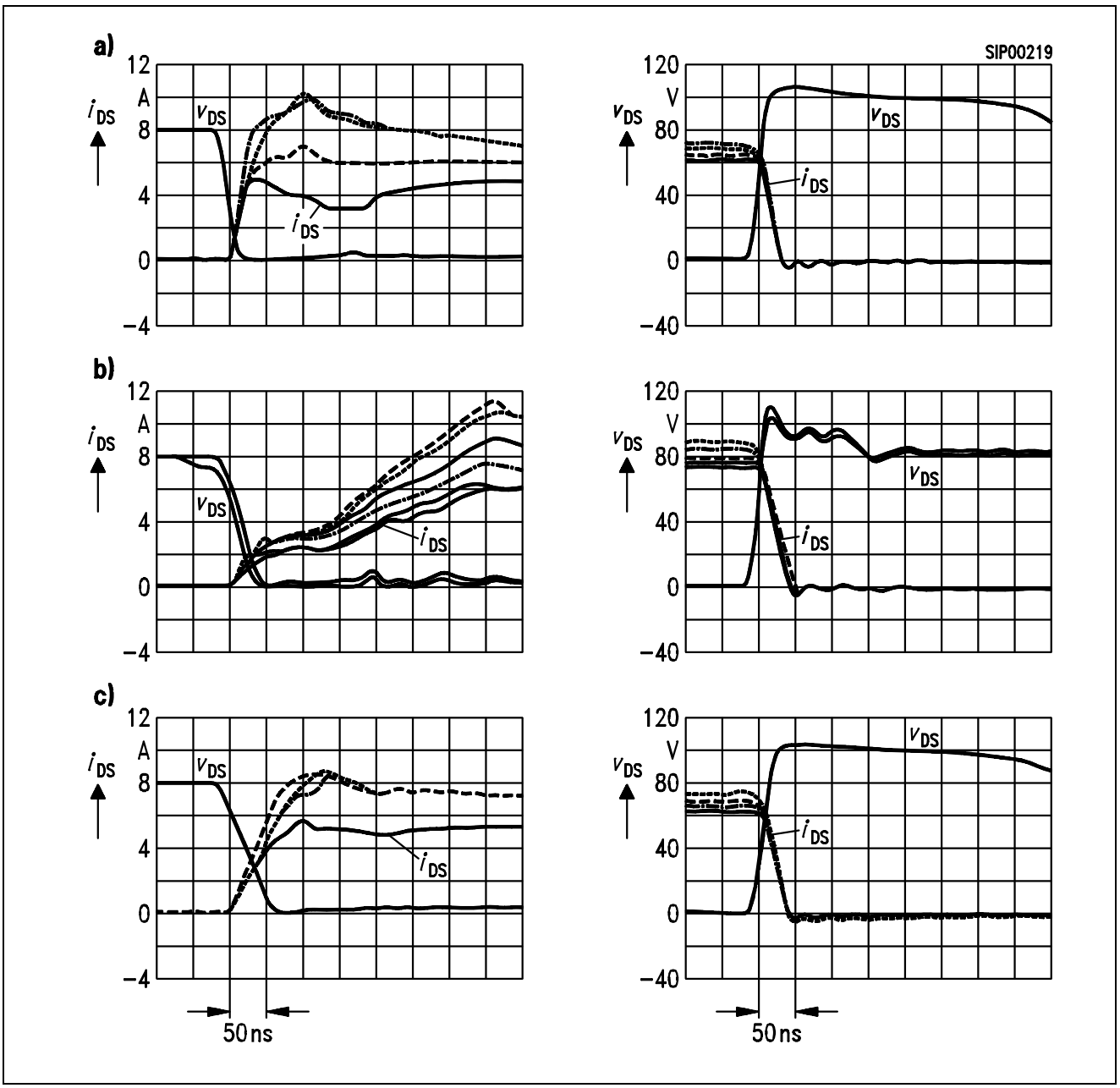

Figure 17
Current and Voltage Waveforms (Oscillogram) for six Parallel-connected FETs of the Same Type Using Various Current Balancing Methods, in Dynamic Operation and for V_{GS} = ± 15 V
Left: Switch-on Process; Right: Switch-off Process
a) Using Gate Resistors, $R_{st1 \ldots 6}$ = 10 Ω
b) Using Ferrite Beads in the Source Circuit, $R_{st1 \ldots 6}$ = 0 Ω
c) Using "Hard" Drive, right with no Additional Devices

The total power dissipation of a semiconductor switch consisting of six parallel-connected FETs, when the switched current is 72 A and at a voltage of V_{DS} = 80 V, is shown in **Figure 18** as a function of the switching frequency (pulse separation ratio 1:1). This figure also shows the subcomponents of the power loss. The semiconductor switch was “hard” driven, and included an RCD circuit.

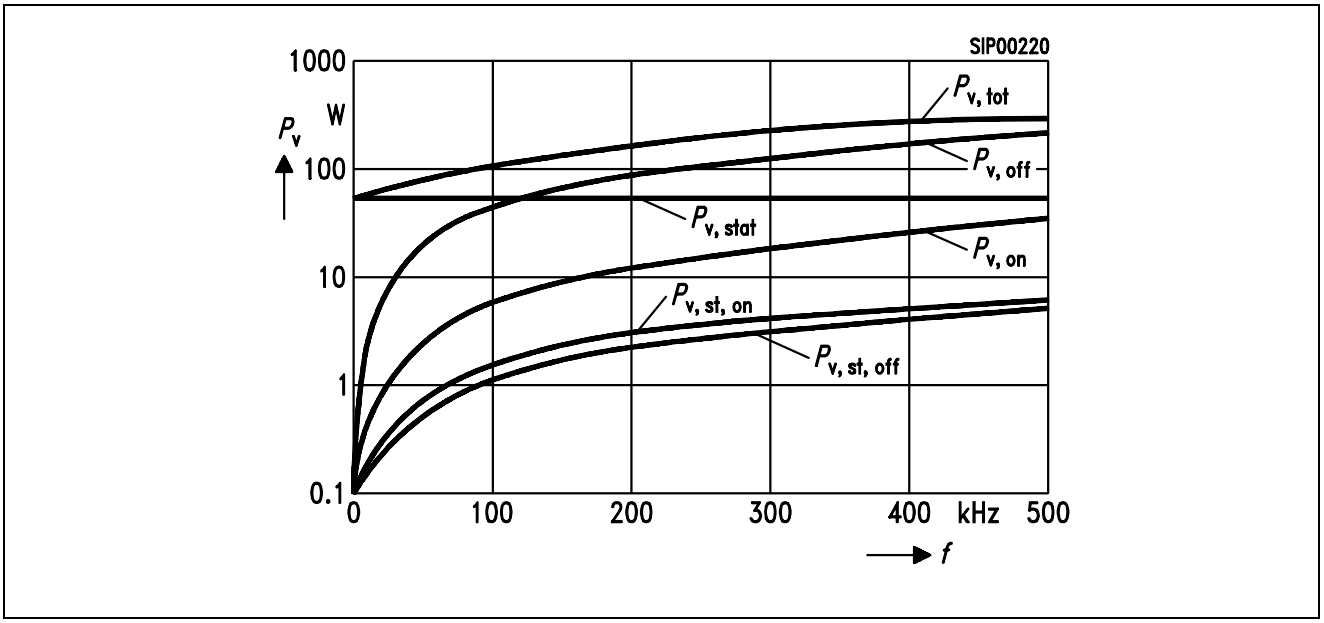

Figure 18
Power Loss (Measured) in a Semiconductor Switch Consisting of six Power MOSFETs Connected in Parallel, as a Function of the Frequency
(I_{ges} = 72 A; V_{DS} = 80 V; T = 25°C)

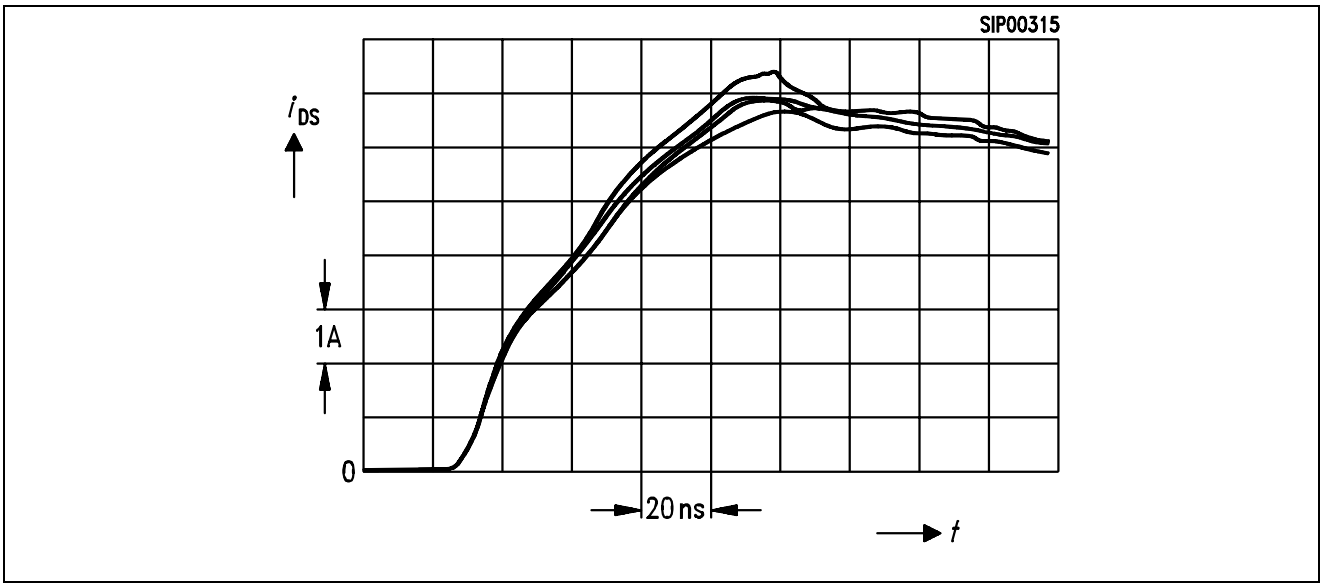

Figure 19
Drain Current Waveform During Switch-on of Four Parallel-connected High-voltage Power FETs (Oscillogram)

Whereas **Figure 17** compares the switching behavior for low-voltage FETs (V_{DS} = 100 V), **Figure 19** shows the waveforms for switching using high-voltage FETs (V_{DS} = 1000 V). Here too, it is evident that for “hard switching” (with no gate resistance and no ferrite beads in the source circuit) the dynamic current split is very symmetrical.