Version 1.0 , Aug 2004

Datasheet

DS-CoreControl-TDA21203

TDA21103

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http://www.infineon.com/DCDC

Power Management & Supply

Never stop thinking.

Contents:

High speed Driver with bootstrapping for dual Power MOSFETs

P-DSOP-14

Features :

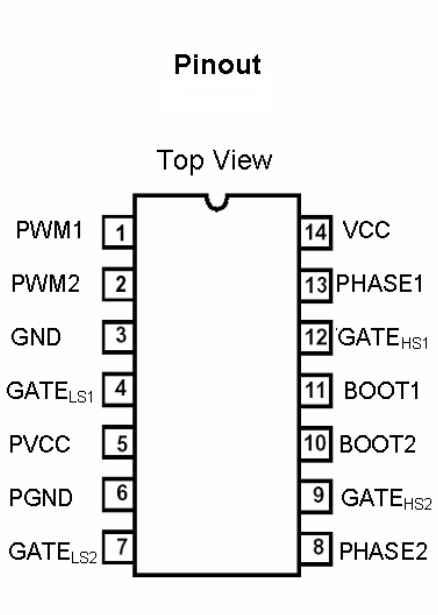
- Fast rise and fall times for frequencies up to 1 MHz
- Changes the High Side and Low Side MOSFET´s gate to 6..12 V according to PVCC setting.
- Adjustable High Side and Low Side MOSFET gate drive voltage via PVCC pin for optimizing ON losses and gate drive losses
- Integrates the bootstrap diode for reducing the part count
- Prevents from cross-conducting by adaptive gate drive control
- Supports shut-down mode for low quiescent current through three-state input
- Compatible to standard PWM controller ICs (Intersil, Analog Devices)
- Floating High Side MOSFET drive
- Power-On Overvoltage Protection
- Ideal for multi-phase Desktop CPU supplies on motherboards and VRM´s

Application :

- Voltage Regulator Modules
- Low Output Voltage High Output Current DC-DC Converters

Type	Package	Marking	Ordering Code
TDA21103	P-DSOP-14	21103	Q67042-S4252

Pinout Drawing and Description :



Number	Name	Description
1	PWM1	Input for the PWM1 controller signal
2	PWM2	Input for the PWM2 controller signal
3	GND	Ground
4	GATE$_{LS1}$	Gate drive output for the N-Channel Low Side MOSFET 1.
5	PVCC	Input to adjust the High Side gate drive
6	PGND	Power ground return for the Low Side Drivers
7	GATE$_{LS2}$	Gate drive output for the N-Channel Low Side MOSFET 2.
8	PHASE2	To be connected to the junction of the High Side and the Low Side MOSFET 2
9	GATE$_{HS2}$	Gate drive output for the N-Channel High Side MOSFET 2.
10	BOOT2	Floating bootstrap pin. To be connected to the external bootstrap capacitor to generate the gate drive voltage for the High Side N-Channel MOSFET 2.
11	BOOT1	Floating bootstrap pin. To be connected to the external bootstrap capacitor to generate the gate drive voltage for the High Side N-Channel MOSFET 1.
12	GATE$_{HS1}$	Gate drive output for the N-Channel High Side MOSFET 1.
13	PHASE1	To be connected to the junction of the High Side and the Low Side MOSFET 1
14	VCC	Supply Voltage

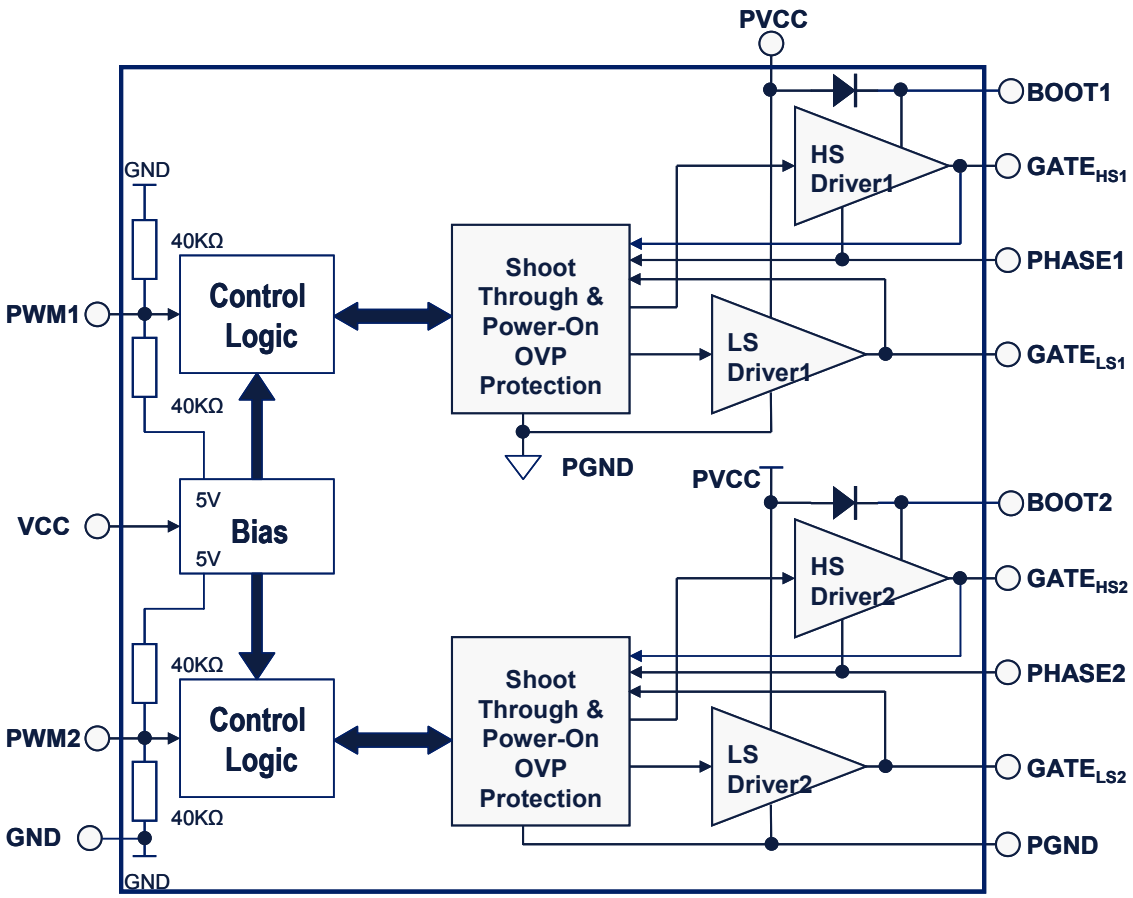
General Description

The dual high speed driver is designed to drive a wide range of N-Channel low side and N-Channel high side MOSFETs with varying gate charges. It has a small propagation delay from input to output, short rise and fall times and the same pin configuration as the HIP6602B. In addition it provides several protection features as well as a shut down mode for efficiency reasons.

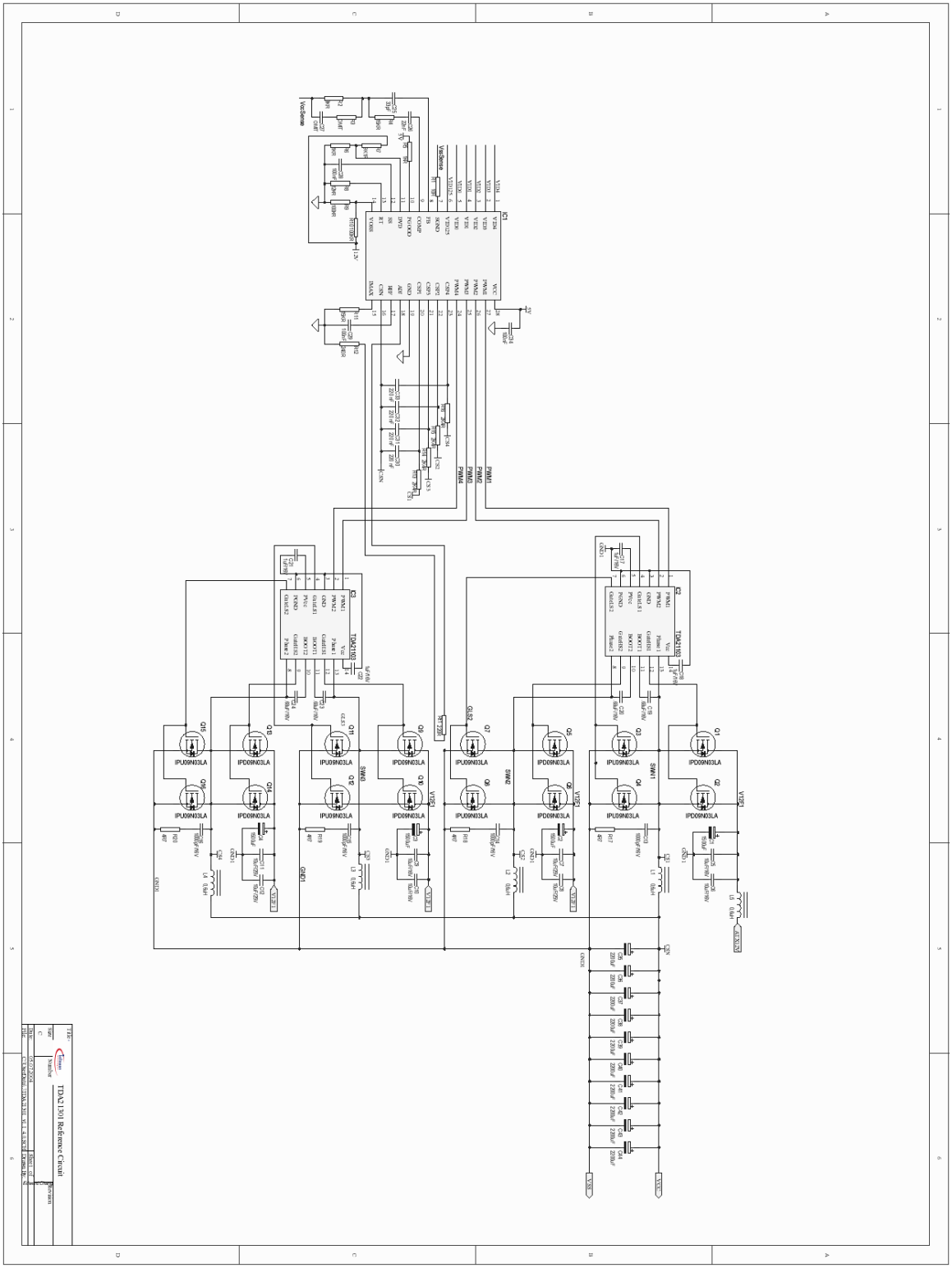
Target application

The dual high speed driver is designed to work well in half-bridge type circuits where dual N-Channel MOSFETs are utilized. A circuit designer can fully take advantage of the driver´s capabilities in high-efficiency, high-density synchronous DC/DC converters that operate at high switching frequencies, e.g. in multi-phase converters for CPU supplies on motherboards and VRM´s but also in motor drive and half bridge class-D amplifier type applications.

Block Diagram



Application Circuit



Absolute Maximum Ratings

At Tj = 25 °C, unless otherwise specified

Parameter	Symbol	Value		Unit
		Min.	Max.	
Voltage supplied to 'VCC' pin; DC	V_{VCC}	-0,3	15	V
Voltage supplied to 'PVCC' pin; DC	V_{PVCC}	-0,3	V_{CC}+0,3	
Voltage supplied to 'PWM' pin	V_{PWM}	-0,3	7	
Voltage supplied to 'BOOT' pin referenced to 'PHASE'	$V_{BOOT} - V_{PHASE}$	-0,3	15	
Voltage supplied to 'BOOT' pin referenced to 'GND'	V_{BOOT}	-0,3	30	
Voltage rating at 'PHASE' pin, DC	V_{PHASE}	-4	15	
Junction temperature	T_J	0	125	°C
Storage temperature	T_S	-40	150	
Lead temperature (Soldering, 10 seconds)			260	
ESD Rating; Human Body Model Machine Mode			2 200	KV V
IEC climatic category; DIN EN 60068-1		55/ 150/ 56	-	

Thermal Characteristic

Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
Thermal resistance, junction-soldering point					K/W
Thermal resistance, junction-ambient			127		

Operating Conditions

At Tj = 25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Voltage supplied to 'VCC' pins	V_{VCC}		10,8		13,2	V
Voltage supplied to 'PVCC' pins	V_{PVCC}		6		13,2	V
Input signal transition frequency	f		0,1		1	MHz
Power dissipation	P_{TOT}	T_A = 25 °C, T_J = 125 °C		0,75		W
Junction temperature	T_J		0		125	°C
Ambient temperature	T_A		0		70	°C

Electrical Characteristic

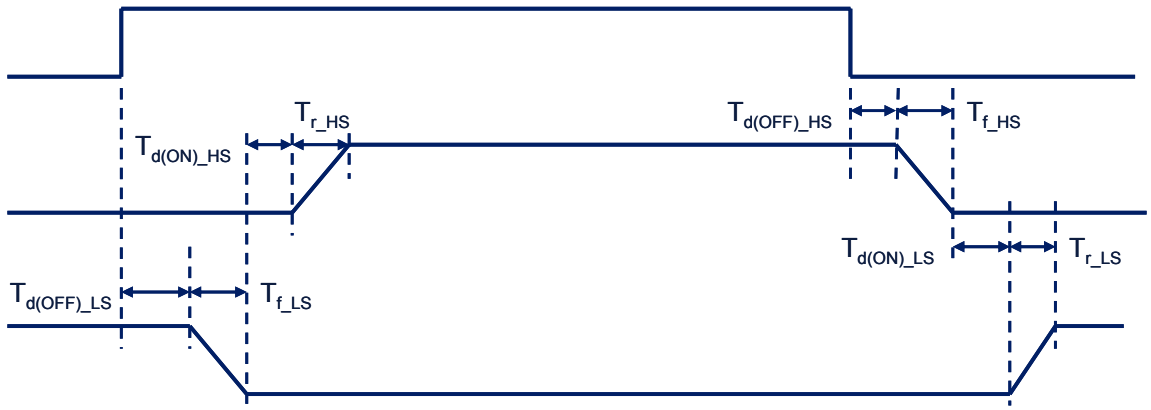
At Tj = 25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Supply Characteristic						
VCC supply current Bias Current Power Supply Current	 I_{VCC} I_{PVCC}	f =250 KHz, V_{PVCC} = V_{VCC} = 12 V C_{BOOT}=0.1uF, R_{PHASE} = 20 Ω		 5,5 5,5	 8 10	mA
Under-voltage lockout		V_{VCC} rising threshold	8,6	9,9	10,7	V
Hysteresis			0,6	1,35		
Input Characteristic						
Current in 'PWM' pin	I_{PWM_L}	$V_{\_PWM}$ = 0 V	-80	-127	-150	µA
Current in 'PWM' pin	I_{PWM_H}	$V_{\_PWM}$ = 5 V	80	127	150	
PWM pin open	V_{PWM_O}		1,1	2,1	3,7	
PWM Low level	V_{PWM_L}		1,0	1,26	1,5	V
PWM High level	V_{PWM_H}		3,3	3,7	4,3	

At Tj = 25 °C, unless otherwise specified

Dynamic Characteristic						
Turn-on propagation Delay High Side	$t_{d(ON)\_HS}$	P_{PVCC} = V_{VCC}= 12 V C_{ISS} = 3000 pF				ns
Turn-off propagation delay High Side	$t_{d(OFF)\_HS}$			60		
Rise time High Side	t_{r_HS}			30		
Fall time High Side	t_{f_HS}			40		
Turn-on propagation Delay Low Side	$t_{d(ON)\_LS}$					
Turn-off propagation delay Low Side	$t_{d(OFF)\_LS}$			45		
Rise time Low Side	t_{r_LS}			30		
Fall time Low Side	t_{f_LS}			30		

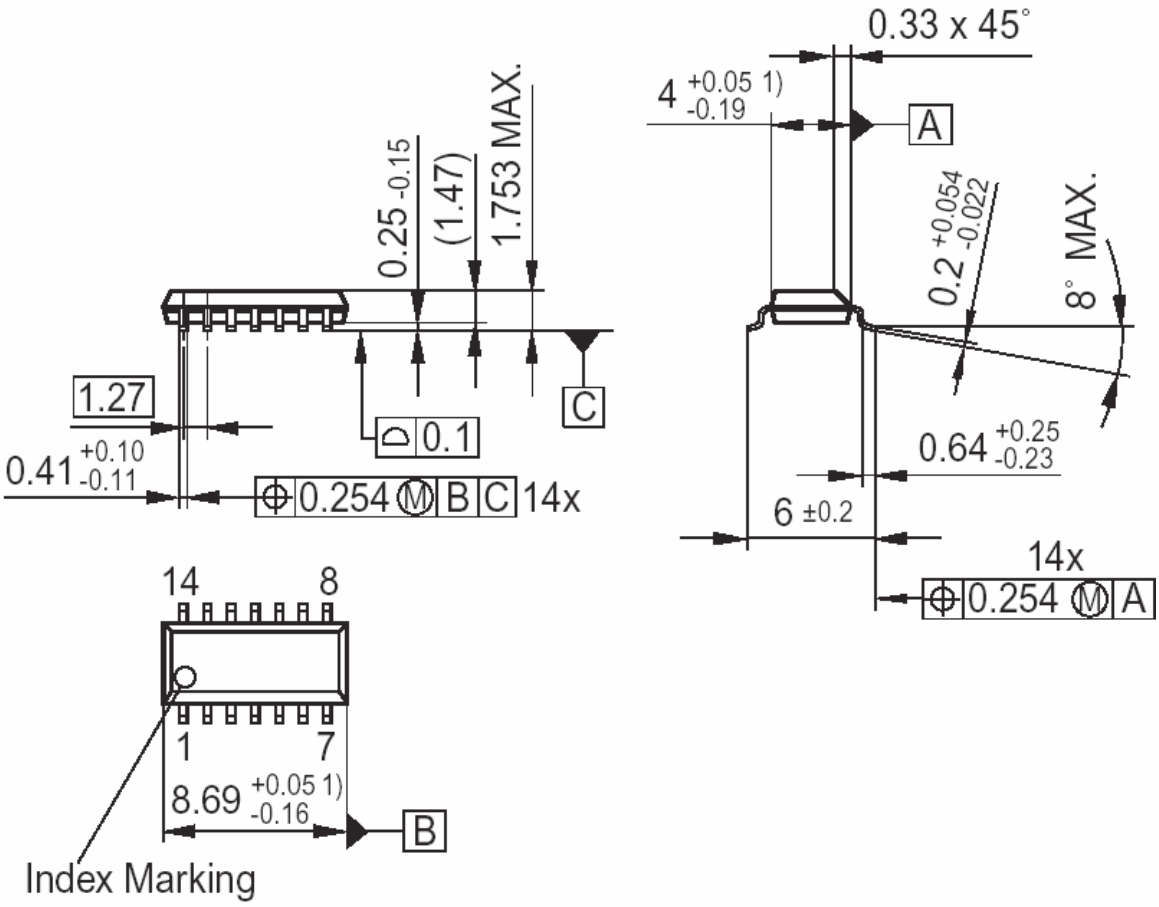
Timing diagram



At Tj = 25 °C, unless otherwise specified

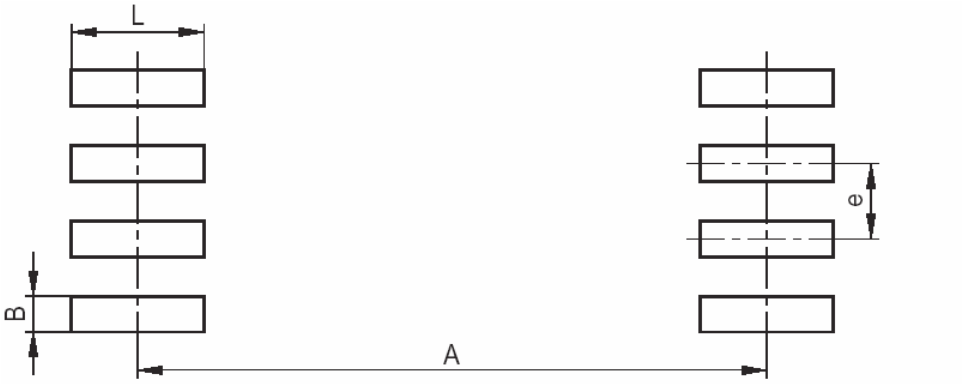
Parameter		Conditions	Values			Unit
			Min.	Typ.	Max.	
Output Characteristic High Side (HS) and Low Side (LS), ensured by design						
Output Resistance	HS; Source	V_{PVCC} = V_{VCC}= 12 V		1,75	3,0	Ω
	HS; Sink	V_{PVCC} = V_{VCC}= 12 V		2,8	5,0	Ω
	LS; Source	V_{PVCC} = V_{VCC}= 12 V		1,9	3,0	Ω
	LS; Sink	V_{PVCC} = V_{VCC}= 12 V		1,6	3,0	Ω

Package Drawing P-DSO-14



1) Does not include plastic or metal protrusion of 0.25 max. per side

Layout Footprints



e	A	L	B
1,27 mm	5,69 mm	1,31 mm	0,65 mm

Revision History			
Datasheet DS-CoreControl-TDA21103			
Actual Release: V1.0 Date: 10.08.2004		Previous Release:	Date:
Page of actual Rel.	Page of prev. Rel.	Subjects changed since last release	

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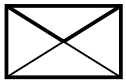

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