AND8035/D

CS51227 in a 112 W Boost Converter Application

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APPLICATION NOTE

INTRODUCTION

This design note describes the design and operating characteristics of a 112 W Boost Converter based on the CS51227 Enhanced Voltage Mode PWM Controller. The design discussed herein converts an input voltage range of 10–18 VDC to 28 VDC at an output current of 4.0 A.

CS51227 Controller

The CS51227 is a fixed frequency, single output pulse–width–modulated controller using feed forward voltage mode control. This controller also features:

- 1.0 MHz Frequency Capability
- Low Voltage Start–Up

- Undervoltage Lockout (UVLO)
- Low Start–Up Current
- Thermal Shutdown
- 1.0 A Source/Sink Gate Drive
- Pulse by Pulse Current Limiting with Leading Edge Blanking
- Programmable Volt–Second Clamp

A block diagram of the IC is shown below in Figure 1. Please refer to the product data sheet for a detailed description of the device and its functional blocks.
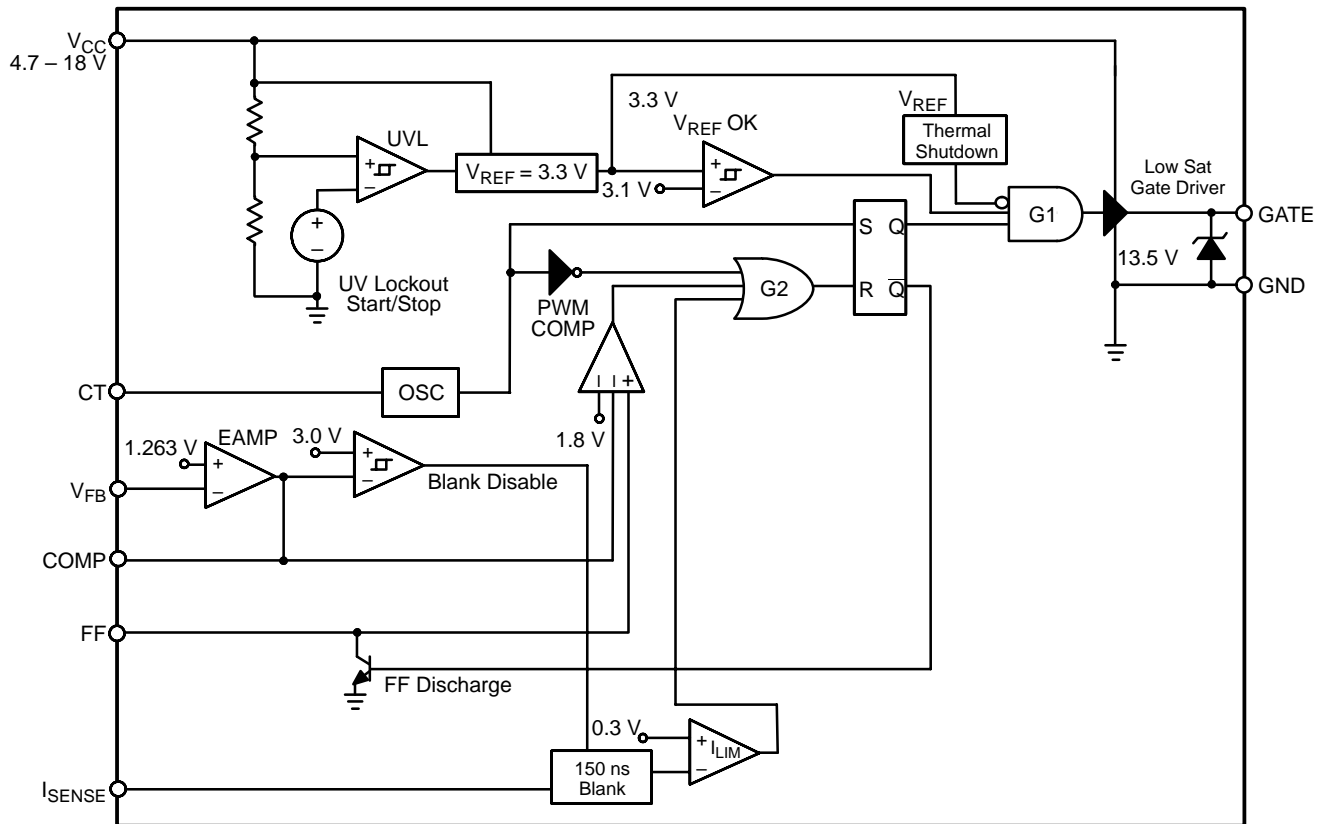

**Figure 1. Functional Block Diagram of the CS51227**

Boost Converter Topology

This power supply is a boost or step–up converter, which converts an unregulated input voltage to an output that is always greater that the input voltage. Figure 2 depicts a simplified schematic of a boost converter. The circuit consists of a control block, a switch (Q1), a diode (D1), inductor (L1) and output capacitor (C1).
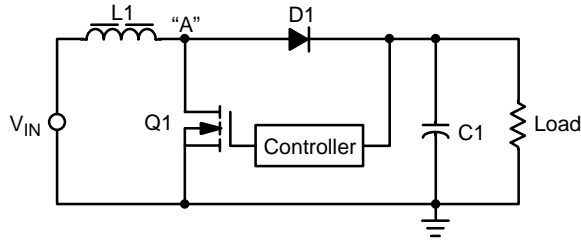
Figure 2. Simplified Boost Converter Schematic

During normal operation the switch (Q1) is continuously switched between the "on" and "off" state by the controller to maintain output regulation. As a result of the switching, a repetitive pulse train is created at the junction of the switch, diode and inductor (labeled as "A" on Figure 2). A filter formed with the output capacitor transforms this pulse train to a DC output voltage. In the simplest case, continuous–conduction mode explained in the next section, the circuit has two states during each switching cycle. In the "on" state of the switch (Q1), energy is stored in inductor (L1), D1 is reversed biased and the load current is supplied by the output capacitor (C1). And conversely during the "off" state of the switch, stored energy in the inductor is transferred to the load through the now forward biased diode (D1). The boost converter has two distinct modes of operation characterized by the current waveform of the inductor. These modes are referred to as continuous–conduction mode (CCM) or discontinuous–conduction mode (DCM). In CCM, the inductor current is greater than zero after each switching cycle, and in DCM the inductor current falls to zero after each switching cycle. Figure 3 shows the topological circuit state diagrams for the boost converter operating in CCM, followed by Figure 4 which shows typical idealized waveforms of the inductor current, switch current, diode current, and switch off–state voltage (node "A").

Stage I–switch "on",
diode reversed biased

Stage II–switch "off",
diode is forward biased
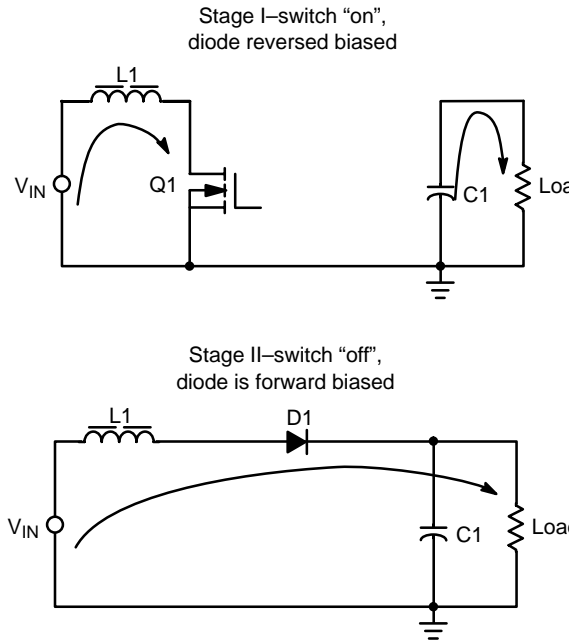
Figure 3. Boost Converter Topological States

An expression relating the input and output voltage may be derived using fundamental circuit parameters. In CCM, the inductor current increase during the "on" state neglecting any loss terms is given by:
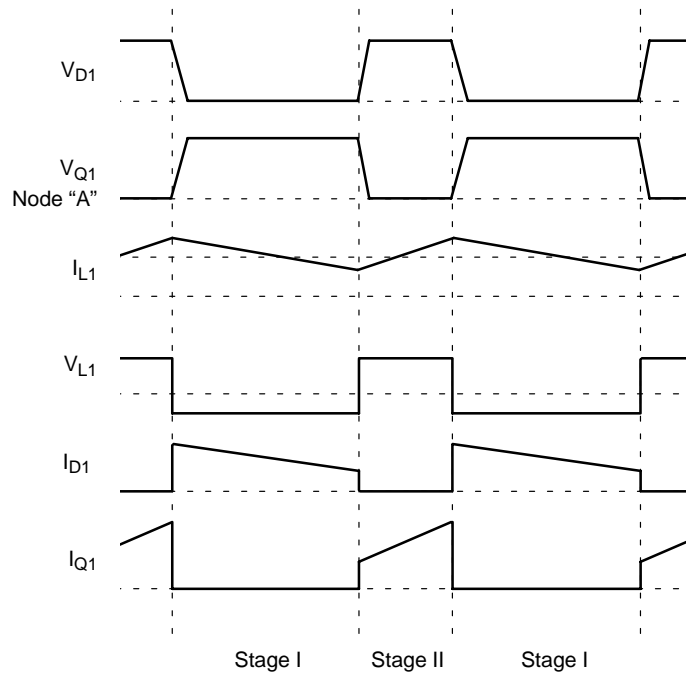
$$\Delta I_{L(+)} = \frac{V_{IN}}{L} \times t_{ON}$$

As previously mentioned during this circuit state the load current is supplied by the output capacitor. When the switch (Q1) is turned off, the inductor current continues to flow through diode (D1) since the inductor current can not change instantaneously. In order for this to occur, the voltage polarity across the inductor reverses due to a decreasing inductor current. The voltage polarity reversal across the inductor commutates the diode to turn on. The voltage across the inductor during the switch "off" time is $V_O – V_{IN}$. The inductor current decreases during the "off" time is given by:

$$\Delta I_{L(-)} = \left(\frac{V_O - V_{IN}}{L} \right) \times t_{OFF}$$

The ripple current in the inductor during the on state ($\Delta I_{L(+)}$) and off state ($\Delta I_{L(-)}$) are equal in steady state. If these quantities were imbalanced, there would be either a net increase or decrease in inductor current from cycle to cycle, which would violate the steady state condition. In addition, equating these two quantities is analogous to the volt–second balancing on the inductor. Equating these two expressions and solving for V_O yields the CCM boost–converter voltage conversion ratio (V_O/V_{IN}):

Figure 4. CCM Idealized Boost Converter Waveforms

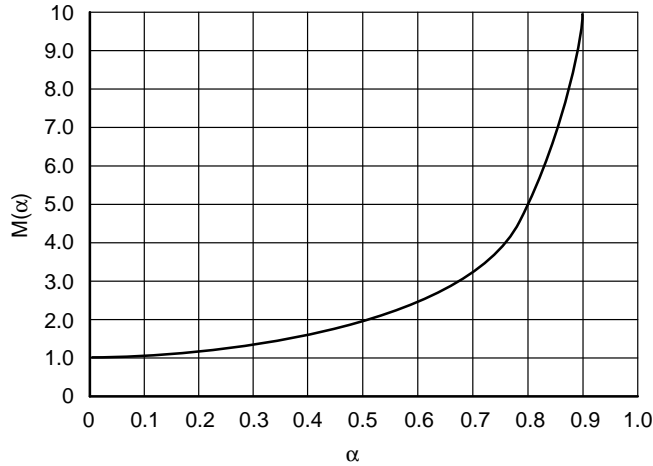$$\frac{V_{IN}}{L} \times t_{ON} = \left(\frac{V_O - V_{IN}}{L}\right) \times t_{OFF}$$

$$\frac{V_O}{V_{IN}} = \left(\frac{t_{ON} + t_{OFF}}{t_{OFF}}\right)$$

Since the continuous–conduction mode only has two states the sum of the "on" and "off" times is the switching period.

$$Ts = t_{ON} + t_{OFF}$$

The switch duty cycle (α) is the ratio of "on" time to the switching period (Ts):

$$\alpha = t_{ON} \times Ts$$

An expression for the off–time (t_{OFF}) can be derived the two expression above in terms of the duty cycle:

$$t_{OFF} = (1 - \alpha) \times Ts$$

Substituting this expression for t_{OFF}, t_{ON} and the switching period Ts into the voltage conversion ratio equation yields:

$$\frac{V_O}{V_{IN}} = \frac{1}{1 - \alpha}$$

A plot of the non–linear voltage conversion ratio ($M = V_O/V_{IN}$) of a boost converter in CCM is shown in Figure 5.

Figure 5. Boost Converter Voltage Conversion Ratio vs. Duty Cycle
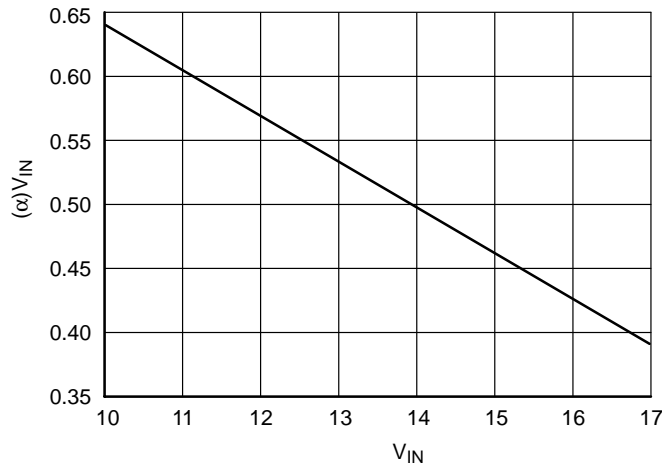
Figure 6. Duty Cycle (CCM Only) Over Operating Input Voltage Range (28 VDC Output)

The voltage conversation ratio graph illustrates that the output voltage is always greater than or equal to the input voltage since the duty ratio is a quantity bounded between 0 and 1. In practical circuits, typically the duty ratio is constrained to values below 80%, which sets an upper bound on the set–up voltage conversion ratio. Assuming CCM, the duty cycle of this converter over the entire input voltage range is shown in Figure 6.

The discussion in the previous sections mainly dealt with the continuous–conduction mode (CCM) of operation since it is the primary operation mode of this converter example. The converter will operate in the discontinuous–mode (DCM) at light loads. The boundary condition between CCM and DCM, is a determined by the input and output voltage, inductance, switch frequency and load current. An expression for this boundary condition presented can be found in (1) and is given by:

$$\frac{M - 1}{2 \times M^3} = \frac{L_C \times f_s}{R_L}$$

Where $M = V_O/V_{IN}$, L_c is the critical inductance, f_s is the switching frequency, and R_L is the load resistance.

Operating Specifications

Input Voltage Range:	10–18 VDC
Output Voltage:	28 V +/– 1%
Output Power Range:	0–112 W
Output Current:	0–4 A
Switching Frequency:	250 kHz
Output Voltage Ripple:	150 mVp–p
Efficiency @ Nom. Line/Load:	90%
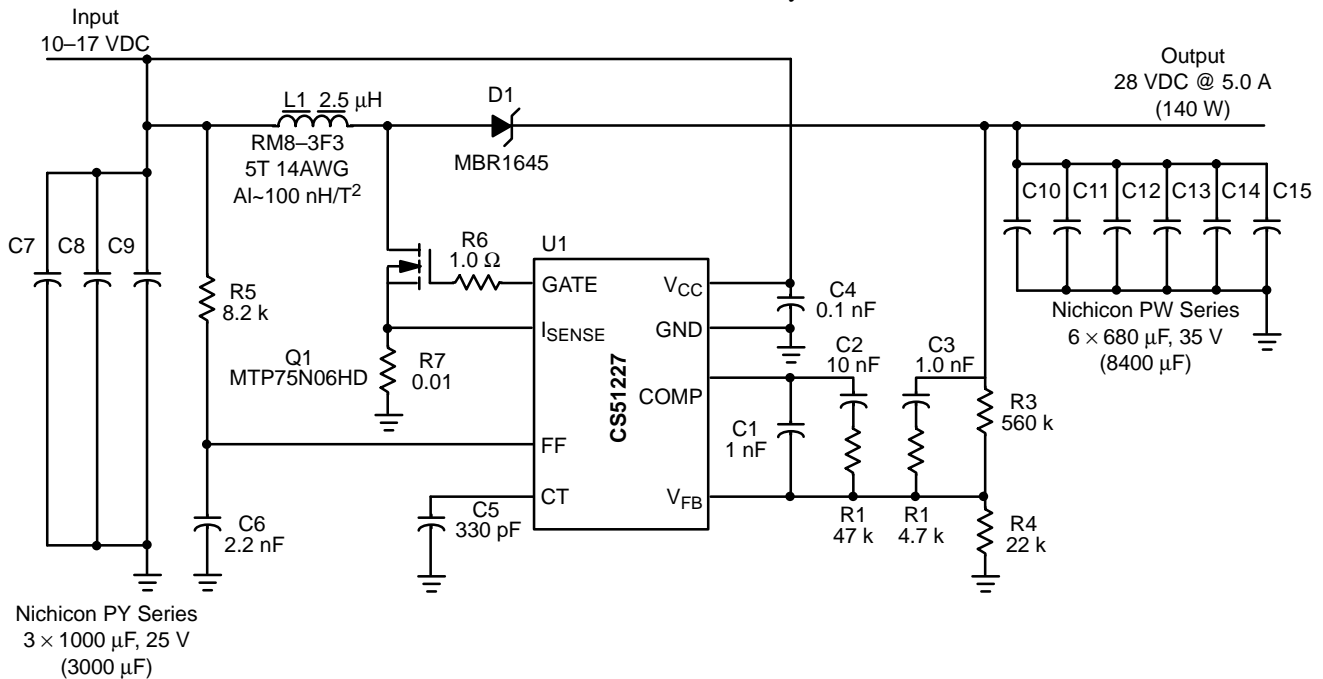
Figure 7. Circuit Schematic
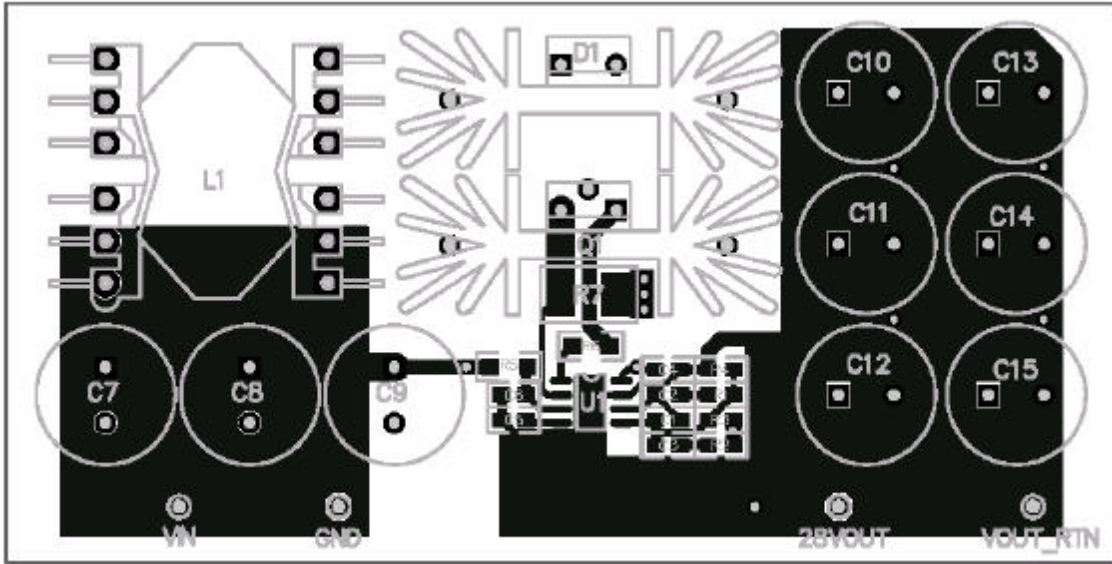
PCB Layout

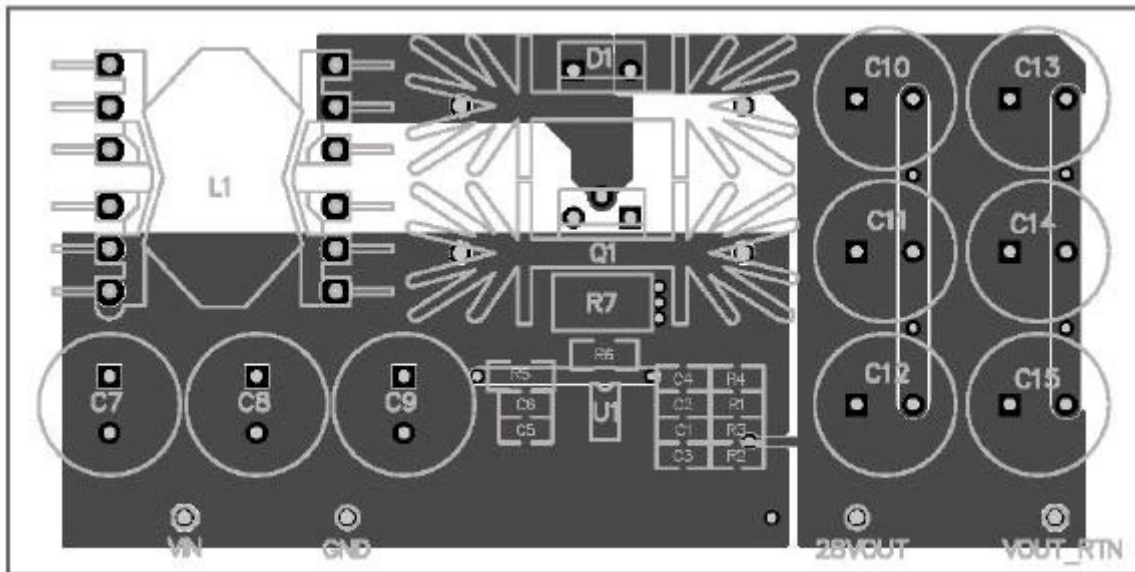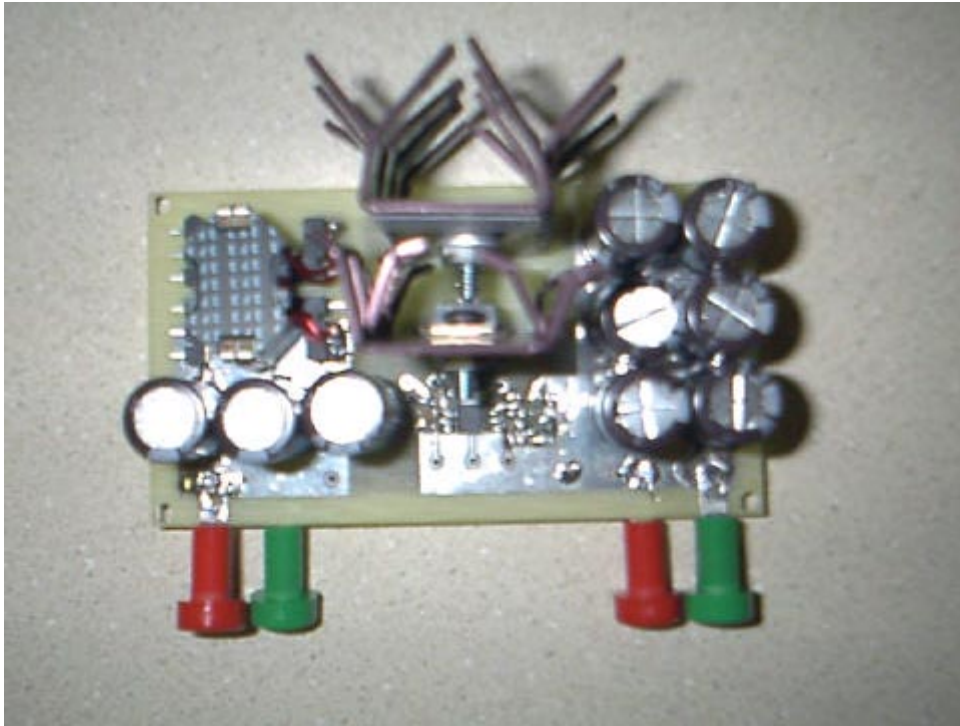**Top Layer (Component Side)**

Figure 8.

Bottom Layer

Figure 9.

Figure 10. Circuit Photograph

Parts List

Designator	Quantity	Value/Rating	Description
R1	1	47 kΩ, 0805	–
R2	1	4.7 kΩ, 0805	–
R3	1	560 kΩ, 0805	–
R4	1	22 k, 0805	–
R5	1	8.2 kΩ, 1206	–
R6	1	1.0 Ω, 1206	–
R7	1	0.01 Ω, 1.0 W, 2510	–
C1	1	1.0 nF, 0805	–
C2	1	10 nF, 0805	–
C3	1	1.0 nF, 0805	–
C4	1	0.1 μF, 0805	–
C5	1	330 pF, 0805	–
C6	1	2.2 nF, 0805	–
C7–C9	3	1000 μF, 25 V	Nichicon PY Series (10 x 12.5 mm)
C10–C15	6	680 μF, 35 V	Nichicon PW Series (10 x 12.5 mm)
D1	1	MBR1645	Schottky 16 A/45 V (TO–220)
L1	1	2.5 μH	RM8–3F3 5T #14 AWG AL=100 nH/T^2
U1	1	CS51227	IC, Enhanced Voltage Mode Controller
Q1	1	MTD60N06HD	N–chan. MOSFET 60 A/60 V (TO–220)

Design Summary

This circuit was fully parameterized with the use of the Power456 software from Ridley Engineering (2). As a brief summary the following sections will describe the PWM converter mode of operation, selection of the switching frequency, boost inductor design, semiconductor component selection, output capacitor, loop compensation and stability, and finally some thermal considerations.

PWM Converter

As previously described the controller for this converter is the CS51227 enhanced voltage mode converter with feed–forward compensation. Voltage–mode control in switch–mode power supplies is characterized by a single control loop that senses the output voltage and compares it to a reference voltage. The output of this error amplifier stage is then applied to a PWM comparator that compares the error voltage to a fixed frequency triangle wave. The output of the PWM comparator is a square–waveform that is then applied to a driver stage to control the switching element. Figure 11, below illustrates a simplified voltage mode control loop.
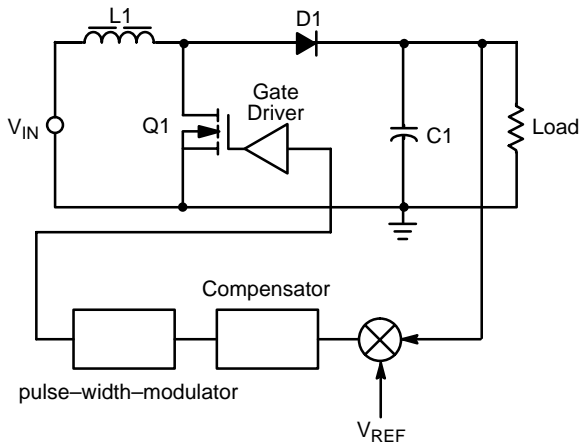
Figure 11. Simplified Voltage Mode Control Loop

Several variations of this basic control method exist, which include steering logic, blanking delays, pulse by pulse current limiting etc. A key variation of the CS51227 is the inclusion of a feed–forward input that allows an input voltage contribution to the control loop. A more thorough discussion about the control loop will follow in a later section.

Switching Frequency

The switching frequency of this converter was chosen at 250 kHz. The switching frequency is the chosen arbitrarily to minimize the size of the boost inductor and limit the loss of the semiconductor devices. At higher frequencies the switching losses in the MOSFET increase, and therefore reduce the overall efficiency of the circuit. At lower frequencies the required output capacitance and boost inductor size increases, and the volumetric efficiency of the supply degrades.

Boost Inductor

Given that the switching frequency is set at 250 kHz, the boost inductor value may be optimally determined to set the converter operating–mode in the required load and line range. The critical inductance is defined as the inductance at the boundary edge between continuous and discontinuous modes and is defined as:

$$L_C = \frac{V_O \times T_S}{I_O} \times \frac{M - 1}{2 \times M^3}$$

Where Io is the output current, V_O is the output voltage, Ts is the switching period, and M is the voltage conversion ratio (V_O/V_{IN}). At the nominal line condition (15 VDC input) and maximum load (5.0 A), the critical inductance for a 28 VDC output and a switch period of 4.0 μsec is:

$$L_C = \frac{28.4\,\mu}{5} \times \frac{1.867 - 1}{2 \times 1.867^3} \approx 1.5\,\mu H$$

To ensure continuous conduction mode for these operating conditions the inductance is chosen at a value greater than the critical inductance, and for this converter is set at 2.5 μH. Figure 12, shows the value of load current for critical conduction mode operation over the line range.
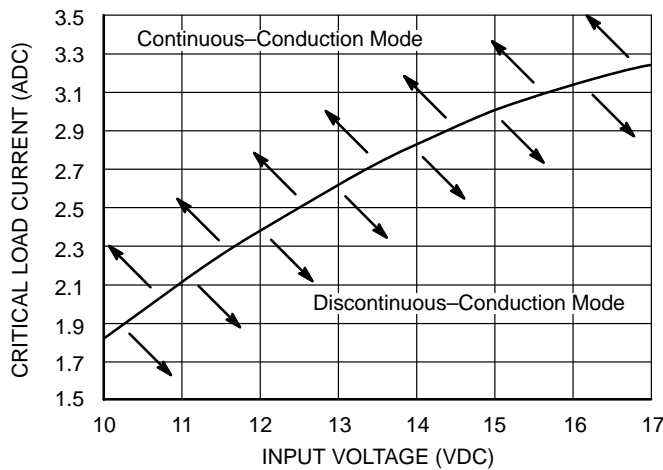
Figure 12. Critical–Conduction Mode Load Current

Component Selection

The main switching element is chosen to handle the worst–case current and voltage stresses. The peak off–state voltage stress on the MOSFET is given as the sum of maximum input voltage and output voltage.

$$V_{DS(max)} = V_{IN(max)} + V_O = 17 + 28 = 45 \text{ V}$$

In CCM mode the current waveform through the switch resembles a ramp on a step (refer to Figure 4). The worst–case peak switch current occurs at low line (10 VDC Input) and maximum load (5.0 A). An expression for the peak and step current in CCM is given as:

$$I_{pk} = I_O \times \left[M + \left(\frac{1}{2 \times \tau_L} \right) \times \left(\frac{M-1}{M^2} \right) \right]$$

$$I_{STEP} = I_O \times \left[M - \left(\frac{1}{2 \times \tau_L} \right) \times \left(\frac{M-1}{M^2} \right) \right]$$

Where τ_L is given as:

$$\tau_L = \frac{I_O \times L}{V_O \times T_S}$$

Substituting values into these expressions yields a worst–case peak current stress in the MOSFET as ~19.2 Apk. The step value of current with these conditions is ~8.9 A. A theoretical switch current waveform for these conditions is shown in Figure 13.
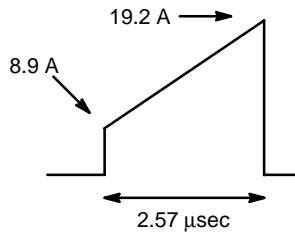
Figure 13. Switch Current Waveform with 10 V Input, 28 V Output @ 5.0 ADC Load

The RMS of the waveform shown in Figure 13 may be expressed in general terms by the following expression:

$$I_{T(rms)} = I_O \times \sqrt{M \times (M-1) + \frac{1}{3} \times \left(\frac{1}{2 \times \tau_L} \right)^2 \times \left(\frac{M-1}{M^2} \right)^3}$$

Substituting values into the RMS current expression above yield a worst–case RMS switch current of ~11.3 A_{RMS}. A MTD60N06 MOSFET having a breakdown voltage rating of 60 V and a continuous drain current rating of 60 A was chosen because it met the operating requirements as well as offer a low on–state resistance ($r_{DS}(on)$) of less than 16 mΩ at a 100°C junction temperature. The worst–case conduction loss of this MOSFET is given as:

$$P_{cond} = I_{T(rms)}^2 \times r_{DS(on)} = 11.3^2 \times 0.016 = 2.04 \text{ W}$$

Figure 14, shows the values of the peak switch current, RMS current, and conduction loss over the input voltage range at maximum load (5.0 A).

The boost diode reverse voltage rating is limited to the output voltage, which in this case is 28 VDC. The diode conducts when the power switch is in the "off" state and provides a current path for the inductor to the output. Similar to the power transistor the worst–case peak current through the diode occurs at low line (10 VDC input) and maximum load (5.0 ADC). The peak current capability of the diode must be at least ~19.2 Apk. The maximum average current through the diode is the same as the maximum output current of the converter (5.0 ADC). Other important considerations in selecting the diode besides its ability to block the required off–state voltage stress and have sufficient peak and average current handling capability, is fast switching characteristics, low reverse–recovery, and low forward voltage drop. In low voltage circuits such as this one, typically the best choice of diodes is a Schottky barrier rectifier. The MBR1645 Schottky diode with a 45 V reverse voltage rating and 16 A continuous current rating was chosen for this application. This device has a forward voltage drop of 0.47 V at 5.0 A continuous current at 125°C junction temperature. The worst–case conduction loss in the Schottky diode is given as:

$$P_D = I_D \times \nu_f = 5 \times 0.47 = 2.35 \text{ W}$$

The output filter capacitor(s) is chosen to meet an output voltage ripple specifications, as well as its ability to handle the required ripple current stress. Two important criteria in selecting a capacitor is its capacitance and equivalent–series–resistance (ESR). The Nichicon PW series capacitors feature low–impedance as well as high ripple current handling capability, which made then ideal choices for this design. An approximate expression for the required capacitance as a function of ripple voltage requirement (ΔV_O), peak inductor current (I_{pk}), boost inductance (L) and input (V_{IN}) and output voltage (V_O) is given as:

$$C_{req} \geq \frac{I_{pk}^2 \times L}{2 \times \Delta V_O \times (V_O - V_{IN})}$$

Where ΔV_O is specified at 50 mV, and the worst case peak current is 19.2 Apk (computed above). Substituting these and other known quantities yields an approximate required capacitance neglecting ESR of:

$$C_{req} \geq \frac{19.2^2 \times 2.5 \text{ μ}}{2 \times 0.05 \times (28 - 10)} = 512 \text{ μF}$$

An expression to compute the required RMS ripple current rating of the output capacitor(s) is given as:

$$I_{C(rms)} = I_O \times \sqrt{(M-1) + \frac{1}{3} \times \left(\frac{1}{2 \times \tau_L} \right)^2 \times \left(\frac{M-1}{M^2} \right)^2 \times \left(\frac{1}{M} \right)}$$
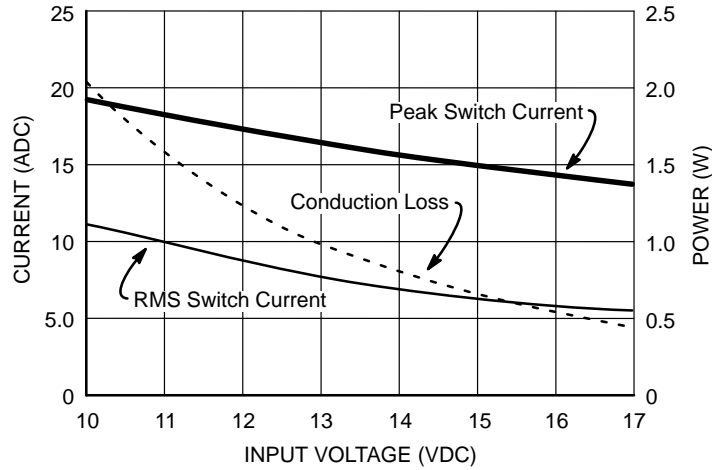
Figure 14. Switch Currents and Conduction Loss

Substituting values in the RMS ripple expression yields a requirement of at least ~7.0 A$_{RMS}$ for the output capacitor. This designs employs six parallel 680 mF/35 V Nichicon PW–series capacitors each individually having a ripple current rating of 1.655 A$_{RMS}$, providing a combined capacitance of 8400 µF and ripple current rating of 9.93 A$_{RMS}$.

Simulation Results

This converter was designed, parameterized and simulated with the use of Power456 from Ridley Engineering which a powerful and dedicated power electronics converter design tool capable of generating time domain plots of the switching waveforms at different operating conditions. The following simulation results (Figures 15–18) were performed at 15 VDC input and 28 VDC output at maximum load of 5.0 ADC.
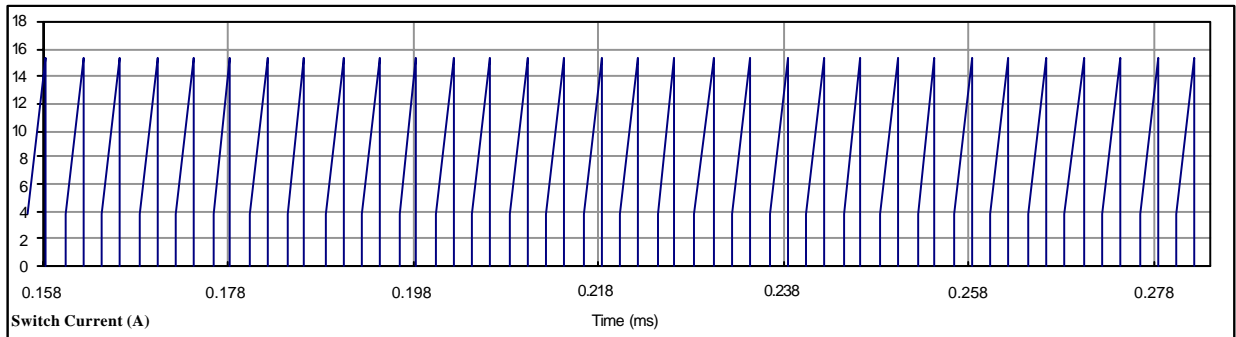
Figure 15.
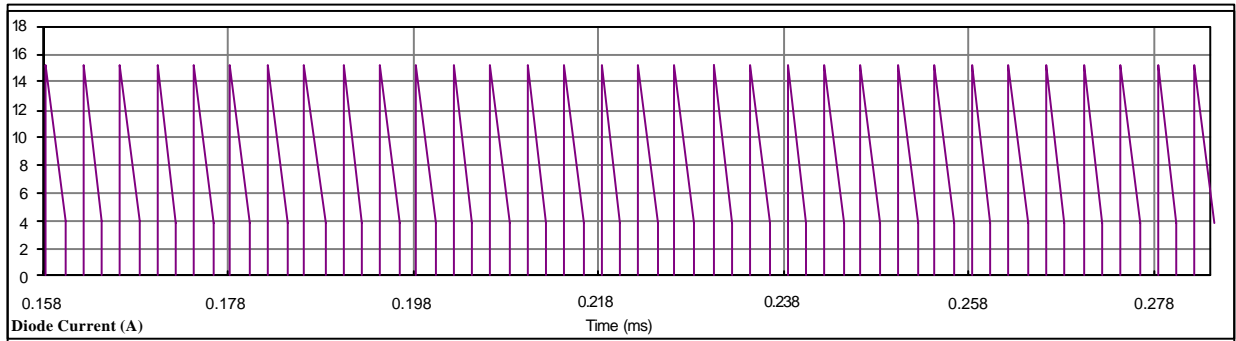
Figure 16.
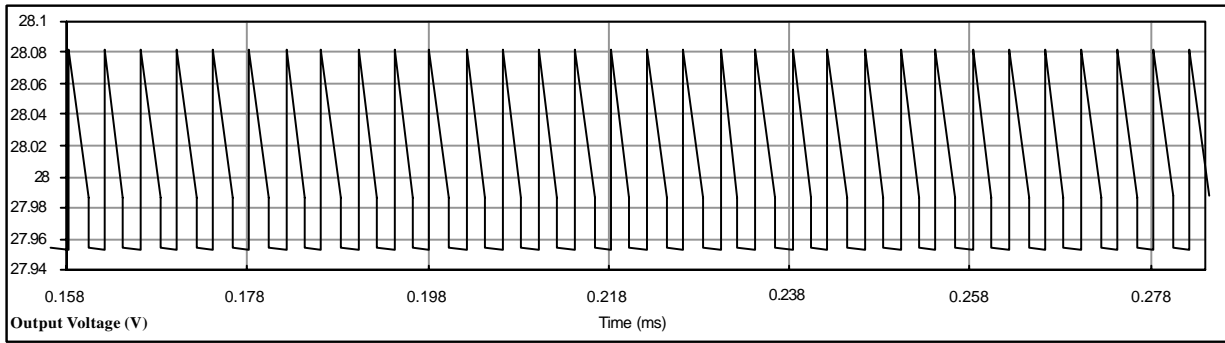
Figure 17.
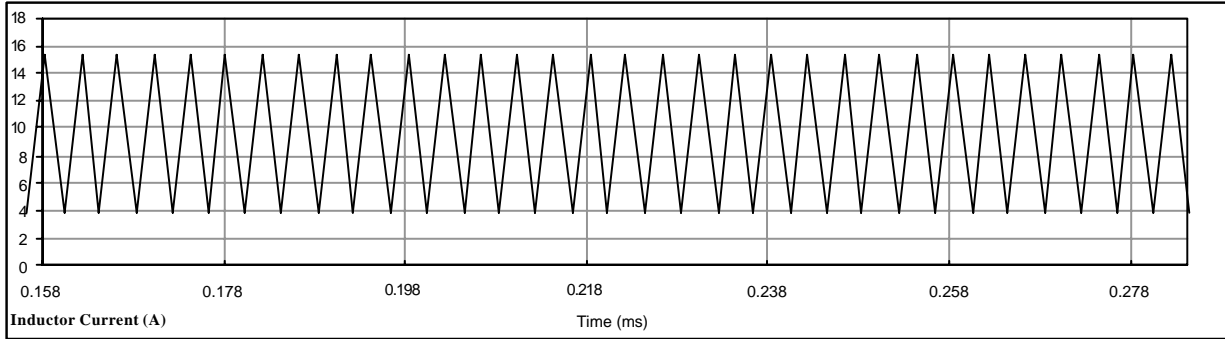
Figure 18.

Loop Compensation/Stability

The power stage model is an essential step in characterizing and optimizing the loop dynamics of the converter. The technique employed in Power456 involves only modeling the switching elements of the power stage, in an equivalent circuit referred to as the PWM switch model, rather than use more laborious techniques like state–space averaging or circuit–averaged models. The key to this model is that it uses of the fact that only the switching elements of the circuit are nonlinear and that the remainder of the circuit consists of linear elements. Linear equivalents of these non–linear elements can be derived by averaging the across voltage and through current of the switching elements in a given switching cycle. The DC and small signal PWM CCM switch model is shown in Figure 19.
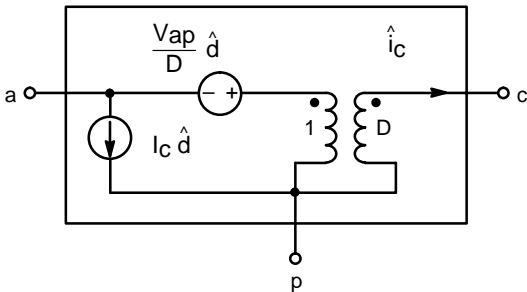
Figure 19. CCM PWM Switch Model

In a boost converter the PWM switch model is inserted into the model in the orientation shown in Figure 20.
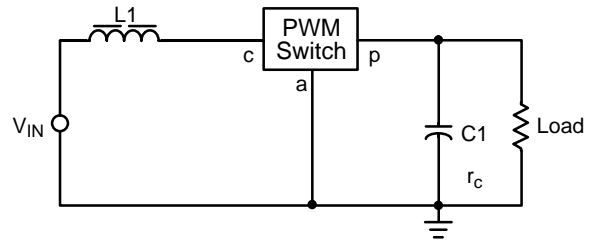
Figure 20. Boost Converter with PWM Switch Model

The model is used to represent the ac behavior of the converter about a given operating point. Linearizing the non–linear converter behavior at a given operating is accomplished using the PWM switch model, which allows optimization of the compensation network to meet stability and line/load transient requirements. The Power456 software tool was used to design the required compensation network and generate the following Bode diagram for the power stage.

The recommended compensator in this design is a type–3 compensator containing 3–poles and 2–zeros. A schematic of this compensator with design values from Power456 and the frequency response of the compensator are shown in Figures 22 and 23, respectively.
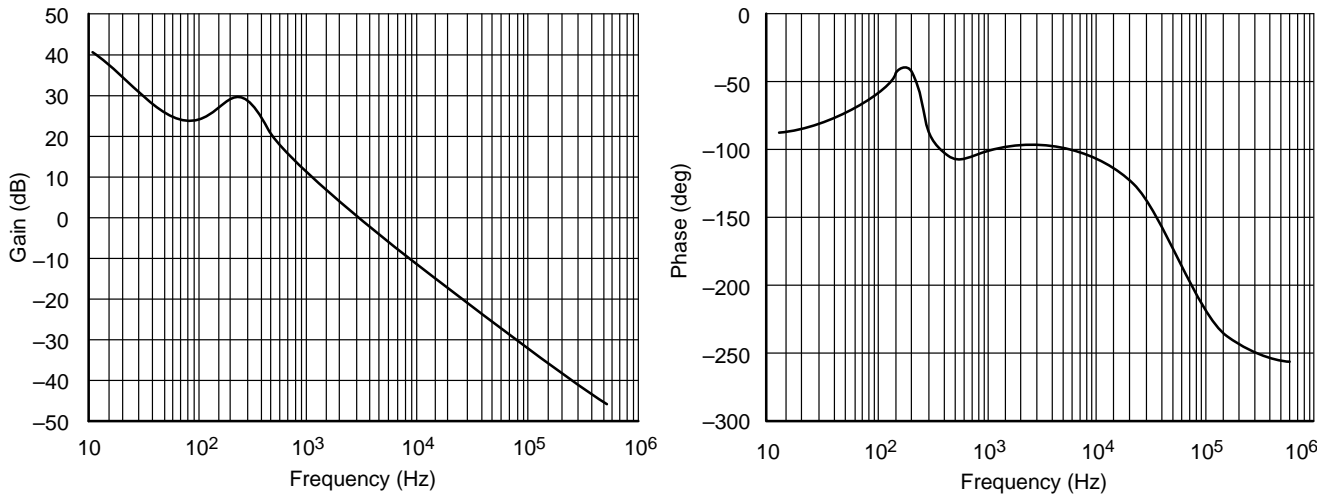
Figure 21. Power Stage Response (V$_{IN}$ = 15 VDC, V$_O$ = 28 VDC @ 5.0 A)
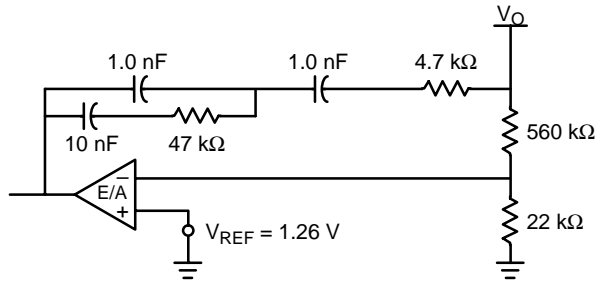
Figure 22. Type–3 Compensator Design
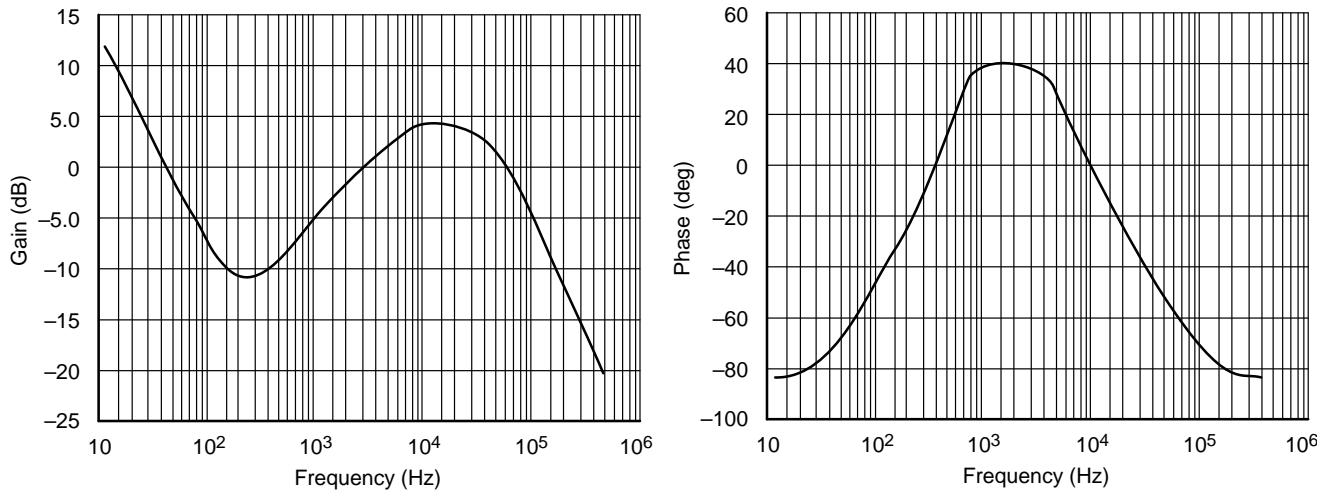
Figure 23. Type–3 Compensator Frequency Response
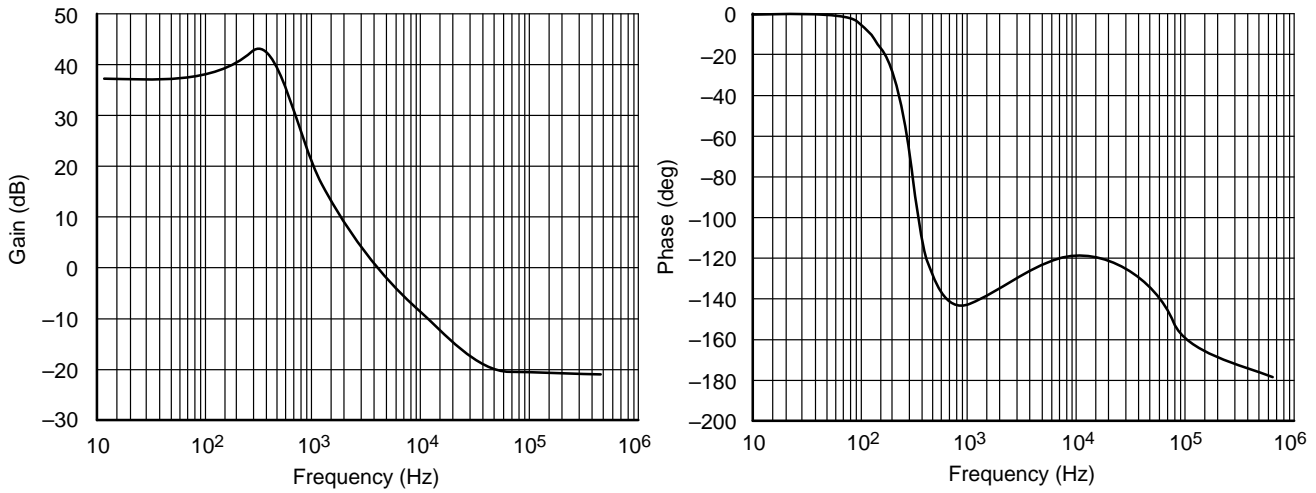
Figure 24. Closed Loop Response (V_{IN} = 15 VDC, V_O = 28 VDC @ 5.0 A)

The composite Loop response using this compensator is shown in Figure 24. It predicts that the converter will have a bandwidth of approximately 40 kHz, a gain margin of greater than 20 dB, and a phase margin of slightly greater than 60 degrees.

Operating Characteristics

The 112 W boost converter was built and tested to evaluate and compare the actual circuit performance to the simulated results of the prior sections. The following sections summarize the measured converter performance over the specified load and line range.

Some important differences between the theoretical design and actual measured performance (due to the use of available components) include the switching frequency, output voltage regulation, and maximum delivered power at low line. The switching frequency of the converter was measured at 227 kHz rather than 250 kHz; this is due to the value of C5 (330 pF). A value of 360 pF would have yielded a switching frequency closer to the target

specification. The regulated output voltage of this converter was 27.4 VDC +/–1%, rather than 28 VDC; this was due to the values of R3 and R4. Standard 5% resistor component values were used throughout the converter; 1–% resistor values would have yielded closer adherence to the target specification. Finally, the maximum delivered power at low line conditions (V_{IN} = 10 VDC) was 82 W. The power limitation was due to the value of R7, which is the peak switch current sense resistor. Since the peak current limit value (~17 ADC) was achieved at low input conditions, the CS51227 naturally limited the delivered power to the output by reducing the output voltage. The effect was visible is the observed converter waveforms.

The converter power efficiency was measured and is depicted on Figure 25. The converter efficiency is defined as the ratio of delivered to input power.

$$\eta = \frac{P_O}{P_{IN}} \times 100\%$$
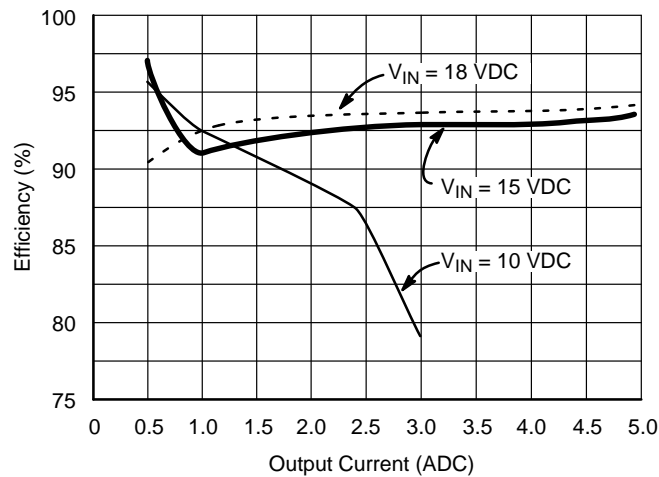
Figure 25. Converter Efficiency
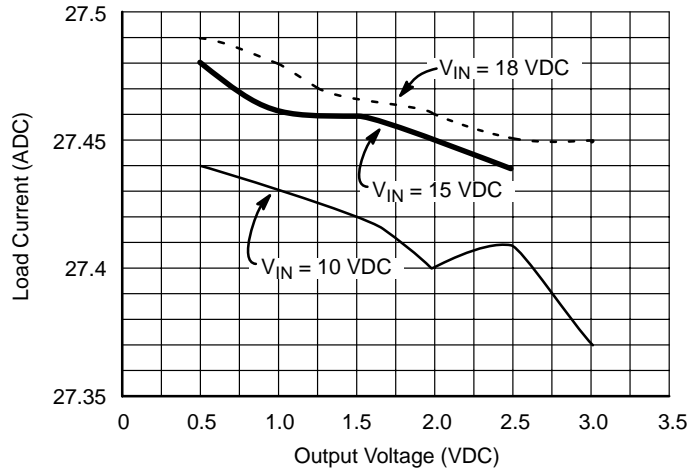
Figure 26. Load/Line Regulation

The previous figure shows that the converter achieves better than 90% conversion efficiency for a majority of the operating range. The efficiency falls dramatically at low line (V_{IN} = 10 VDC) and high load conditions (Io > 2.0 ADC) due to the operating conditions of the converter.

Figure 26, depicts the line/load output voltage regulation of the converter. The following plot shows that the output voltage holds a regulation tolerance of +/– 2% over the specified operating range. Signs of voltage regulation drop–off is evident at low line, high load conditions.

The following oscillographs depict the MOSFET gate–source, inductor current and drain–source voltage of the converter at low, nominal and high line conditions, for minimum and maximum load.
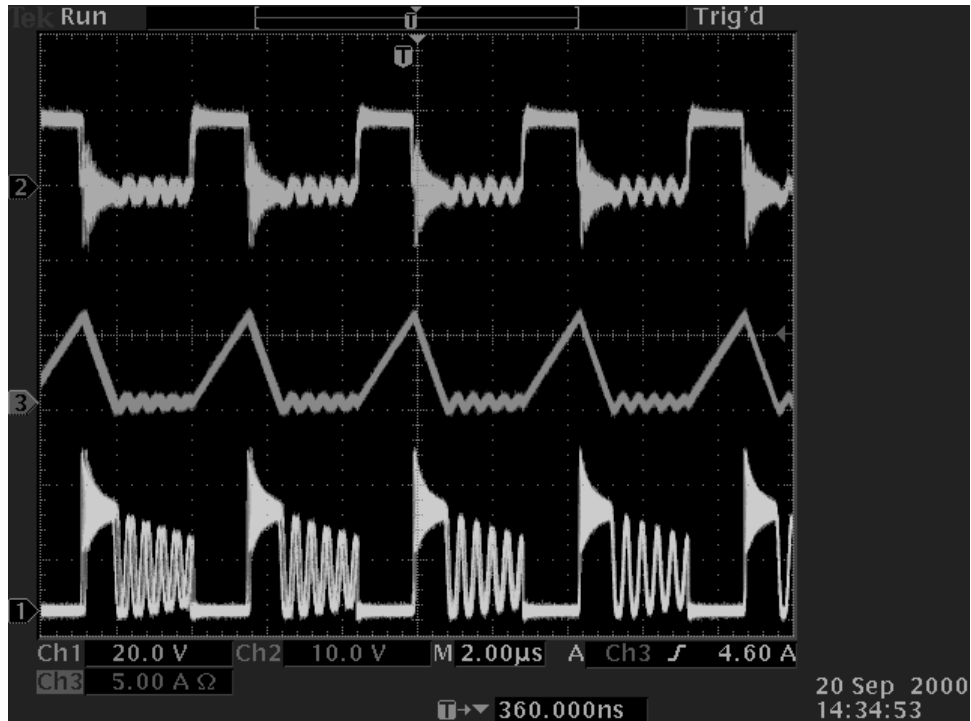
Figure 27. MOSFET V_{GS}, Inductor Current and V_{DS}
V_{IN} = 10 VDC, V_O = 28 VDC, I_o = 0.5 ADC
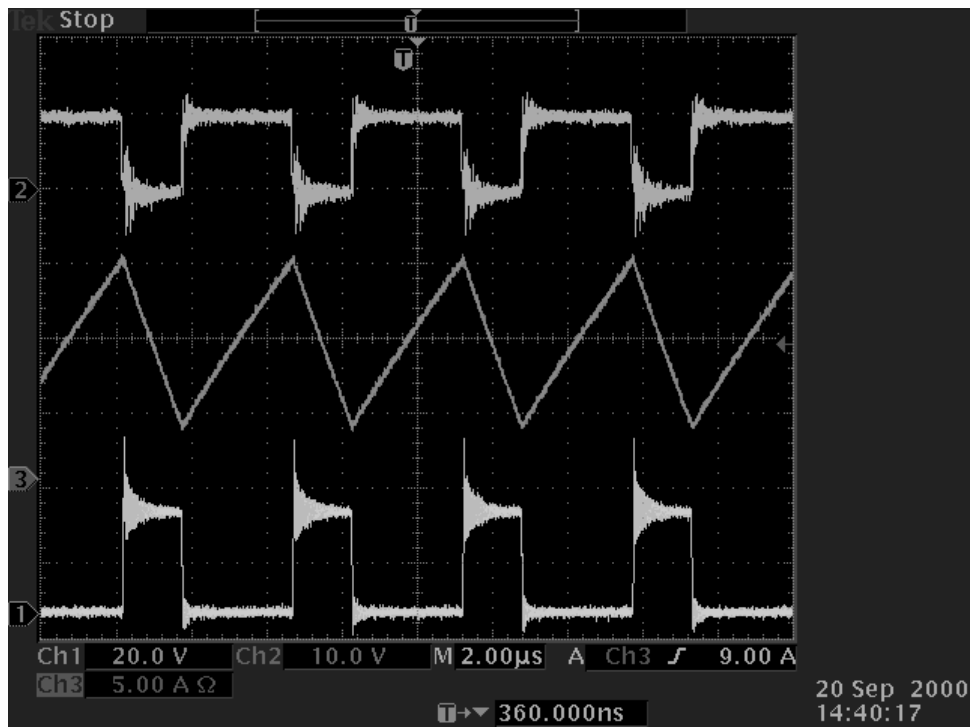
Figure 28. MOSFET V$_{GS}$, Inductor Current and V$_{DS}$
V$_{IN}$ = 10 VDC, V$_O$ = 28 VDC, I$_o$ = 3.0 ADC
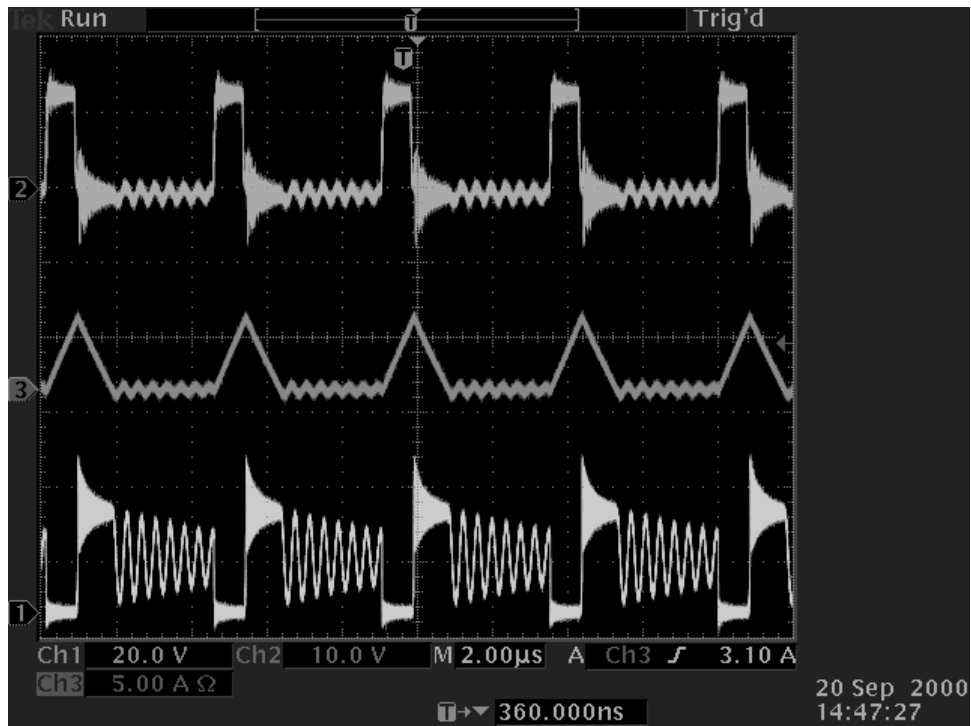
Figure 29. MOSFET V$_{GS}$, Inductor Current and V$_{DS}$
V$_{IN}$ = 15 VDC, V$_O$ = 28 VDC, I$_o$ = 0.5 ADC
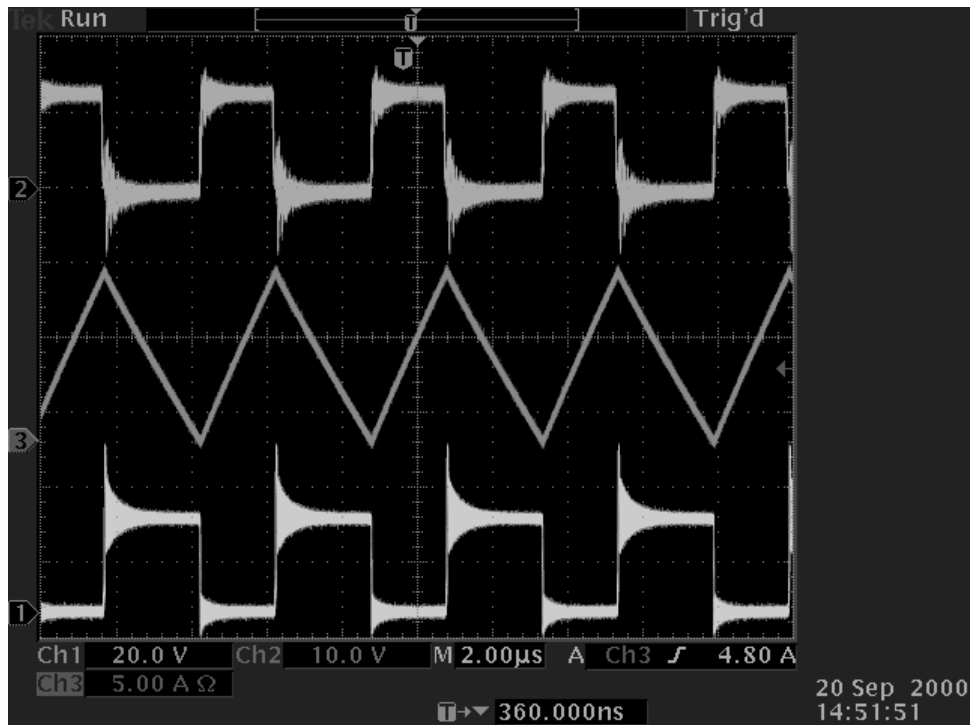
Figure 30. MOSFET V$_{GS}$, Inductor Current and V$_{DS}$
V$_{IN}$ = 15 VDC, V$_O$ = 28 VDC, I$_o$ = 3.0 ADC
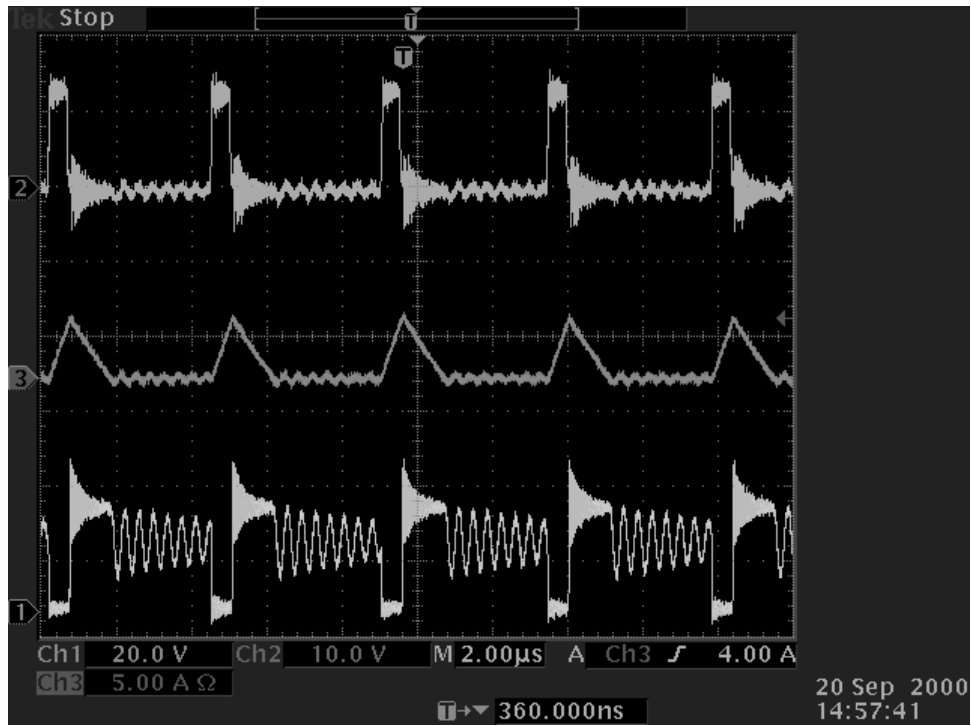
Figure 31. MOSFET V$_{GS}$, Inductor Current and V$_{DS}$
V$_{IN}$ = 18 VDC, V$_O$ = 28 VDC, I$_o$ = 0.5 ADC
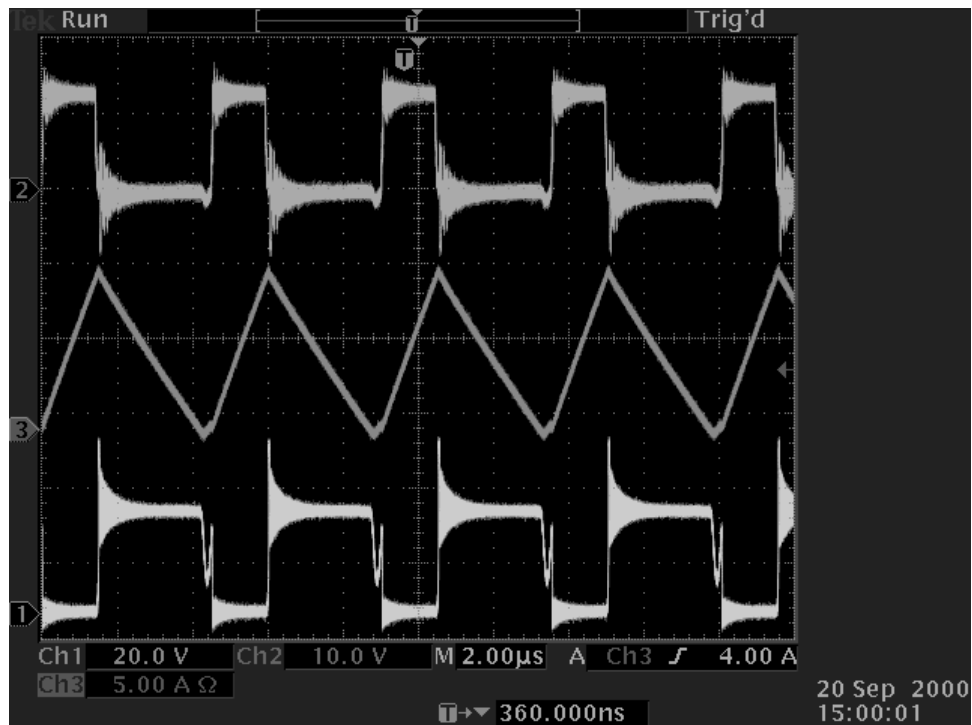
Figure 32. MOSFET V_{GS}, Inductor Current and V_{DS}
V_{IN} = 18 VDC, V_O = 27.5 VDC, I_O = 3.0 ADC

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<u>Notes</u>

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