UNITRODE
APPLICATION NOTE

# PRACTICAL CONSIDERATIONS IN CURRENT MODE POWER SUPPLIES

## Introduction

This detailed section contains an in-depth explanation of the numerous PWM functions, and how to maximize their usefulness. It covers a multitude of practical circuit design considerations, such as slope compensation, gate drive circuitry, external control functions, synchronization, and paralleling current mode controlled modules. Circuit diagrams and simplified equations for the above items of interest are included. Familiarity with these topics will simplify the design and debugging process, and will save a great deal of time for the power supply design engineer.

## I. SLOPE COMPENSATION

Current mode control regulates the PEAK inductor current via the 'inner' or current control loop. In a continuous mode (buck) converter, however, the output current is the AVERAGE inductor current, composed of both an AC and DC component.

While in regulation, the power supply output voltage and inductance are constant. Therefore, $V_{OUT} / L_{SEC}$ and dI/dT, the secondary ripple current, is also constant. In a constant volt-second system, dT varies as a function of $V_{IN}$, the basis of pulse width modulation. The AC ripple current component, dI, varies also as a function of dT in accordance with the constant $V_{OUT} L_{SEC}$.

### Average Current

At high values of $V_{IN}$, the AC current in both the primary and the secondary is at its maximum. This is represented graphically by duty cycle D1, the corresponding average current II, and the ripple current d(I1). As $V_{IN}$ decreases to its minimum at duty cycle, the ripple current also is at its minimum amplitude. This occurs at duty cycle D2 of average current I2 and ripple current d(I2). Regulating the peak primary current (current mode control) will produce different AVERAGE output currents I1, and I2 for duty cycles D1 and D2. The average current INCREASES with duty cycle when the peak current is compared to a fixed error voltage.

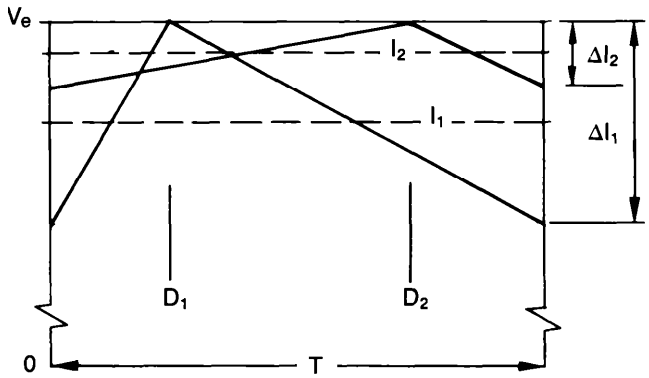



**Figure 1. Average Current Error**

### Constant Output Current

To maintain a constant AVERAGE current, independent of duty cycle, a compensating ramp is required. Lowering the error voltage precisely as a function of $T_{ON}$ will terminate the pulse width sooner. This narrows the duty cycle creating a CONSTANT output current independent of $T_{ON}$, or $V_{IN}$. This ramp simply compensates for the peak to average current differences as a function of duty cycle. Output currents I1 and I2 are now identical for duty cycles D1 and D2.

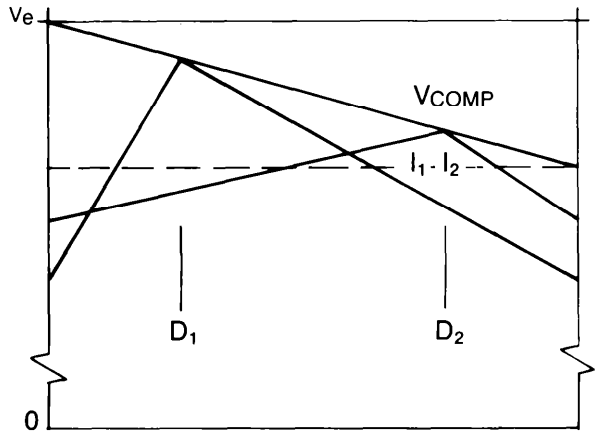



**Figure 2. Constant Average Current**

### Determining the Ramp Slope

Mathematically, the slope of this compensating ramp must be equal to one-half (50%) the downslope of the output inductor as seen from the control side of the circuit. This is proven in detail in "Modelling, Analysis and Compensating of the Current Mode Controller," (Unitrode publication U-97 and its references). Empirically, slightly higher values of slope compensation (75%) can be used where the AC component is small in comparison to the DC pedestal, typical of a continuous converter

### Circuit Implementation

In a current mode control PWM IC, the error voltage is generated at the output of the error amplifier and compared to the primary current at the PWM comparator At this node, subtracting the compensating ramp from the error voltage, or adding it to the primary current sense input will have the same effect: to decrease the pulse width as a function of duty cycle (time). It is more convenient to add the slope compensating ramp to the current input. A portion of the oscillator waveform available at the timing capacitor ($C_T$) will be resistively summed with the primary current. This is entered to the PWM comparator at the current sense input.

**Parameters Required for Slope Compensation Calculations**

Slope compensation can be calculated after specific parameters of the circuit are defined and calculated.

| SECTION | PARAMETER |
|---|---|
| Control | T on (Max) Oscillator<br>ΔV Oscillator (PK-PK Ramp Amplitude)<br>I Sense Threshold (Max) |
| Output | V Secondary (Min)<br>L output<br>I AC Secondary<br>(Secondary Ripple Current) |
| General | R Sense (Current Sensing Resistor)<br>M (Amount of Slope Compensation)<br>N Turns Ratio ($N_P / N_S$) |

Once obtained, the calculations for slope compensation are straightforward, using the following equations and diagrams.

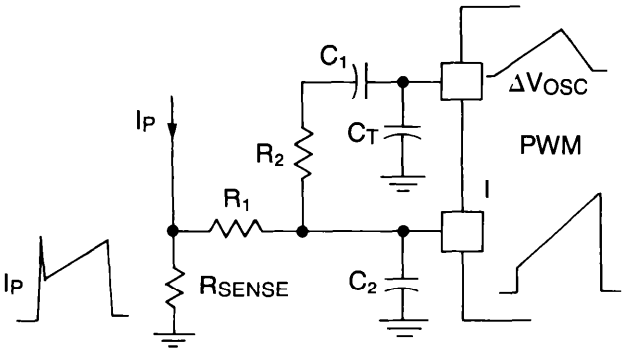



**Figure 3. General Circuit**

Resistors R1 and R2 form a voltage divider from the oscillator output to the current limit input, superimposing the slope compensation on the primary current waveform. Capacitor C1 is an AC coupling capacitor, and allows the AC voltage swing of the oscillator to be used without adding offset circuitry. Capacitor C2 forms an R-C filter with R1 to suppress the leading edge glitch of the primary current wave. The ratio of resistor R2 to R1 will determine the exact amount of slope compensation added.

For purposes of determining the resistor values, capacitors $C_T$ (timing), C1 (coupling), and C2 (filtering) can be removed from the circuit schematic. The oscillator voltage ($V_{OSC}$) is the peak-to-peak amplitude of the sawtooth waveform. The simplified model is represented schematically in the following circuit.

These calculations can be applied to all current mode converters using a similar slope compensating scheme.

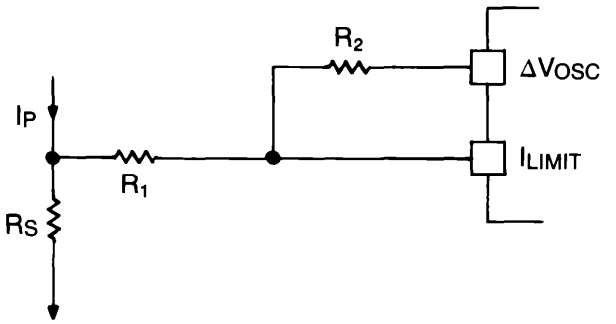



**Figure 4. Simplified Circuit**

Step 1. Calculate the Inductor Downslope

$S(L) = di/dt = V_{SEC}/L_{SEC}$ (Amps/Second)

Step 2. Calculate the Reflected Downslope to the Primary

$S(L)' = S(L)/N$ (Amps/Second)

Step 3. Calculate Equivalent Downslope Ramp

$V\,S(L)' = S(L)' \bullet R\ sense$ (Volts/Second)

Step 4. Calculate the Oscillator Charge Slope

$V\,S_{(OSC)} = d(V_{OSC}) / T\,on$ (Volts/Second)

Step 5. Generate the Ramp Equations

Using superposition, the circuit can be illustrated as:

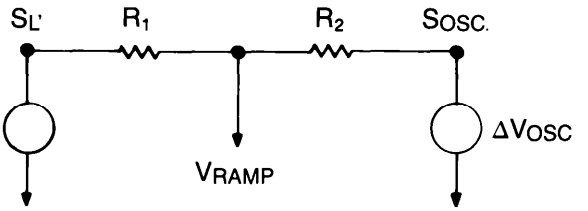



**Figure 5. Superposition**

$$V_{(RAMP)} = \frac{V\,S(L)' \bullet R2}{R1 + R2} + \frac{V\,S_{(OSC)} \bullet R1}{R1 + R2} \quad \text{simplifying,}$$

$$V_{(RAMP)} = V\,S(L)'' + V\,S_{(COMP)} \quad \text{where}$$

$$V\,S_{(COMP)} = \frac{V\,S_{(OSC)} \bullet R1}{R1 + R2}\text{, and } V\,S(L)'' = \frac{V\,S(L)' \bullet R2}{R1 + R2}$$

Step 6. Calculate Slope Compensation

$V\,S(COMP) = M \bullet S(L)''$ where M is the amount of inductor downslope to be introduced.

$$\text{Equating } \frac{V\,S_{(OSC)} \bullet R1}{R1 + R2} = \frac{M \bullet V\,S(L)' \bullet R2}{R1 + R2}$$

, solving for R2

$$R2 = R1 \bullet \frac{V\,S_{(OSC)}}{V\,S(L)' \bullet M}$$

Equating R1 to 1K ohm simplifies the above calculation and selection of capacitor C2 for filtering the leading edge glitch. Using the closest standard value to the calculated value of R2 will minimally effect the exact amount of down-slope introduced. It is important that R2 be high enough in resistance not to load down the I.C. oscillator, thus causing a frequency shift due to the slope compensation ramp to R2.

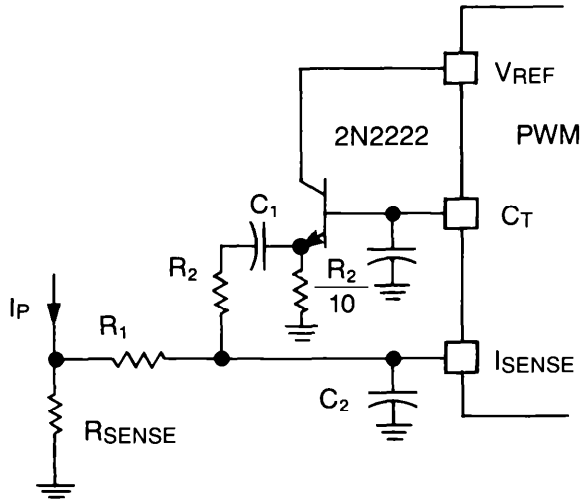



**Figure 6. Emitter Follower Circuit**

Design Example — Slope Compensation Calculations

Circuit Description and Parameter Listing:

Topology: Half-Bridge Converter
Input Voltage: 85-132 VAC "Doubler Configuration"
Output: 5 VDC/45 ADC
Frequency: 200 KHz, T Period = 5.0 µS
T Deadtime: 500 ns, T on Max = 4.5 µS
Turns Ratio: 15/1, (Np/Ns)
V Primary: 90 VDC Min, 186 Max
V Sec Min: 6 VDC
R Sense: 0.25 Ohm
I Sec Ac: 3.0 Amps (<l0% I DC)
L Output: 5.16 µh

1. Calculate the Inductor Downslope on the Secondary Side

$S(L) = di/dt = V_{SEC}/L_{SEC}$ = 6 v/5.16 µh = 1.16 A/$\mu$s

2. Calculate the Transformed Inductor Slope to the Primary Side

S (L)' = S (L) • Ns/Np = 1.16 • 1/15 = 0.0775 A/µS

3. Calculate the Transformed Slope Voltage at Sense Resistor

V S(L)' = S (L)' • Rsense = 7.72 • $1O^{-2}$ • 0.250 = $1.94 \bullet 10^{-2}$ V/$\mu$S

4. Calculate the Oscillator Slope at the Timing Capacitor

$S_{(OSC)}$ = d V osc/T on max = 1.8/4.5 = 0.400 V/µS

5. Let Amount of Slope Compensation (M) = 0.75 and R1 = 1K

$$R2 = R1 \bullet \frac{V\,S_{(OSC)}}{V\,S(L)' \bullet M} \quad ; R2 = \frac{1\,K \bullet 0.400}{0.0192 \bullet 0.75}$$

= 27.4 K ohms

## II. GATE DRIVE CIRCUITRY

The high current totem-pole outputs of most PWM ICs have greatly enhanced and simplified MOSFET gate drive circuits. Fast switching times of the high power FETs can be attained with nearly a "direct" drive from the PWM. Frequently overlooked, only two external components — a resistor and Schottky diode are required to insure proper operation of the PWM while delivering the high current drive pulses.

### MOSFET Input Impedance

Typical gate-to-source input characteristics of most FETs reveal approximately 1500 picofarads of capacitance in series with 15 nanohenries of source inductance. For this example, the series gate current limiting resistor will not be used to exemplify its necessity. Also, the totem pole transistors are replaced with ideal (lossless) switches. A dV/dT rate of 0.5 volts per nanosecond is typical for most high speed PWMs and will be incorporated.

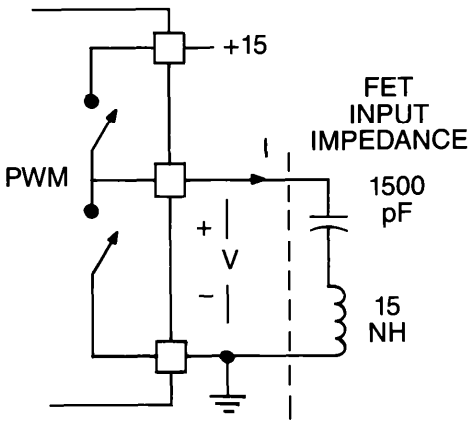



**Figure 7. Ideal Circuit Gate Drive**

Assuming no external circuit parasitics of R, L or C, the PWM is therefore driving an L-C resonant tank with no attenuation. The driving function is a 15 volt pulse derived from the auxiliary supply voltage. The resulting current waveform is shown in figure 8, having a peak current of approximately seven amps at a frequency of thirty-three megahertz.

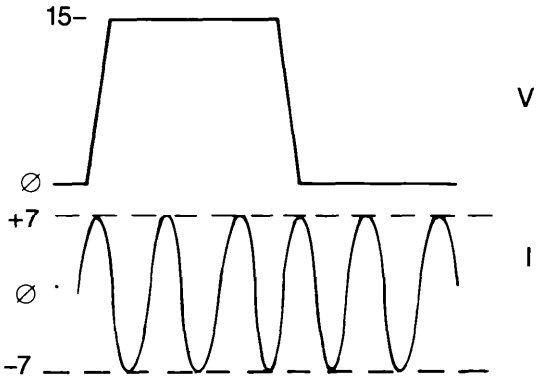



**Figure 8. Voltage & Current Waveforms at Gate**

In a practical application, the transistors and other circuit parameters, fortunately, are less than ideal. The results above are unlikely to happen in most designs, however they will occur at a reduced magnitude if not prevented.

Limiting the peak current through the IC is accomplished by placing a resistor between the totem-pole output and the gate of the MOSFET. The value is determined by dividing the totem-pole collector voltage ($V_C$) by the peak current rating of the IC's totem-pole. Without this resistor, the peak current is limited only by the dV/dT rate of the totem-pole and the FET gate capacitance.

For this example, a collector supply voltage of 10 volts is used, with an estimated totem-pole saturation voltage of approximately 2 volts. Limiting the peak gate current to 1.5 amps max requires a resistor of six ohms, and the nearest standard value of 6.2 ohms was used. Locating the resistor in series with the collector to the auxiliary voltage source will only limit the turn-on current. Therefore it must be placed between the PWM and gate to limit both turn-on and turn-off currents.

Actual circuit parasitics also play a key role in the drive behavior. The inductance of the FET source lead (15 nanohenries typical) is generally small in comparison to the layout inductance. To model this network, an approximation of 30 nanohenries per inch of PC trace can be used. In addition, the inductance between the pins of the IC and the die can be rounded off to 10 nanohenries per pin. It now becomes apparent that circuit inductances can quickly add up to 100 nanohenries, even with the best of PC layouts. For this example, an estimate of 60 nh was used to simulate the demonstration PC board. The equivalent circuit is shown in figure 10. A 10 volt pulse is applied to the network using 6.2 ohms as the current limiting resistance. Displayed is the resulting voltage and current waveform at the totem-pole output.

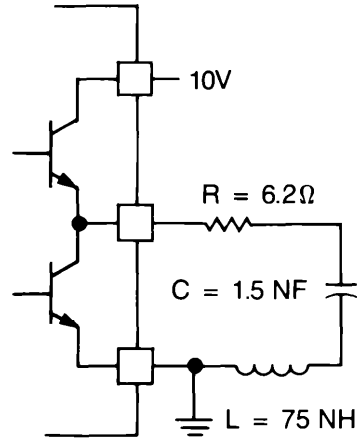



**Figure 9. Circuit Parameters**

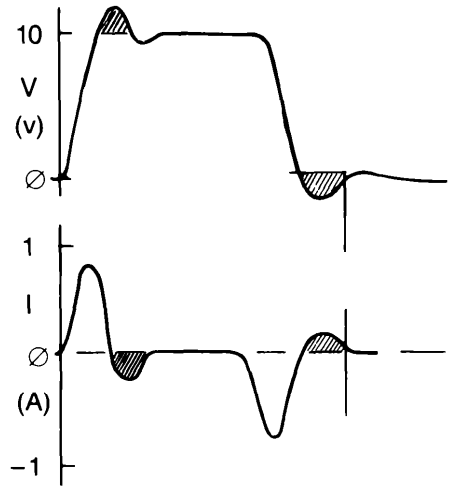



**Figure 10. Circuit Response**

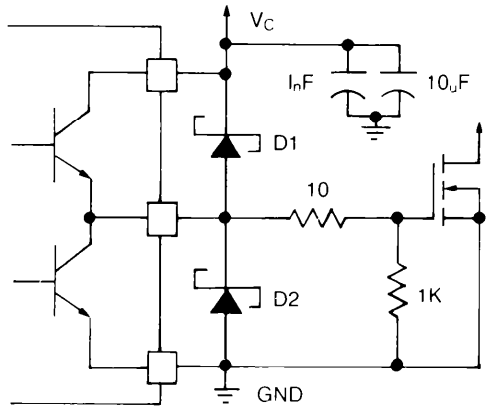
The shaded areas of each graph are of particular interest. During this time, the lower totem-pole transistor is saturated. The voltage at its collector is negative with respect to it's emitter (ground). In addition, a positive output current is being supplied to the RLC network thru this saturated NPN transistor's collector. The IC specifications indicate that neither of these two conditions are tolerable individually, nevermind simultaneously. One approach is to increase the limiting resistance to change the response from underdamped to slightly overdamped. This will occur when:

$$R\ (\text{gate}) \geq 2 \bullet \sqrt{L/C}$$

Unfortunately, this also reduces the peak drive current, thus increasing the switching times of the FETS - highly undesirable. The alternate solution is to limit the peak current, and alter the circuit to accept the underdamped network.

The use of a Schottky diode from the PWM output to ground will correct both situations. Connected with the anode to ground and cathode to the output, it will prevent the output voltage from going excessively below ground, and will also provide a current path. To be effective, the diode selected should have a forward voltage drop of less than 0.3 volts at 200 milliamps. Most 1-to-3 amp diodes exhibit these traits above room temperature. The diode will conduct during the shaded part of the curve shown in figure 10 when the voltage goes negative and the current is positive. The current is allowed to circulate without adversely effecting the IC performance. Placing the diode as physically close to the PWM as possible will enhance circuit performance. Circuit implementation of the complete drive scheme is shown in the schematic.

**Power MOSFET Drive Circuit**

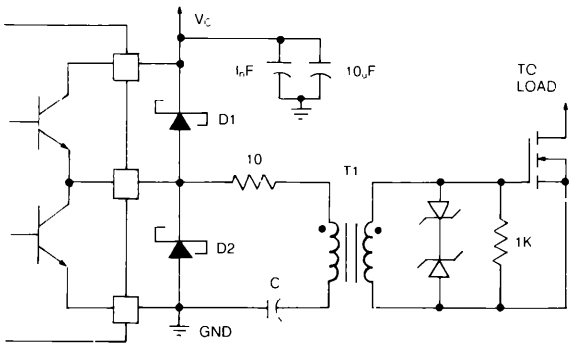



D1.D2: UC3611 Schottky Diodes

**Figure 11.**

Transformer driven circuits also require the use of the Schottky diodes to prevent a similar set of circumstances from occurring on the PWM outputs. The ringing below ground is greatly enhanced by the transformer leakage inductance and parasitic capacitance, in addition to the magnetizing inductance and FET gate capacitance. Circuit implementation is similar to the previous example.

**Transformer Coupled MOSFET Drive Circuit**




D1 .D2: UC3611 Schottky Diode Array

**Figure 12.**

**Transformer Coupled Push-Pull MOSFET Drive Circuit**

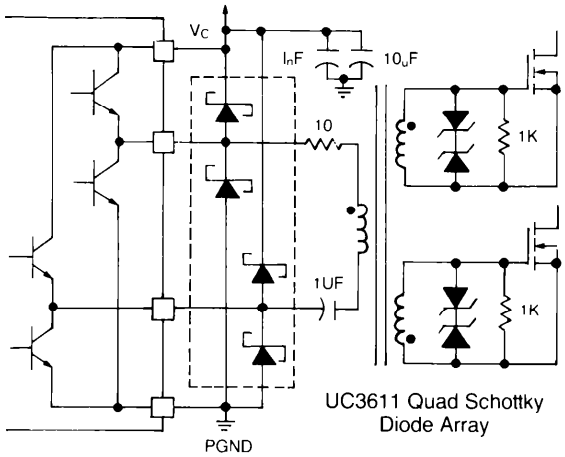



**Figure 13.**

**Peak Gate Current and Rise Time Calculations**

Several changes occur at the MOSFET gate during the turn-on period. As the gate threshold voltage is reached, the effective gate input capacitance goes up by about fifteen percent, and as the drain current flows, the capacitance will double. The gate-to-source voltage remains fairly constant while the drain voltage is decreasing. The peak gate current required to switch the MOSFET during a specified turn-on time can be approximated with the following equation.

$$I\,pk = \frac{2}{Ton}\left\{ Ciss\left[ (2.5 \bullet Vgth) + \frac{Id}{gm} \right] + [Crss\,(VDD - Vgth)] \right\}$$

Several generalizations can be applied to simplify this equation. First, let Vgth, the gate turn-on threshold, equal 3 volts. Also, assume gm equals the drain current Id divided by the change in gate threshold voltage, dVgth. For most applications, dVgth is approximately 2.5 volts for utilization of the FET at 75% of its maximum current rating. In most off-line power supplies, the gate threshold voltage is a small percentage of the drain voltage and can be eliminated from the last part of the equation. The formulas to determine peak drive current and turn-on time using the FET parameters now simplify to:

$$I\,pk = \frac{2}{Ton} \bullet \{ (10 \bullet Ciss) + (Crss \bullet V\,drain) \}$$

$$Ton = \frac{2}{I\,pk} \bullet \{ (10 \bullet Ciss) + (Crss \bullet Vdrain) \}$$

Switching times in the order of 50 nanoseconds are attainable with a peak gate current of approximately 1 .0 amps in many practical designs. Higher drive currents are obtainable using most Unitrode current mode PWMs which can source and sink up to 1.5 amps peak (UC1825). Driver ICs with similar output totem poles (UC1707) are recommended for paralleled MOSFET high speed applications. SEE APPLICATION NOTE U-118

## III. SYNCHRONIZATION

Power supplies have historically been thought of as "black boxes," an off-the-shelf commodity by most end users. Their primary function is to generate a precise voltage, independent of load current or input voltage variations, at the lowest possible cost. In addition, end users allocate a minimal amount of system real estate in which it must fit. The major task facing design engineers is to overcome these constraints while exceeding the customers' expectations, attaining high power densities and avoiding thermal management problems. It is imperative, too, that the power supply harmonize and integrate with the system rather than cause catastrophic noise problems and last minute headaches. Products that had performed to satisfaction on the lab workbench powered by well filtered linear supplies may not fare as well when driven by a noisy switcher enclosed in a small cabinet.

Basic power supply design criteria such as the switching frequency may be designated by the system clock or CPU and thus may not be up to the power supply designer's discretion. This immediately impacts the physical size of the magnetic components, hence overall supply size, and may result in less-than-optimum power density. However, for the system to function properly, the power supply must be synchronized to the system clock.

There are numerous other reasons for synchronizing the power supply to the system. Most switching power noise has a high peak-to-average ratio of short duration, generally referred to as a spike. Common mode noise generated by these pulsating currents through stray capacitance may be difficult (if not impossible) to completely eliminate after the system design is complete. Ground loop noise may also be amplified due to the interaction of changing currents through parasitic inductances, resulting in crosstalk through the system. EMI filtering to the main input line is much simpler and more repeatable when power is processed at a fixed frequency.

In addition, multiple power stages require synchronization to reduce the differential noise generated between modules at turn-on. In unison, the converters begin their cycles at the same time, each contributing to common mode noise simultaneously, rather than randomly. This also simplifies peak power considerations and will result in predictable power distribution and losses. Compensation made for voltage drops along the bus bars, produced by both the AC and DC power current components, can be accomplished. Balancing of the loads and power bus losses also contributes to diminishing the differential noise and should be administered for optimum results.

### Operation of the PWM Oscillator

In normal operation, the timing capacitor (Ct) is linearly charged and discharged between two thresholds, the upper and lower comparator thresholds. The charging current is determined by means of a fixed voltage across a user selected timing resistance (Rt). The resulting current is then mirrored internally to the timing capacitor Ct at the IC's Ct output. The discharge current is internally set in most PWM designs.

As Ct begins its charge cycle, the outputs of the PWM are initiated and turn on. The timing capacitor charges, and when its amplitude equals that of the error amplifier output, the PWM output is terminated and the outputs turn off. Ct continues to charge until it reaches the upper threshold of the timing comparator Once intersected, the discharge circuitry activates and discharges Ct until the timing comparator lower threshold is reached. During this discharge time, the PWM outputs are disabled, thus insuring a "dead" time when each output is off.

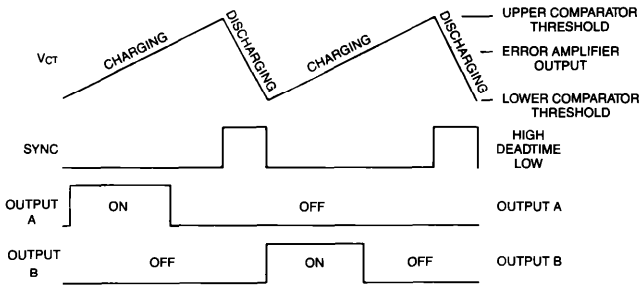



**Figure 14. Voltage Mode Control – Normal Operation**

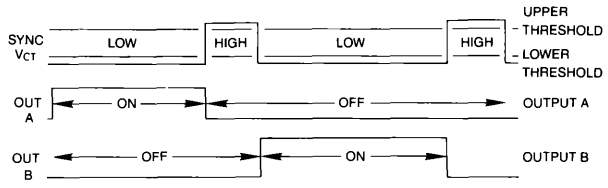



**Figure 15.**

The SYNC terminal provides a "digital" representation of the oscillator charge/discharge status and can be utilized as both an input or an output on most PWM's. In instances where no synchronization port is easily available, the timing circuitry (Ct) can be driven from a digital (0V, 5V) logic input rather than in the analog mode. The primary considerations of on-time, off-time, duty cycle and frequency can be encompassed in the digital pulse train. A LOW logic level input determines the PWM ON time. Conversely, a HIGH input governs the OFF time, or dead time. Critical constraints of frequency, duty cycle or dead time can be accurately controlled by a digital signal to the PWM timing cap (Ct) input. The command can be executed by anything from a simple 555 timer, to an elaborate microprocessor software controlled routine.

Not all PWM IC's have a direct synchronization input/output connection available to the internal oscillator In these applications, the slave oscillator must be disabled and driven in a different fashion. This approach may also be required when using different PWMs amongst the slave modules with different sync characteristics, or anti-phase signals.

Unfortunately, there are several drawbacks to this method, depending on the implementation. First, the PWM error amplifier has no control over the pulse width in voltage mode control. The error amplifier output is compared to a digital signal instead of a sawtooth ramp, rendering its attempts fruitless. The conventional soft start technique of clamping the error amp output, thereby clamping the duty cycle will not function. With no local timing ramp available, the supply is completely under the direction of the sync pulse source. Should the pulse become latched or removed, the PWM outputs will either stay fully on, or fully off, depending on the sync level input (voltage mode). Also, without the local Ct ramp, the supply will not self-start, remaining off until the sync stream appears. Slope compensation for current mode controlled units requires additional components to generate the compensating ramp. Every supply must be produced as a dedicated master, or slave, and must be non-interchangeable with one another, barring modification. This is only a brief list of the numerous design drawbacks to this "open-ended" sync operation. To circumvent these shortcomings, a universal sync circuit has been developed with the following performance features and benefits:

- Sync any PWM to/from any other PWM
- Sync any PWM to/from any number of other PWMs
- Sync from digital levels for simple system integration
- Bidirectional sync signal
- Any PWM can be master or slave with no modifications
- Each control circuit will start and run independently of sync if sync signal is not present
- Localized ramp at Ct for slope compensation
- No critical frequency settings on each module
- High speed - minimum delays
- High noise immunity
- Low power requirements
- Remote off capability
- Minimal effect on frequency, duty cycle, and dead time
- Low cost and component count
- Small size

**Sync Circuit Operating Principles**

These optimal objectives can be obtained using a combination of both analog and digital signal inputs. The timing capacitor Ct input will be used as a summing junction for the analog sawtooth and digital sync input. The PWM is allowed to run independently using its own Rt and Ct components in standard configuration. When synchronization is required, a digital sync pulse will be superimposed on the Ct waveform.

When applied, the sync pulse quickly raises the voltage at Ct above the PWM comparator upper threshold. This forces a change in the oscillator charge/discharge status and operation. The oscillator then begins its normal discharge cycle synchronized to the sync signal. This digital sync pulse simply adds to the analog Ct waveform, forcing the Ct input voltage above the comparator upper threshold.

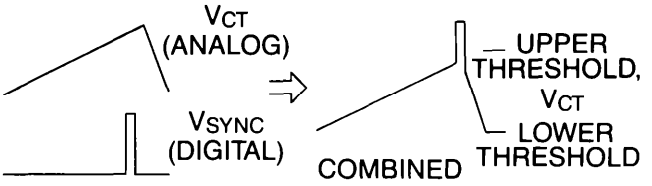



**Figure 16.**

In practice, this approach is best implemented by bringing Ct to ground through a small resistance, about 24 ohms. This low value was selected to have minimal offset and effects on the initial oscillator frequency. The sync pulse will be applied across the 24 ohm resistor Since all PWMs utilize the timing capacitor in their oscillator section, it is both a convenient and universal node to work with.

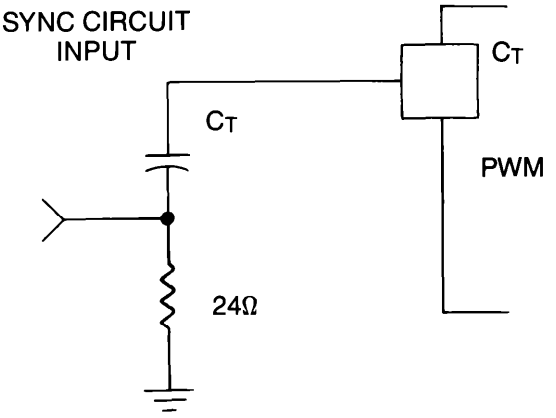



**Figure 17. Sync Circuit Implementation**

**Oscillator Timing Equations**

The oscillator timing components must be first selected to guarantee synchronization to the sync pulse. The sawtooth amplitude must be lower than the upper threshold voltage at the desired sync frequency. If not, the oscillator will run in its normal mode and cross the upper threshold first, before the sync pulse. This requirement dictates that the PWM oscillator frequency must be lower than the sync pulse frequency to trigger reliably. Typically, a ten percent reduction in free running frequency can be accommodated throughout the power supply. Adding the sync circuit will have minor effects on the PWM duty cycle, deadtime and ramp amplitude. (These will be examined in detail .)

### The Timing Ramp

As mentioned, the timing ramp amplitude needs to be approximately ten percent lower in frequency than normal. Therefore, the MINIMUM sync pulse amplitude must fill the remaining ten percent of the peak-to-peak ramp amplitude to reach the upper threshold. Synchronization can be insured over a wide range of frequency inputs and component tolerances by supplying a slightly higher amplitude sync pulse.

Lowering the peak-to-peak charging amplitude also lowers the peak-to-peak discharge amplitude. This shortens the time required to discharge Ct since it begins at a lower potential. Consequently, this reduces the deadtime accordingly. However, the sync pulse width adds to the IC generated deadtime and increases the effective off, or deadtime due to discharge. This sync pulse width need only be wide enough to be sensed by the IC comparator, which is fairly fast. Additional sync pulse width increases deadtime which can be used to compensate for the 10% lower ramp, hence deadtime.

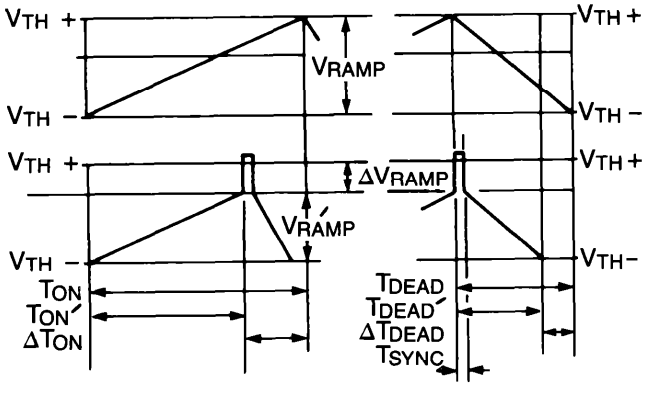



**Figure 18. Oscillator Ramp Relationships**

### Oscillator Ramp Equations

The timing components required in the oscillator section are generally determined graphically from the manufacturers' data sheets for frequency and deadtime versus Rt and Ct. While fine for most applications, a careful examination of the equations is necessary to analyze the impacts of the additional sync circuit components on the timing relationships.

### Oscillator Charging Ramp Equations

$$\Delta V\,osc = \frac{1}{Ct}\left( I\,chg\,dT = \frac{I\,chg}{Ct}\right]_{0}^{t} \quad T$$

$$T\,chg = \{\,\Delta V\,osc \bullet Ct\,\} / Ichg \quad \text{where } Ichg = Vchg / Rt$$

$$\Delta V\,osc = Vth\ upper - Vth\ lower$$

$$\Delta V\,osc' = \Delta V\,osc \frac{(tchg')}{t\,chg(o)} - V\ (24\ ohm)$$

$$V\ (24\ ohm) = I\,chg \bullet 24 = [Vchg / Rt] \bullet 24$$

These equations can be reduced if an approximation is made that the deadtime is very small in comparison to the total period. In this case, the entire effect of changing the ramp voltage is upon the charging time of the oscillator Synchronizing to a higher frequency simply reduces the charging time of Ct, (Tchg). The new charging time (Tchg') is the original charge time multiplied by the change in frequency between F original and F sync. This relative change will be used in several equations; it is labelled P, for percentage of change.

$$\frac{T\,chg'}{T\,chg(o)} = \frac{T\,sync}{T\,orig} = \frac{F\,orig}{F\,sync} = P\ \text{“relative F change”}$$

For small values of charging current, or large values of Rt, the voltage drop across the 24 ohm resistor is negligible. A current of 2 milliamps will result in a 2.5% timing error with a 2 volt peak to peak oscillator ramp at Ct. It is also preferrable to free-run the IC oscillator at about a 15% lower frequency than the synchronization frequency, where “P” = 0.85.

$$\Delta Vosc'\ (sync) = \Delta Vosc(o) \bullet P = 0.85 \bullet \Delta[Vosc]\ orig.$$

$$T\,chg' = T\,chg(o) \bullet P = 0.85\ T\,chg(o)$$

$$V\ sync\ (minimum)\ amplitude = \Delta\,[Vosc] \bullet (1\text{-}P)$$
$$= 0.15 \bullet \Delta\,[Vosc(o)]$$

With an approximate 2 volt peak to peak oscillator amplitude, the minimum sync pulse amplitude is 0.30 volts for synchronization to occur with a 15% latitude in frequencies.

### Oscillator Discharge Ramp Equations

Proper deadtime control in the switching power stage is required to safeguard against catastrophic failures. Adding the sync circuit to the oscillator reduces the discharge time of the timing capacitor Ct, hence reducing the deadtime of the PWM. There are two contributing factors. First, the peak amplitude at the timing capacitor is lowered by ΔV osc(o) - ΔVosc', and the capacitor begins its discharge from a lower potential. Second, the 24 ohm resistor adds an offset voltage, dependent on its current. Typical IC discharge currents range from approximately 6 to 12 milliamps. This offset due to charging current (1-2 ma) is low in comparison to that of the discharge current (6 to 12 ma). While negligible during the charge cycle, its tenfold effects must be taken into account during the discharge, or deadtime.

The discharge time (T dchg) can be calculated knowing the discharge current of the particular IC. More convenient is to use the manufacturers' published deadtime listing for a known value of Ct, and to calculate the effects of the sync circuit. The discharge current has been averaged to 8 milliamps for brevity.

$$\Delta V\,dschg' = [\Delta Vdchg(o) \bullet P] - V\ (24\ ohm)$$
$$= [0.85 \bullet \Delta Vosc(o)] - 0.2\ volts$$

$$T\,dchg' = T\,dchg(o) - T\ loss\ (24\ ohms)$$
where T dchg(o) = initial deadtime from curve
$$= T\,dchg(o) \bullet [\Delta V\,dchg' / \Delta Vosc(o)]$$

The actual deadtime is a summation of both the discharge time of Ct and the width of the sync pulse. While being applied, the sync pulse disables the PWM outputs and must be added to the discharge time. The sync pulse width can be used to compensate for the "lost" deadtime, or as a deadtime extension.

T dead' = T dchg' + T sync pulse width

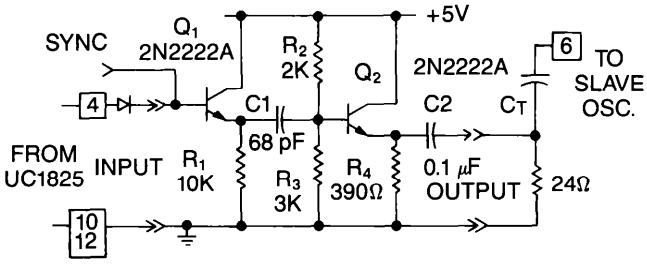



**Figure 19. Sync Circuit Schematic**

**Operating Principles**

A positive going signal is input to the base of transistor Q1 which operates as an emitter follower. The leading edge of the sync signal is coupled into the base of Q2 through capacitor Cl, developing a voltage across R4 in phase with the sync input. This signal is driven through C2 to the slave timing capacitor and 24 ohm resistor network, forcing synchronization of the slave to the master This high speed pulse amplifier circuit adds a minimum of delay (≈ 50 ns) between the master to slave timing relationship.

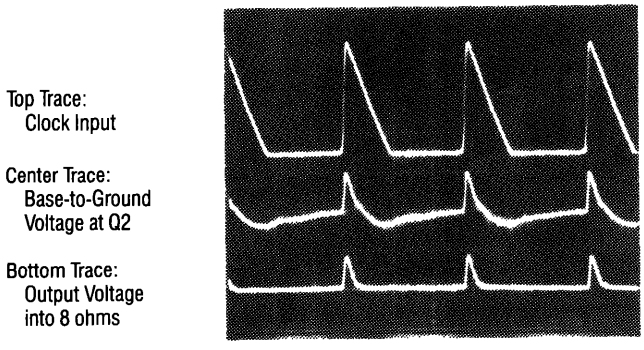



**Figure 20. Sync Circuit Waveforms**

This photo displays the waveforms of the sync circuit in operation at a clock frequency of 1 megahertz. The top trace is the circuit input, a 2.5 volt peak-to-peak clock output signal from the UC3825 PWM. Any of several other PWMs can be used as the source with similar results at lower frequencies. The center trace depicts the base to ground voltage waveform at transistor Q2, biased at 3 volts. The lower trace displays the output voltage across R4 while driving three slave modules, or about 8 ohms from the 5 volt reference.

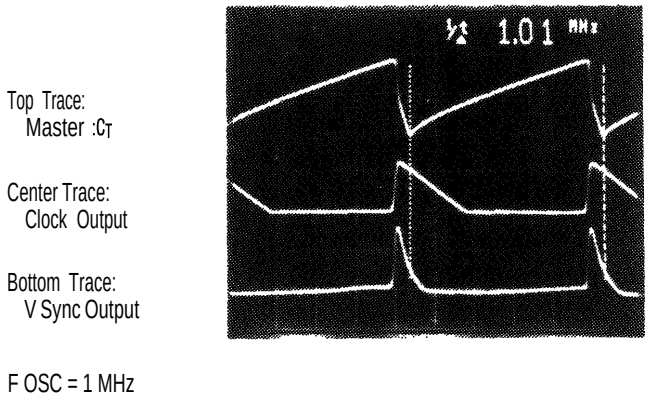



**Figure 21. Circuit Timing Waveforms**

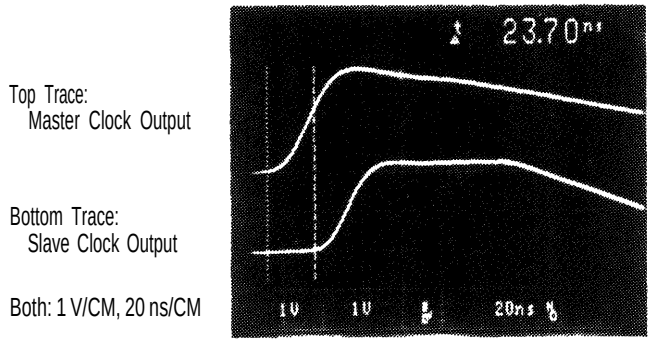



**Figure 22. Sync Circuit Delay; Input to Output**

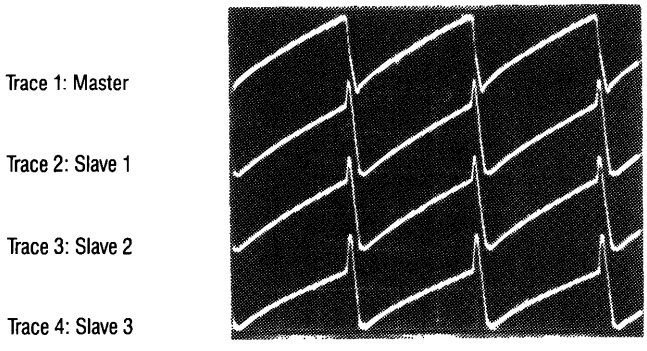



**Figure 23. Oscillator Waveforms: Master and Slaves**

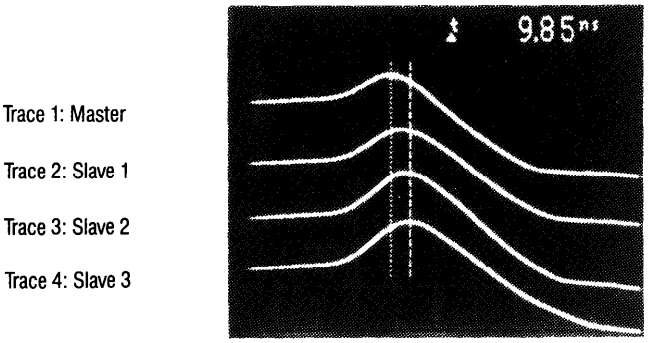



**Figure 24. Typical Sync Delay at CT: Master to Slaves**

Synchronization ranges for the slaves were discussed in the previous text. The 1 volt sync pulse will accommodate most ranges in frequency due to manufacturers' tolerances. The following photo is included to display the outcome of trying to use the sync circuit on slaves with oscillator frequencies set beyond the sync circuit range. The upper trace is the master Ct waveform. The center trace is Ct of a slave free-running at approximately one half that of the master. The sync pulse alters the waveform, however does not bring it above the comparator's upper threshold to force synchronization. The lower trace shows a slave free running at approximately twice that of the master's oscillator In this instance, the sync pulse forces synchronization at alternate cycles to the master.

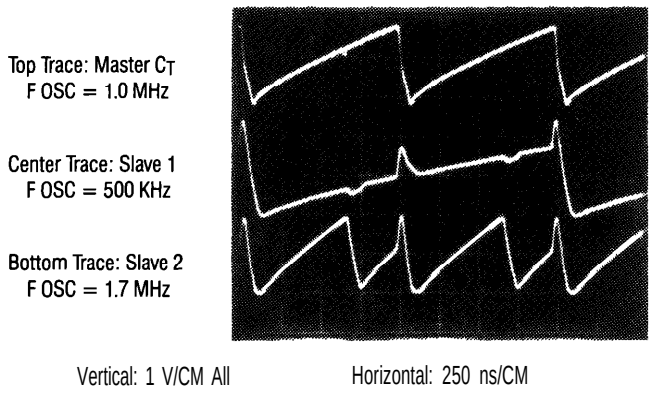



**Figure 25. Nonsynchronous Operation**

For voltage mode control, the free-running frequencies of the oscillator should be set as close to the master as tolerances will allow. One of the consequences of not doing so is the reduced amplitude of the Ct waveform, resulting in a lower dynamic range to compare against the error amplifier output. The top trace in the following photo shows that slave 1 has a much smaller ramp than slave 2, the lower trace. The amplitude should be made as large as possible to enhance circuit performance.

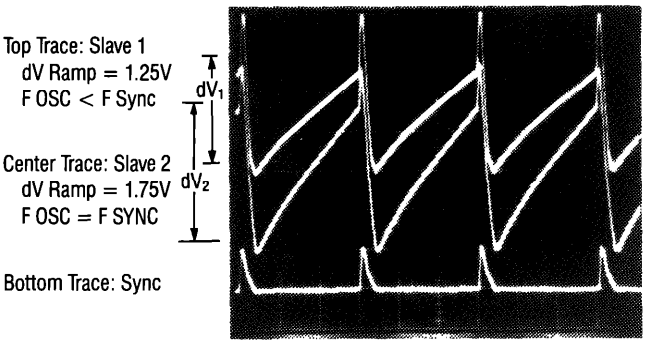



**Figure 26. $C_T$ Ramp Amplitude Waveforms**

### Sync Pulse Generation from the Oscillator Ct Waveform

Not every PWM IC is equipped with a sync output terminal from the oscillator. This is certainly the case with most low cost, mini-dip PWMs with a limited number of pin, like the UC1842/3/4/5. These ICs can provide a sync output with a minimum of external components.

Common to all PWMs of interest is the timing capacitor, Ct, used in the oscillator frequency generation. The universal sync circuit previously described triggers from the master deadtime, or Ct discharge time. A simple circuit will be described to detect this falling edge of the Ct waveform and generate the sync pulse required to the slave PWM(s).

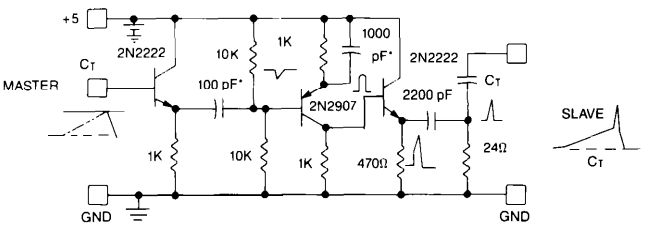



**Figure 27. Sync Pulse Generator Circuit**

### Operating Principles

Transistor Q1 is an emitter follower to buffer the master oscillator circuit, and capacitively couples the falling edge of the timing waveform to the base of Q2. Since the rising edge of the waveform is typically ten or more times slower, it does not pass through to Q2, only the falling edge, or deadtime pulse is coupled. Transistor Q2 inverts this sync signal at its collector, which drives Q3, the power stage of this circuit. Similar to the universal sync circuit, the slave oscillator sections are driven from Q3's emitter. This circuit is useable to several hundred kilohertz with a minimum of delays between the master and slave synchronization relationship.

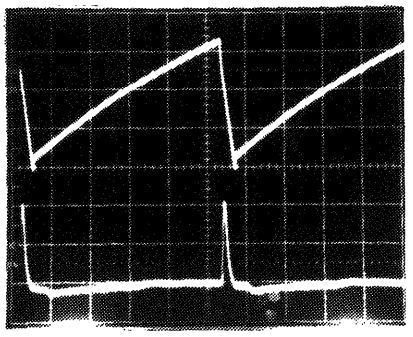



**Figure 28. Operating Waveforms at 500 KHz**

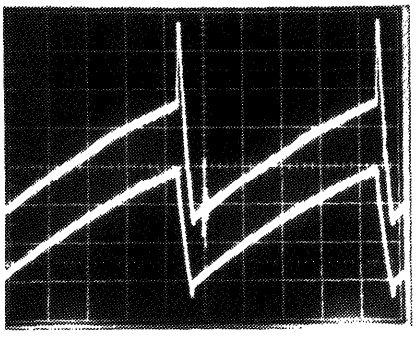



**Figure 29. Master/Slave Sync Waveforms at CT**

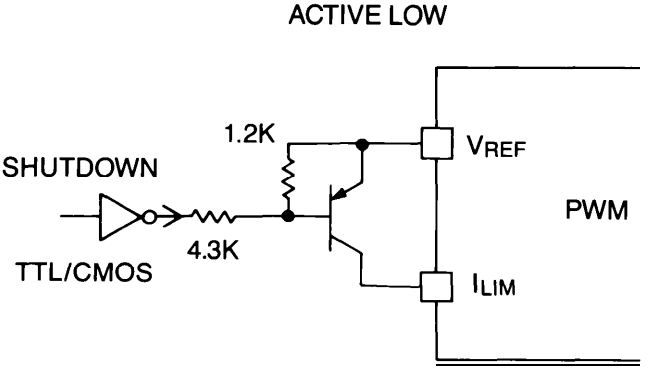
## IV. EXTERNALLY CONTROLLING THE PWM

Many of today's sophisticated control schemes require external control of the power supply for various reasons. While most of these requirements can be incorporated quite easily with a full functioned control chip, (typical of a 16 pin device), implementation may be more complex with a low cost, 8 pin PWM. Circuits to provide these functions with a minimum of external parts will be highlighted.

### Shutdown

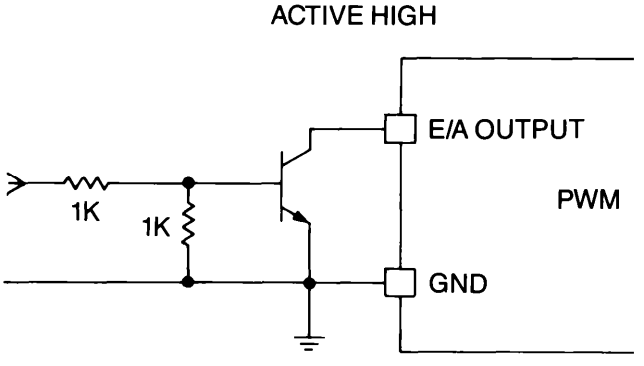
One of the most common requirements is to provide a complete shutdown of the power supply for certain situations like remote on/off, or sequencing. Typically, a TTL level input is used to disable the PWM outputs. Both voltage and current mode control ICs can perform this task by simply pulling the error amplifier output below the lower threshold of the PWM comparator of approximately 0.5 volts. This can be easily implemented via an NPN transistor placed between the E/A output and ground, used to short circuit the E/A output to zero volts. In most cases, this node is internally current limited to prevent failures.

Another scheme is to pull the current limit or current sense input above its upper threshold. A small transistor from this input to the reference voltage will fulfill this requirement.




A. NONLATCHING

**Figure 30. PWM Shutdown Circuits**

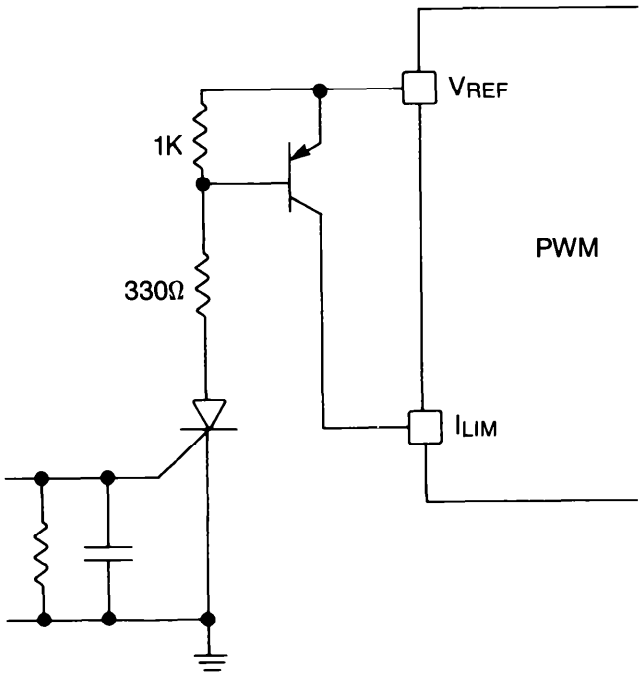



B. NONLATCHING

**Figure 31.**

### Latching Shutdown

For those applications which require a latching shutdown mechanism, an SCR can be used in conjunction with the above circuits, or in lieu of them. The SCR can also be placed from the PWM E/A output to ground, provided the PWM E/A minimum short circuit current is greater than the maximum holding current of the SCR, and the voltage drop at I(hold) is less than the lower PWM threshold.

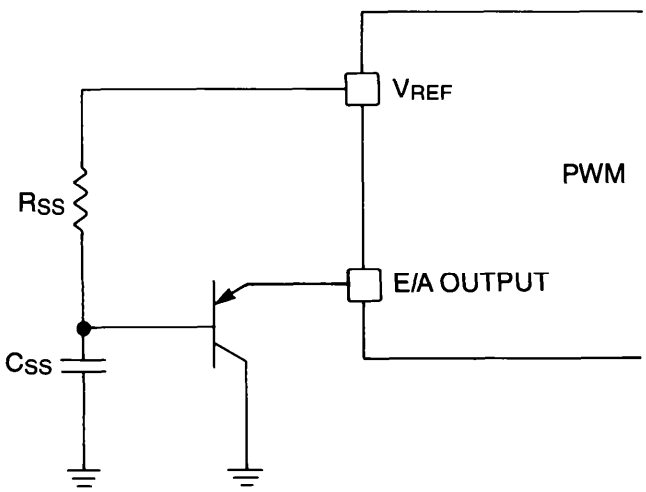



C. LATCHING

**Figure 32.**

**Soft Start**

Upon power-up, it is desirable to gradually widen the PWM pulse width starting at zero duty cycle. On PWMs without an internal soft start control, this can be implemented externally with three components. An R/C network is used to provide the time constant to control the I limit input or error amplifier output. A transistor is also used to isolate the components from the normal operation of either node. It also minimizes the loading effects on the R/C time constant by amplification through the transistors gain.




B. USING E/A

**Figure 33.**

**Variable Frequency Operation**

Certain topologies and control schemes require the use of a variable frequency oscillator in the controlling element. However, most PWMs are designed to operate in a fixed frequency mode of operation. A simple circuit is presented to disable the ICs internal oscillator between pulses, thus allowing variable frequency operation.

Internal at the ICs timing resistor (Rt) terminal is a current mirror The current flowing through Rt is duplicated at the Ct terminal during the charge cycle, or "on" time. When the Rt terminal is raised to V ref (5 volts), the current mirror is turned off, and the oscillator is disabled. This is easily switched by a transistor and external logic as the control element, for example, a pulse generator. The PWM's timing resistor and capacitor should be selected for the maximum "ON" time and minimum "DEAD" time of the PWM output(s). The rate at which the PWM oscillator is disabled determines the frequency of the output(s).

The frequency can be varied in two distinct fashions depending on the desired control mode and trigger source. The "off" time of both outputs will occur on a pulse-by-pulse basis when the PWM outputs are OR'd to the trigger source. In this configuration either output initiates the "off" time, triggered by its falling edge. The PWM output A is activated, then both outputs A and B are low during the "off" time of the pulse generator. This is followed by output B being activated, then both outputs A and B low again during the next "off" time. This cycle repeats itself at a frequency determined by the pulse generator circuitry.

Another method is to introduce the "off" time after two (alternate A, then B) output pulses. Output A is activated, followed immediately by output B, then the desired "off" time. The pulse generator circuitry is triggered by the PWM's falling edge of output B. The specific control scheme utilized will depend on the power supply topology and control requirements.

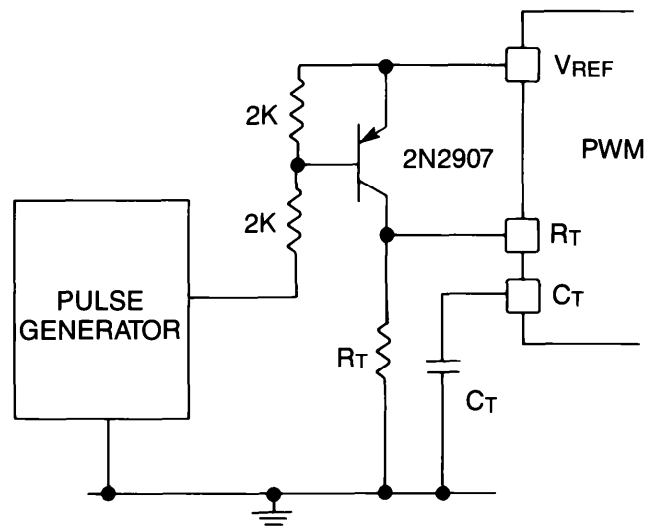
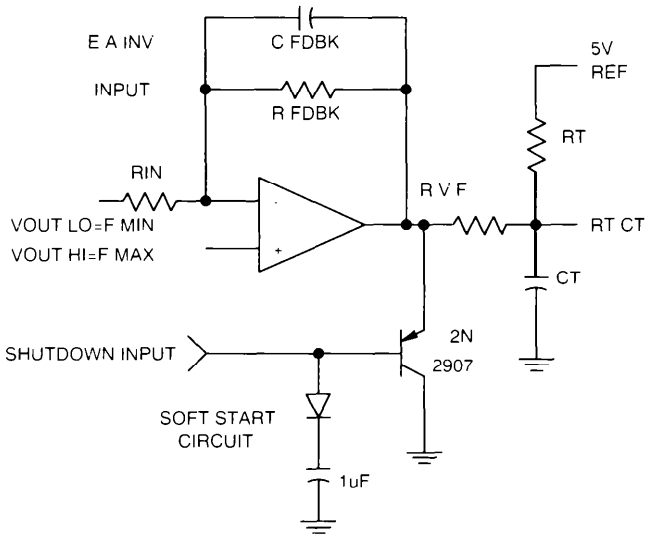



**Figure 34. Oscillator Disable Circuit Variable Frequency Operation**

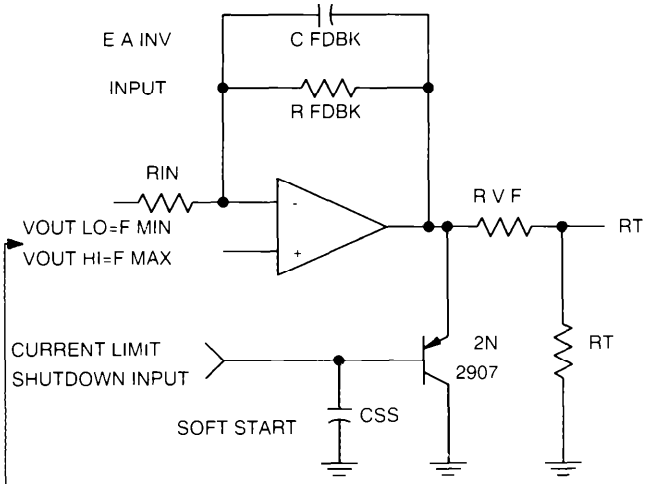
## VOLTAGE CONTROLLED OSCILLATOR GENERAL CONFIGURATION

VARIABLE FREQUENCY OPERATION
FIXED 50% DUTY CYCLE
OSCILLATORS WITH SINGLE PIN PROGRAMMING




UC3851 / UC3844A / UC3845A
*GROUND RAMP OR CURRENT SENSE INPUT

OSCILLATORS WITH SEPARATE RT & CT PINS



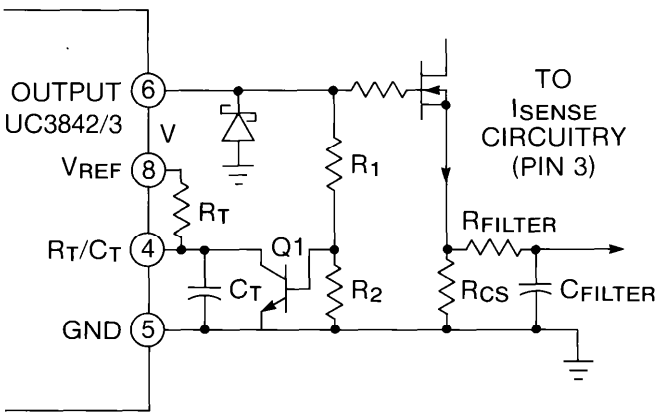

U C 3 8 2 3 / U C 3 8 2 5 / U C 3 8 4 7
*GROUND RAMP OR CURRENT SENSE INPUT
USE NONINV E/a INPUT FOR REVERSE V/F OPERATION

**Fixed "Off -Time" Applications**
Obtaining a fixed "off-time" and a variable "on-time" can easily be accomplished with most current-mode PWM IC's. In these applications, the Rt/Ct timing components are used to generate the "off-time" rather than the traditional "on-time." Implementation is shown schematically in Figure 3 along with the pertinent waveforms.

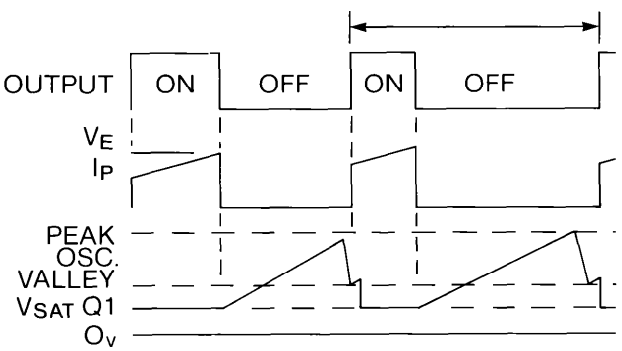
At the beginning of an oscillator cycle, Ct begins charging and the PWM output is turned on. Transistor Q1 is driven from the output and also turns on with the PWM output, thus discharging Ct and pulling this node to ground. As this occurs, the oscillator is "frozen" with the PWM output fully ON. On-time can be controlled in the conventional manner by comparing the error amplifier output voltage with the current sense input voltage. This results in a current controlled "on-time" and fixed "off-time" mode of operation. Other variations are possible with different inputs to the current sense input.

When the PWM output goes low (off ), transistor Q1 also turns off and Ct begins charging to its upper threshold.The off-time generated by this approach will be longer for a given Rt/Ct combination than first anticipated using the oscillator"charging" equations or curves. Timing capacitor Ct now begins charging from Vsat of Q1 (approx. 0V) instead of the internal oscillator lower threshold of approximately 1 volt.

FIXED "OFF-TIME", CURRENT
CONTROLLED "ON-TIME"




SCHEMATIC




WAVEFORMS

**Figure 35.**

### Current Mode ICs Used in Voltage Mode

Most of today's current mode control ICs are second and third generation PWMs. Their features include high current output driver stages, reduced internal delays through their protection circuitry, and vast improvements in the reference voltage, oscillator and amplifier sections. In comparison to the first generation ICs (1524), numerous advantages can be obtained by incorporating a second or third generation IC (18XX) into an existing voltage mode design.

In duty cycle control (voltage mode), pulse width modulation is attained by comparing the error amplifier output to an artificial ramp. The oscillator timing capacitor Ct is used to generate a sawtooth waveform on both current or voltage mode ICs. To utilize a current mode chip in the voltage mode, this sawtooth waveform will be input to the current sense input for comparison to the error voltage at the PWM comparator. This sawtooth will be used to determine pulse width instead of the actual primary current in this method.

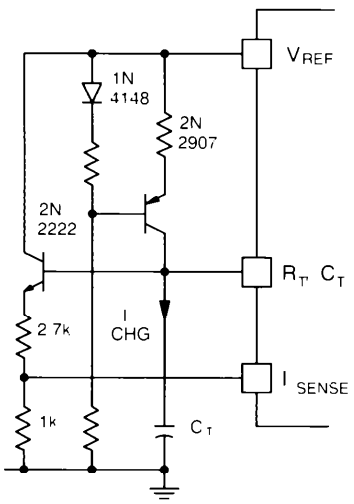



**Figure 36. Current Mode PWM Used as a Voltage Mode PWM**

Compensation of the loop is similar to that of voltage mode, however, subtle differences exist. Most of the earlier PWMs (15xx) incorporate a transconductance (current) type amplifier, and compensation is made from the E/A output to ground. Current mode PWMs use a low output resistance (voltage) amplifier and are compensated accordingly. For further reference on topologies and compensation, consult "Closing the Feedback Loop" listed in this appendix.

### VI. FULL DUTY CYCLE (100%) APPLICATIONS

Many of the higher power (>500 watt) power supplies incorporate the use of a fan to provide cooling for the magnetic components and semiconductors. Other users locate fans throughout a computer mainframe, or other equipment to circulate the air and keep temperatures from skyrocketing. In either case, the power supply designer is usually responsible for providing the power and control.

The popularity of low voltage DC fans has increased throughout the industry due to the stringent agency safety requirements for high voltage sections of the overall circuit. In addition, it's much easier to satisfy dual AC inputs and frequency stipulations with a low cost DC fan, powered by a semi-regulated secondary output.

The most efficient way to regulate the fan motor speed (hence temperature) is with pulse width modulation. An error signal proportional to temperature can be used as the control voltage to the PWM error amplifier. While nearly full duty cycle can be easily attained, the circumstances may warrant full, or true 100% duty cycle.

This condition is highly undesirable in a switch-mode power supply, therefore most PWM IC designs have gone to great extent to prevent 100% duty cycle from occurring. There are simple ways to over-ride these safeguards, however. One method, presented below, "freezes" the oscillator and holds the PWM output in the ON, or high state when the circuit is activated. Feedback from the output is required to guarantee that the oscillator is stopped while the output is high. Without feedback, the oscillator can be nulled with the output in either state.

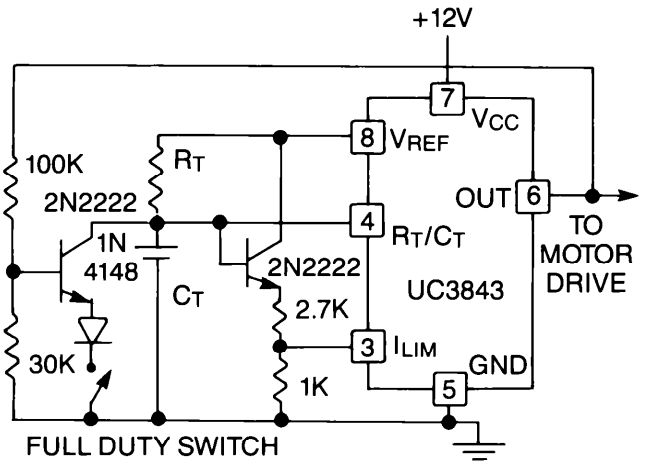



**Figure 37. Full Duty Cycle Implementation**

## VII. HIGH EFFICIENCY START-UP CIRCUITS FOR BOOTSTRAPPED POWER SUPPLIES

Many pulse width modulator I.C.s have been optimized for offline use by incorporating an under-voltage lockout circuit. Demanding only a milliamp or two until start-up, the auxiliary supply voltage (V aux) can be generated by a simple resistor/capacitor network from the high voltage dc rail (+V dc). Once start-up is reached, the auxiliary power is supplied by means of a "boostrap" winding on the main transformer.

While the start-up requirements are quite low, losses in the resistor to the high voltage DC can be significant in steady state operation. This is especially true for low power (< 35 watt) applications and circuits with high voltage rails (400 volts DC, for example). Once the main converter is running, switching the start-up resistor out of circuit would increase efficiency substantially. Circuits have been developed to use either bipolar or MOSFET transistors as the switch to lower the start-up circuit power consumption, depending on the application. Selection can be based on optimizing circuit efficiency (MOSFET) or lowest component cost (bipolar). The overall improvement in power supply efficiency suggests this circuitry is a practical enhancement.

The high efficiency start-up circuit shown in figure 1 utilizes two NPN bipolar transistors to switch the start-up resistor in and out of circuit. It can be used in a variety of applications with minor modifications, and requires a minimum of components. Figure 2 displays a similar circuit utilizing N channel MOSFET devices to perform the switching.

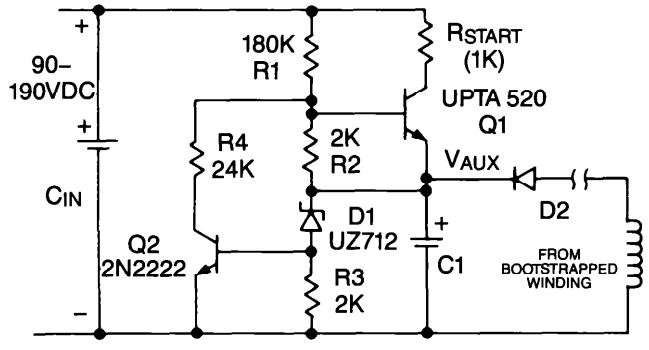



**Figure 38. NPN Switches**

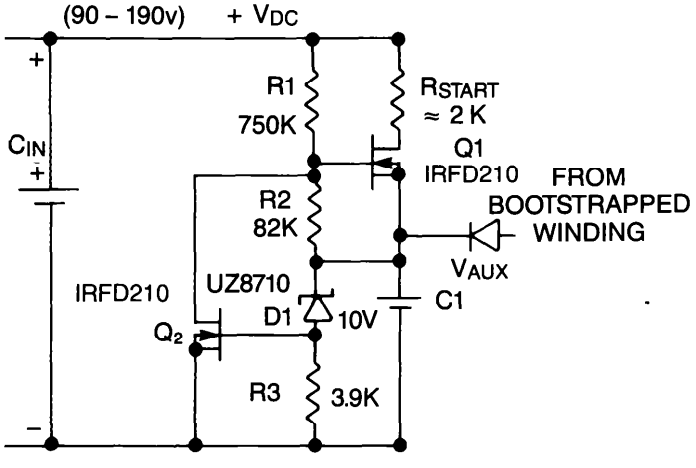



**Figure 39.**

### Theory of Operation

Prior to applying the high voltage DC, capacitor Cl is discharged; switches Q1, Q2 and the main converter are off. As the input supply voltage (Vdc) rises, resistors R1 and R2 form a low current voltage divider. The voltage developed across R2 rises accordingly with +V dc until switch Q1 turns on, thus charging C1 thru R start-up from +V dc. This continues as the UV lockout threshold of the I.C. is reached and the main converter begins operation. Energy is delivered to Cl from the bootstrap winding in addition to that supplied through R start-up.

After several cycles, the auxiliary voltage rises with the main converters increasing pulse width, typical of a soft-start routine. Current flows through zener diode D1 and develops a voltage across the Q2's biasing resistor, R3. Transistor Q2 turns on when the auxiliary voltage reaches V zener plus Q2's turn on threshold. As this occurs, transistor Q1 is turned off, thus eliminating the start-up resistor from the circuit power losses. In most applications, the auxiliary voltage is optimized between 12 and 15 volts for driving the main power MOSFETs, while keeping power dissipation in the PWM IC low.

If the main converter is shut down for some reason, V aux will decay until Q2 turns off. Transistor Q1 then turns back on, and Cl is charged through R start-up from the high voltage DC, as during start-up.

**NOTE:** SEE DESIGN NOTE DN-26 FOR ADDITIONAL CIRCUITS.

## VIII. CURRENT MODE HALF BRIDGE APPLICATIONS

As previously described (1), current mode control can cause a "runaway" condition when used with a "soft" centered primary power source. The best example of this is the half bridge converter using two storage capacitors in series from the rectified line voltage. For 110 VAC operation, the input is configured as a voltage doubler, and one of the AC inputs is tied directly to the storage capacitor's centerpoint. This is considered a "stiff" source, since the centerpoint will remain at one-half of the developed voltage between the upper and lower rail. However, during 220 VAC inputs, a bridge configuration is used for the input rectifiers, and the capacitors are placed in series with each other, across the bridge. Their centerpoint potential will vary when different amounts of charge are removed from the capacitors. This is generally caused by uneven storage times in the switching transistors Q1 and Q2.

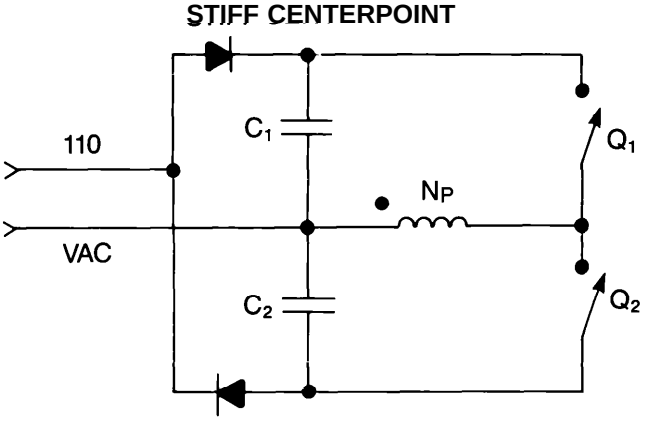



**Figure 40.**

SOFT CENTERPOINT

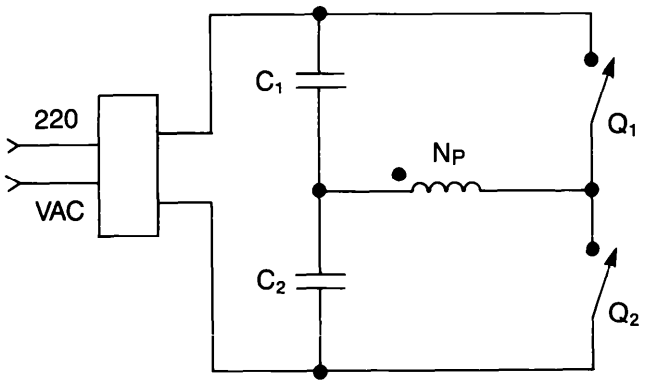



**Figure 41.**

The centerpoint voltage can be maintained at one-half +Vdc by the use of a balancing technique. In normal operation, transistor Q1 turns on, and the transformer primary is placed across one of the high voltage capacitors, C1 for example. On alternate cycles the transformer primary is across the other cap, C2. An additional balancing winding, equal in number in turns to the primary, is wound on the transformer. It is connected also to the capacitor centerpoint at one end and thru diodes to each supply rail at the other end. The phasing is such that it is in series with the primary winding through the ON time of either transistor Q1 or Q2.

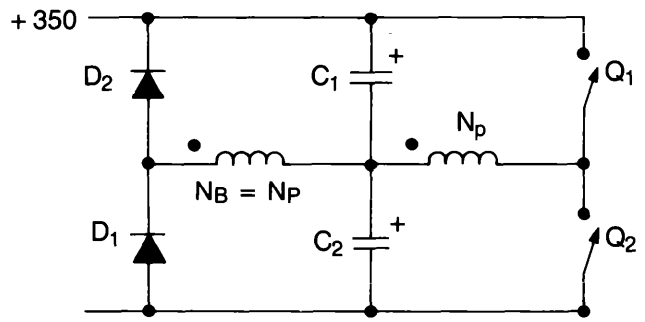



**Figure 42. Schematic - Balancing Winding**

In this configuration, the center point of the high voltage caps is forced to one-half of the input DC voltage by nature of the two series windings of identical turns. Should the midpoint begin to drift, current flows thru the balancing winding to compensate.

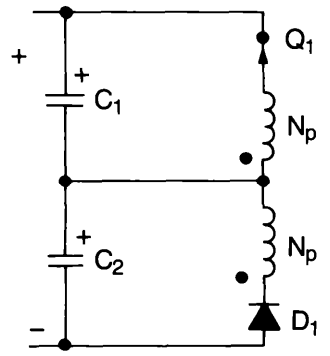



**Figure 43. Transistor Q1 On**

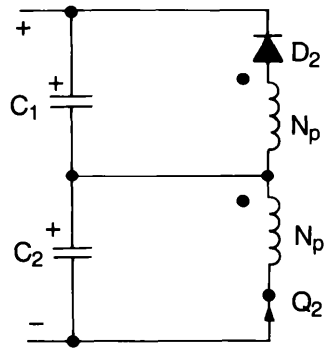



**Figure 44. Transistor Q2 On**

In most high frequency MOSFET designs, the FET mismatches are small, and the average current in the balancing winding is less than 50 milliamps. A small diameter wire can be wound next to the larger sized primary for the balancing winding with good results.

## IX. PARALLELING CURRENT MODE MODULES

One of the numerous advantages of current mode control is the ability to easily parallel several power supplies for increased output power. This discussion is intended as a primer course to explore the basic implementation scheme and design considerations of paralleling the power modules. Redundant operation, failure modes and their considerations are not included in this text.

The prerequisites for parallel operation are few in number, but important to insure proper operation. First, each power supply module must be current mode controlled, and capable of supplying its share of the total output power. All modules must be synchronized together, and one unit can be designated as the master for the sake of simplicity. All remaining units will be configured as slaves.

The master will perform one function in addition to generating the operating frequency. It provides a common error voltage (Ve) to all modules as the input to the PWM comparator. This voltage is compared to the individual module's primary current at its PWM comparator. The slaves are utilized with their error amplifier configured in unity gain. Assume there are identical primary current sense resistors in each module, and no internal offsets in the ICs amplifiers or other circuit components. In this case, the output voltages and currents of each module would be identical, and the load would be shared equally among the modules.

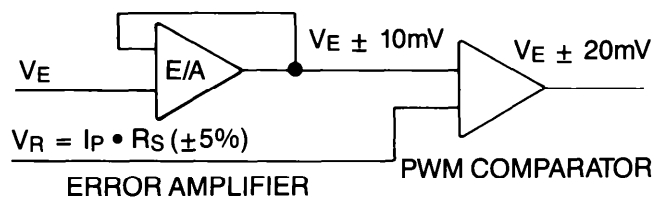



**Figure 45. PWM Diagram**

In reality, small offets of ± 10 millivolts exist in each PWM amplifier and comparator. As the common error voltage, (Ve) traverses through the IC's circuitry, its accuracy decreases by the number and quality of gates in its path. The maximum error occurs at the lowest common mode amplifier voltage, approximately 1 volt. The ± 20 millivolt offset represents a ± 2% error at the PWM comparator. At higher common mode voltages, typical of full load conditions, the error voltage (Ve) is closer to its maximum of 4 volts. Here the same ± 20 millivolts introduces only ± 0.5% error to the signal.

The other input to the PWM comparator, Vr, is the voltage developed by the primary current flowing through the current sense resistor(s). In many applications, a 5% tolerance resistor is utilized resulting in a ± 5% error at the PWM comparator's "current sense" or ramp input.

Pulse width is determined by comparing the error voltage (Ve) with the current sense voltage, (Vr). When equal, the primary current is therefore the error voltage divided by the current sense resistance; Ip = Ve/Rs. Output current is related to the primary current by the turns ratio (N) of the transformer. Sharing of the load, or total output current is directly proportional to the sharing of the total primary current. The previous equations and values can be used to determine the percentage of sharing between modules.

Primary current, Ip = Ve/Rs. Introducing the tolerances, Ip' = Ve (± 2%) / Rs (± 5%); therefore Ip' = Ip (± 7%) The primary currents (hence output currents) will share within ± seven percent (7%) of nominal using a five percent sense resistor. Clearly, the major contribution is from the current sense circuitry, and the PWM IC offsets are minimal. Balancing can be improved by switching to a tighter tolerance resistor in the current sense circuitry.

The control-to-output gain (K) decreases with increasing load. At high loads, when primary currents are high, so is the error amplifier output voltage, (Ve). With a typical value of four volts, the effects of the offset voltages are minimized. This helps to promote equal sharing of the load at full power, which is the intent behind paralleling several modules.

For demonstration purposes, four current mode push-pull power supplies were run in parallel at full power. The primary current of each was measured (lower traces) and compared to a precision 1 volt reference (upper trace). The voltage differential between traces is displayed in the upper right hand corner of the photos. Using closely matched sense resistors, the peak primary currents varied from a low of 2.230A to 2.299 amps. Calculating a mean value of 2.270 amps, the individual primary currents shared within two percent, indicative of the sense resistor tolerances.

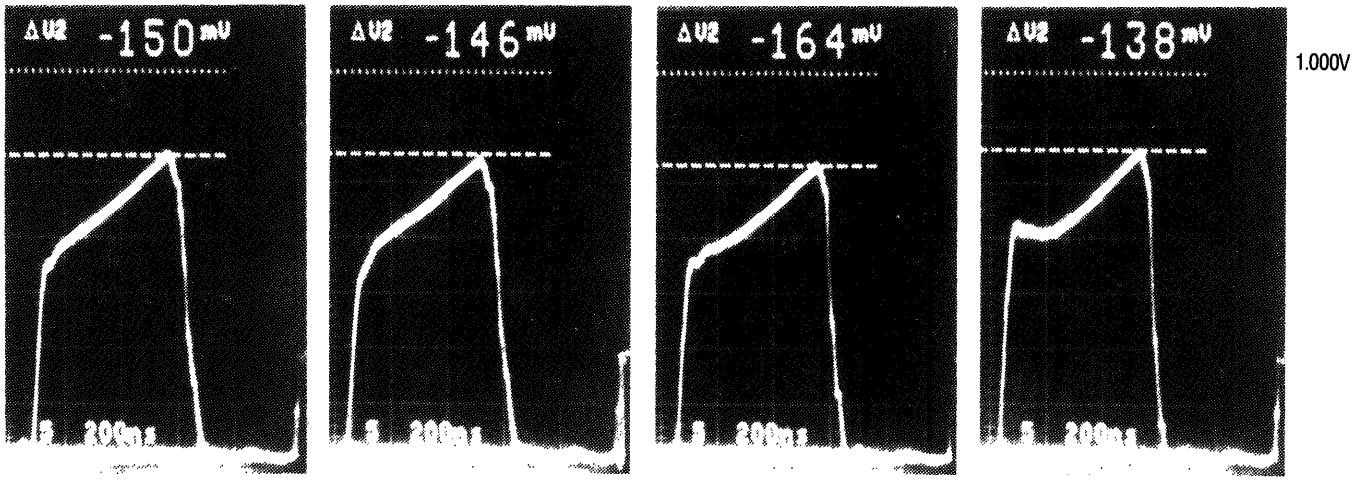



**Figure 46. Primary Currents - Parallel Operation**

Other factors contributing to mismatch of output power are the individual power supply diode voltage drops. The output choke inductance reflects back to the primary current sense, and any tolerances associated with it will alter the primary current slope, hence current. In the control section, the peak-to-peak voltage swing at the timing capacitor Ct effects the amount of slope compensation introduced, along with the tolerance of the summing resistor These must all be accounted for to calculate the actual worst case current sharing capability of the circuit.

Top Trace:
$V_E$: Error Voltage with Noise

Lower Trace:
$V_R$: Primary Current

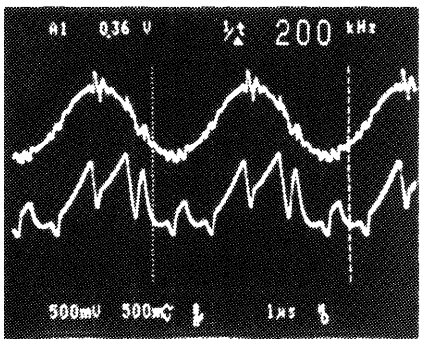



**Figure 47. Noise Modulating $V_E$**

Proper layout of all interconnecting wires is required to insure optimum performance. Shielded coax cable is recommended for distributing the error voltage among the modules. Any noise on this line will demonstrate its impact at the PWM comparator, resulting in poor load sharing, or jitter.

Cables should be of equal length, originating at the master and routed away from any noise sources, like the high voltage switching section. All input and output power leads should be exactly the same length and wire gauge, connected together at ONE single point. Leads should be treated as resistors in series with the load, and deviations in length will result in different currents delivered from each module.

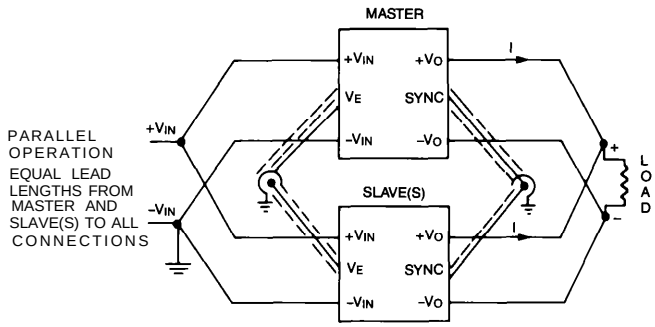



**Figure 48.**

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