

“Single-Cycle Control” Technique sets new Industry Standard for Continuous Conduction Mode PFC Controllers

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Abstract – This paper presents a novel approach for control of high performance Boost Power Factor Correction (PFC) circuits operating at a fixed frequency in the continuous conduction mode. The complex multiplier and input line voltage sensing circuits required with traditional control methods are eliminated with the proprietary "Single-Cycle Control" (SCC) method where they are replaced with an integration reset technique. The benefits of overall system robustness, improved transient performance, and simplicity are complemented by a 75% reduction in pcb space and component count.

I. INTRODUCTION

Power Factor Correction (PFC) and harmonic current reduction are fast becoming standard requirements in most power supply designs today. The compelling environmental and economic benefits resulting from the use of Power Factor Correction in power supplies has encouraged governing bodies and end customers to demand more widespread use of PFC circuits across a much broader spectrum of power levels and product lines than ever before.

This is not particularly good news for Power Supply manufacturers given that the cost and complexity of high performance PFC circuits have not changed drastically since the introduction of the first commercially available Continuous Conduction Mode (CCM) PFC controllers. In fact, to this day, the mainstream controllers used in single phase boost (CCM) PFC circuits still use the same scheme developed many years ago. At lower powers or where low cost is critical, the lower efficiency, lower power density "Discontinuous Current Mode" (DCM) PFC technique is used [Ref 1].

This paper proposes a new industry "standard" for PFC named "Single Cycle Control" (SCC). The features of SCC (design simplicity, component count reduction and minimized pcb space) enable the

higher performance of the CCM topology with the system cost benefits typically associated with DCM PFC.

Simple mathematical derivations will provide clear insight into the theory of the concept. The theory will then be substantiated by lab results from both a discrete controller and the first prototype silicon version of the controller.

A close comparison of the "Single Cycle Control" technique vs. the existing mainstream solution will also demonstrate the dramatic benefits in cost reduction, component count reduction, board space savings and reduced design effort and complexity.

Finally a discussion for potential SCC products will be presented.

II. EXISTING SOLUTION

To understand the benefits of the “Single Cycle Control” scheme better, it is worthwhile to briefly review the existing (CCM) PFC solution. Below is a block diagram of the popular UC3854 controller [ref 2].

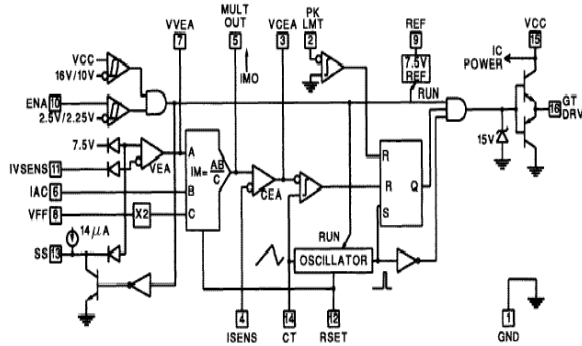


Fig 1.

As seen in Fig 1 the heart of this existing PFC controller is an analog multiplier / divider. In order to force the input current to follow the input voltage, the multiplier circuit samples the rectified AC line voltage and creates a sinusoidal current reference signal. This signal then controls the duty cycle of the main PWM controller, forcing the input current of the Boost converter to follow the sinusoidal shape of the input voltage, thereby providing near unity power factor and reduced current harmonics.

Given the sensitivity of the control loop and the multiplier block, any distortion or noise injected into the inputs can have a negative impact on the power factor and harmonic distortion of the input current. PCB layout issues also play an important role, as does the selection of the components and their optimum values. It is not uncommon to have several design iterations of the control circuit in order to get optimum performance throughout the full line and load range. A well-designed (CCM) PFC circuit requires strong power engineering background both in practice and theory.

III. SINGLE CYCLE CONTROL

The proprietary SCC technique has an elegant and simplistic approach, which does not require a multiplier to create the current reference signal. In fact

there is no sinusoidal current reference per se as the traditional solution.

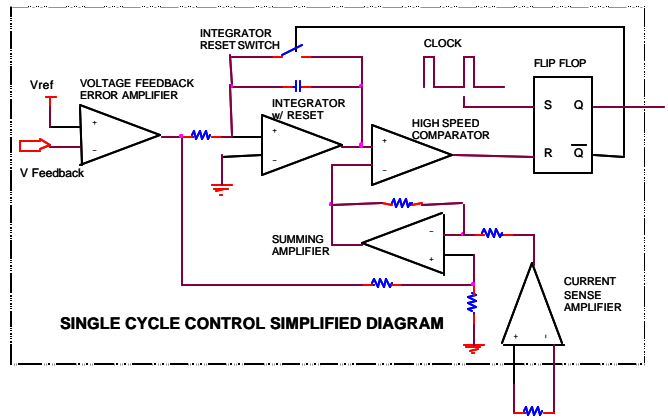


Fig 2

As seen in Fig 2, the heart of the “Single Cycle Control” is a new proprietary Integrator w/ Reset (IWR) circuit block. This block simply integrates the output voltage of the voltage error amplifier. This integrated ramp signal is then compared to an analog reference voltage generated from the sum of the current and the error voltage. When the integrator ramp reaches the limit set by this internally generated reference voltage, the PWM pulse is immediately terminated. At this time the integrator output is also discharged to zero and held low till the next clock pulse. The name “Single Cycle Control” simply refers to the cycle-by-cycle operation of the integrator and the generation of the reference signal during each switching cycle.

IV. MATHEMATICAL DERIVATION

The essential goal of any PFC control system is to force the converter to appear as a resistive load across the AC Line. Following this simple derivation, it can be seen why the new solution is simpler, more robust, less noise sensitive and yet provides the same high level of performance as the older CCM designs. For the avid reader more extensive analysis and theory is available (Ref 3).

Referring to Fig 3 we start by representing the converter as a simple resistor and expressing the current and voltage relationships using simple Ohm's law,

$$(1) \quad I_{IN} = V_{IN} / R_E$$

Where,

I_{IN} is the input current

V_{IN} is the input Voltage

R_E is the emulated resistance of converter

During the Quasi-Steady State, the boost converter conversion ratio $M(d)$ can be stated as

$$(2) \quad V_O / V_{IN} = M(d)$$

Combining (1) and (2) and multiplying both sides with the current sense resistor R_S gives us

$$(3) \quad R_S I_{IN} = v_m / M(d)$$

where,

$$v_m = R_S * V_O / R_E$$

R_S is equivalent current sensing resistor

$M(d)$ is voltage conversion ratio of converter

Rewriting Equation (3) yields,

$$(4) \quad R_S I_{IN} = v_m * V_{IN} / V_O$$

V_O is assumed to remain constant over a line cycle if the output bulk capacitor C_O is large enough. If v_m is constant in that cycle, I_{IN} is proportional to V_{IN} thus making the converter appear as an emulated resistor.

$$(5) \quad R_E = R_S V_O / v_m$$

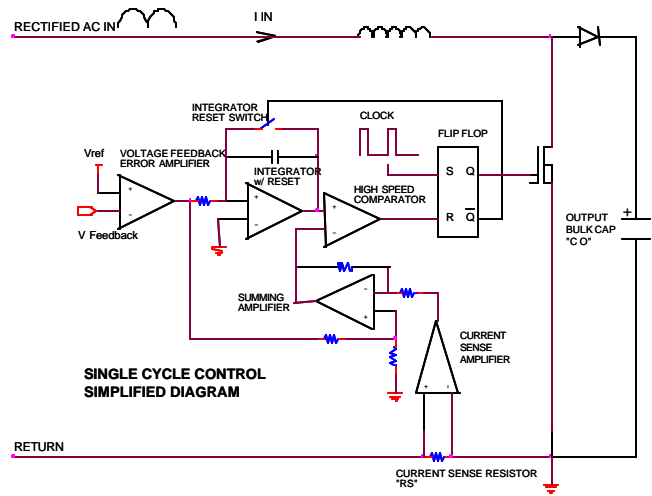


FIG 3. SINGLE CYCLE CONTROL BOOST PFC

V. EXPERIMENTAL RESULTS

A 1KW 100Khz fixed frequency Boost converter was built to verify the operation of the "Single Cycle Control" technique. A control board was fabricated using generic discrete components and the performance was validated at 500W and 1KW with 115V-230VAC 60Hz input. Power train components were independently optimized for both 500W and 1KW operation. The 500W breadboard was subsequently used to validate the prototype IRIS51xx silicon (IRIS = International Rectifier Integrated Switcher).

The converter input current and voltage waveforms are shown below. THD results are summarized in Table 1 and 2.

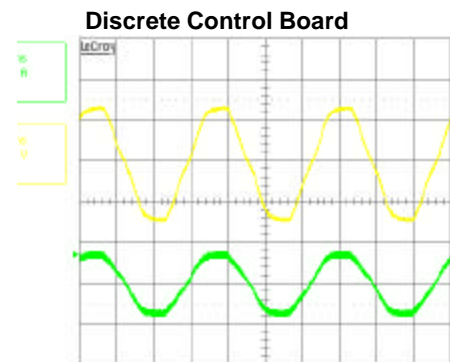


FIG 4. INPUT VOLTAGE AND CURRENT 85VAC 500W

Discrete Control Board

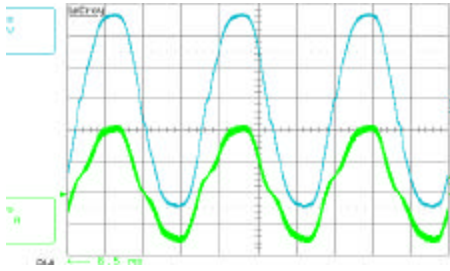


FIG 5. INPUT VOLTAGE AND CURRENT 230VAC 1KW

In-circuit PF / THD Data w/discrete Control

VAC	Pout (W)	Power Factor	THD (%)
115	500	0.997	4.98
230	500	0.987	9.1
115	1000	0.998	4.75
230	1000	0.988	8.9

Table 1.

These results exceed the IEC1000-3-2 specification requirements and show the near unity power factor.

VI. EXPERIMENTAL RESULTS IRIS51xx SILICON

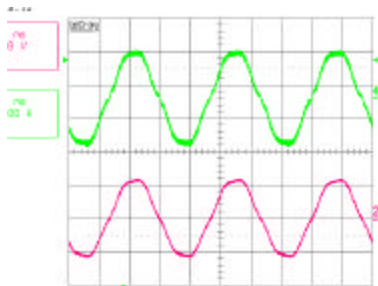


FIG 6. INPUT VOLTAGE AND CURRENT 85VAC 250W

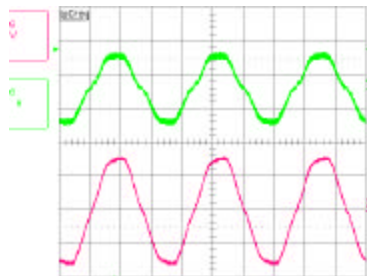


FIG 7 INPUT VOLTAGE AND CURRENT 230V 250W

In-circuit PF/THD Data w/ IRIS51xx (500W system)

VAC	Pout (W)	Power Factor	THD (%)
115	75	0.968	17.5
230	75	0.917	21.25
115	150	0.988	10.5
230	150	0.948	17.3
115	300	0.996	5.5
230	300	0.978	15.4

Table 2.

Again, these results meet IEC1000-3-2.

VII. SYSTEM DESIGN COMPARISON

The advantages of the “Single Cycle Control” method, in terms of required board space, component count, and overall system cost become readily apparent when a side-by-side comparison of a conventional multiplier based solution and an integrated “Single Cycle Control” method is made as shown in the schematic diagrams below.

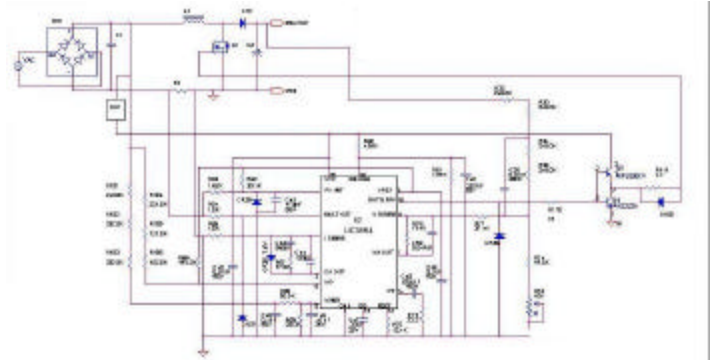


Fig 8. Typical UC3854 Application

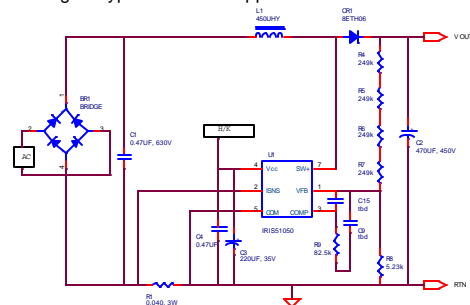


Fig 9. Typical IRIS51xx Application

Further benefit to the designer presents itself in the form of a simplified design process for the Single Cycle Control method. Basic power train selection and design criteria of the SCC IRIS51xx is identical to

that of the UC3854-based solution. The simplification of the design process is attributed to the elimination of the complex multiplier, error amplifier in current loop, and various line sense circuits from the system control loop. Comparison of the converter design procedure for the two methods highlights the true value of the “Single Cycle Control” methodology.

VIII. DESIGN PROCEDURE COMPARISON

The comparison below highlights the critical design steps for both the UC3854 and the “Single Cycle Control” IC.

UC3854 DESIGN PROCEDURE

- ?? Design/select power circuit components
- ?? Design/select current sense resistor
- ?? Design resistive divider for peak current limit
- ?? Design Enable circuit resistor divider
- ?? Select IAC resistor, (multiplier setup)
- ?? Design Vff divider, (multiplier setup)
- ?? Select Rbias resistor, (multiplier setup)
- ?? Select Rset resistor, (multiplier setup)
- ?? Select Rmo resistor, (multiplier setup)
- ?? Design current error amplifier compensation
- ?? Design voltage error amplifier compensation
- ?? Design output voltage feedback divider
- ?? Design 2 cascaded pole feed forward filter

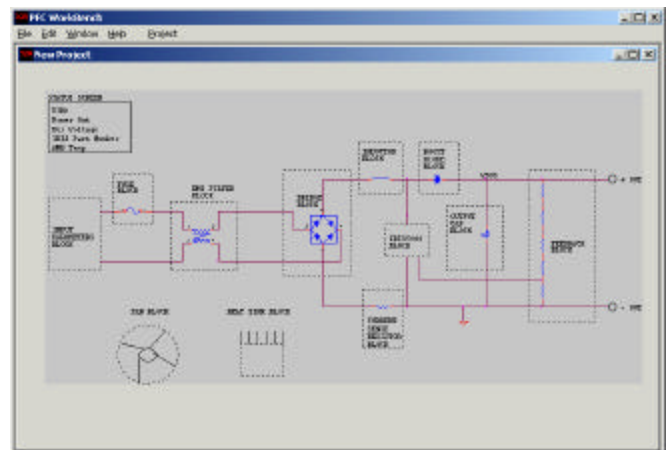
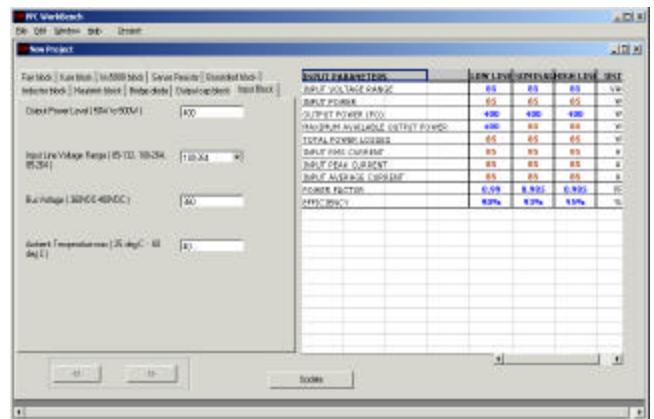
SINGLE CYCLE CONTROL DESIGN PROCEDURE

- ?? Design/select power circuit components
- ?? Design/select current sense resistor
- ?? Design voltage error amplifier compensation

Comparing the typical circuit schematics in FIG 8 and 9 it is easy to see why the new “Single Cycle Control” requires a fraction of the design effort compared to the UC3854 solution. Setting up the multiplier and associated control loop circuits is not a trivial task and often requires several iterations due to the interrelated component values in the feedback loop and the multiplier inputs. Once the circuit components are calculated and fully optimized, there still remains the question of layout and the elimination of noise pick up

on the inputs of the multiplier and control loops throughout the full power range of the converter.

With the new “Single Cycle Control” technique, the complexity of the multiplier circuit is eliminated and the implementation of the final circuit only requires entry-level understanding of PFC control design. The simplified design procedure is made even easier through the use of custom design software specifically developed for the new “Single Cycle Control” IC’s. Below are typical screen shots of the design software developed for the controller.



IX. SINGLE-CYCLE CONTROL POTENTIAL

The proprietary SCC PFC opens up an exciting array of possibilities for application developments.

The SCC unit can be teamed up with power switches from several different technologies to achieve the optimum tradeoff between high performance and cost effectiveness. For example, at 100kHz, the most cost effective (\$/Amp) device for hard switching PFC is an IGBT. If higher efficiencies are required, then HEXFET power MOSFETs or next-generation SuperJunction MOSFETs can be used. It should be noted that - as SCC uses a CCM PFC technique - the choice of boost diode (whether standard low cost ultrafast Si or new SiC devices) plays a major effect on PFC efficiency (due to the energy reflected into the PFC power switch).

The SCC technique may be frequency-tuned for a wide variety of application cost and form-factor design parameters. For example, the SCC can be tuned to operate at 70kHz for immediate and easy use in existing low density PFC or the frequency may be increased to several hundreds of kHz to take full advantage of the higher frequency diode and MOSFET technologies, thereby reducing the size / increasing the power density of the application.

The ease-of-design benefits (as shown in sections VII and VIII) are complemented by massive reductions in component count and pcb space required for SCC vs. the earlier PFC solutions. In the UC3854 comparison, SCC requires 75% fewer components and takes 75% less pcb space. These major savings also come to light when comparing SCC vs. low cost DCM PFC designs. In a 100W DCM design, the comparison resulted in savings of 60-65% in components and board space when using SCC.

In summary, the paper has shown that the features of SCC (design simplicity, component count reduction and minimized pcb space) do indeed enable the higher performance of the CCM topology with the system cost benefits typically associated with DCM PFC.

X. REFERENCES

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2. P.Todd. "UC3854 Controlled Power Factor Correction Circuit Design". Unitrode Application Note.
3. Z.Lai & K.Smedley. "A Family of Power-Factor-Correction Controllers". APEC'97, New York. IEEE 1997