New Snubbers with Energy Recovery into a Local Power Supply

Gregory Ivensky[1], Ilya Zeltser[2] and Sam Ben-Yaakov[1*]

[1]Power Electronics Laboratory, Department of Electrical and Computer Engineering
Ben-Gurion University of the Negev, P. O. Box 653, Beer-Sheva 84105, ISRAEL.
Phone: +972-8-646-1561; Fax: +972-8-647-2949; Email: sby@ee.bgu.ac.il
Website: www.ee.bgu.ac.il/~pel

[2]Green Power Technologies Ltd., 12 Hamada St., Industrial Park T.M.R., Rehovot 76703, ISRAEL.
Phone: + 972-8-9360963; Fax: + 972-8-9360964; Email: ilyaz@g-p-t.com

***Abstract* - The general attributes governing the design of Local Power Supplies (LPS) circuits that are piggybacked on a lossless turn off snubbers are highlighted and analyzed. Based on the proposed general principles, new LPS circuits are presented. They are incorporated as part of a lossless turn-on/turn-off snubber. The proposed snubber/LPS topologies serve two important functions: they help to achieve soft switching of the main switch and main diode at turn-on and turn-off and provide low voltage power source for the auxiliary circuitry such as IC controllers. Since all the switching processes are soft and the reactive energy is recycled (or outputted by the LPS), the losses of the main switch and main diode are significantly reduced. The theoretical analysis of the proposed circuits was verified by simulation and experimental results.**

I. INTRODUCTION

Passive lossless snubbers that are incorporated in high frequency converters can also operate as a Local Power Supply (LPS) [1-4]. This can be accomplished by harvesting some of the energy stored in the reactive elements of such snubbers. Complementing earlier publications, this paper delineates the general attributes governing the design of LPS circuits that are based on passive lossless snubbers. In addition, we propose two versions of a new LPS designed around a passive lossless turn-on/turn-off snubber that has some important advantages. The paper presents a theoretical analysis of the LPS, verified by simulation and experimental results, and develops the design guidelines for it.

II. COMMON PRINCIPLES OF BUILDING LPS/LOSSLESS-SNUBBERS

A LPS that is piggybacked on a lossless snubber includes a storage capacitor C_S and a Zener diode D_Z (Fig. 1). The voltage V_Z across these elements is the output voltage of LPS and is applied to the load R_S. Normally, one of the terminals of voltage stabilizer will be connected to the system's ground.

Lossless turn-off snubbers involve a capacitor C_1 that is used to slow down the dv/dt across the main switch Q. The capacitor C_1 is connected in parallel to the switch Q through a diode D_1. There are two ways for this connection. In the first case (Fig. 1a), the LPS elements C_S, D_Z, R_S are placed in

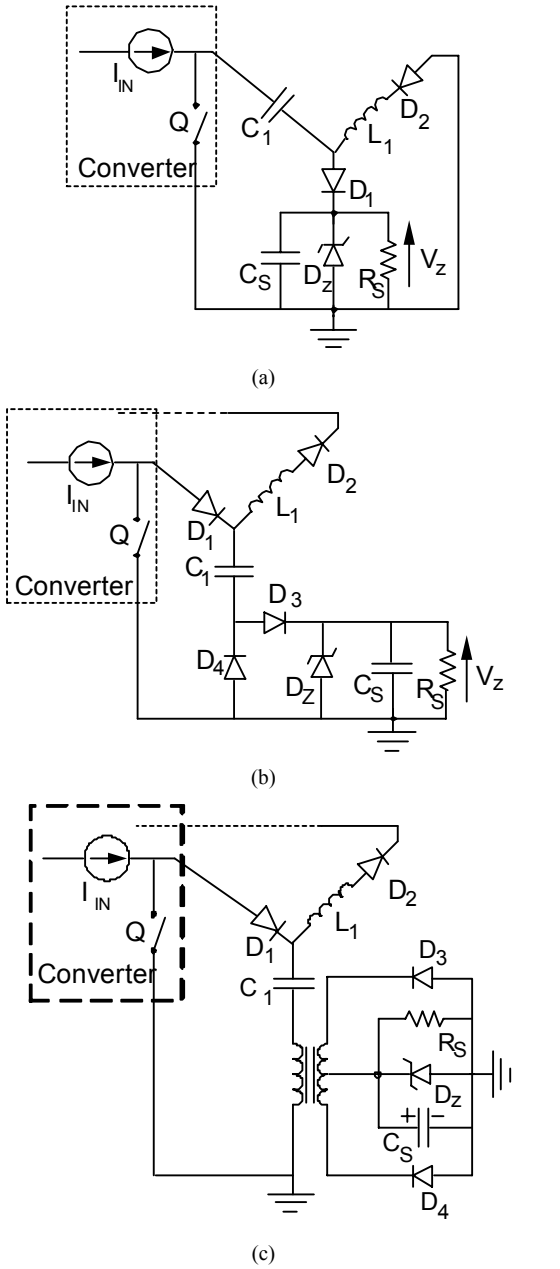

Fig. 1. Combining a LPS and a lossless snubber. (a) Earlier version, (b) Proposed configuration, (c) A isolated version of LPS.

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series with snubber diode D_1, and the reset of C_1 is carried out by an auxiliary resonant circuit (L_1, C_1) [3]. In the second case (Fig. 1b) the discharging of C_1 is initiated by the converter and a second diode (D_4) is used to carry the discharging currents of the snubber capacitor C_1.

The two connections operate equally well as far as slowing down the dv/dt across the switch at turn off. However, they perform differently when coupled to a LPS circuit. The configuration of Fig. 1a generates power that is proportional to the number of voltage transitions per second across the transistor Q since each transition cycle (low to high and high to low) charges and discharges the capacitor C_1. In Continuous Current Mode (CCM) each transition is associated with one switching cycle, so the power delivered to the load is proportional to the switching frequency. In Discontinuous Current Mode (DCM), the number of transitions per second may be larger than the switching frequency due to parasitic ringing across Q. Consequently, excessive and unpredictable power will be fed to the Zener diode, reducing the efficiency and overloading the Zener diode. In contrast, the power generated by the circuit of Fig. 1b is proportional to the switching frequency since the discharge of C_1 is via L_1 that is operated once per switching period (see Section III). Consequently, the power delivered to the LPS in Fig. 2b is constant (for a constant switching frequency case) and therefore this configuration has a substantial advantage over that of Fig. 1a.

In the followings, we demonstrate how the LPS of Fig. 1b can be added to a lossless turn-on/turn-off snubber. A unique feature of the proposed LPS/lossless-snubber system is the fact that is does not require an extra inductor to reset the charge pump capacitor of the LPS (L_1 in Fig. 1b), since it applies the inductor that is already incorporated in the original turn off snubber.

In the LPS topologies described above, the output circuit of the LPS is not isolated from the converter circuit. If isolation is needed, a transformer could be connected between the converter and LPS circuits (Fig. 1c).

III. The Proposed LPS Based on a Turn-On/Off Snubber

The design of the new LPS (Fig. 2) follows the principles of the general topology shown in Fig. 1b. It is assumed here that the basic snubber is connected in a boost converter. The LPS is incorporated into the original lossless turn-on/turn-off snubber [4 - 6] by adding the elements C_S, D_Z, R_S, D_3, D_4 to the original configuration.

The simulated waveforms of the voltage v_Q across the main switch Q, the current i_{C1} of the capacitor C_1, and the current through diodes D_3 and D_4 are depicted in Fig. 3; equivalent circuits for different time intervals are presented at Fig. 4. Considering these circuits, the analysis is developed under the following main assumptions: the switch and diodes are ideal; the input inductance of the converter L_{in} and the output capacitances of the converter (C_O) and of the LPS (C_S) are infinitely large.

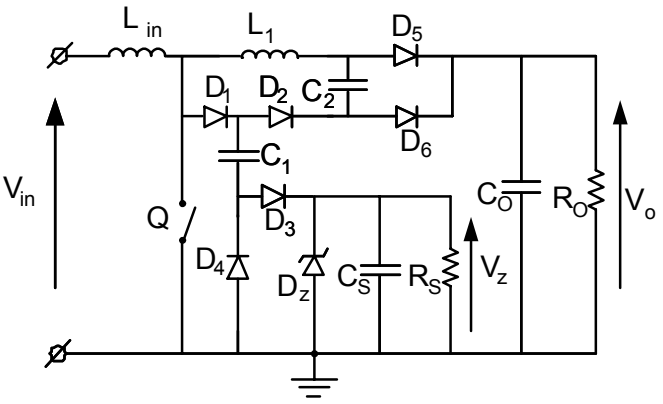

Fig. 2. The proposed LPS combined with a turn on/off snubber.

Prior to instant t_0, the input current of the converter I_{in} flows through the turned on switch Q. At t_0, the switch Q is turned off and the current I_{in} is forced to flow through D_1, C_1, D_3 and the parallel circuit C_S, D_Z, R_S charging the capacitors C_1 and C_S (Fig. 4a). The sum of the LPS output voltage V_Z and of the rising voltage across the capacitor C_1 is applied to the switch Q:

$$v_Q = V_Z + \frac{I_{in}}{C_1}(t - t_0) \tag{1}$$

This provides a pseudo Zero Voltage Switching (ZVS) operation by slowing down the rate at which the voltage across Q rises:

$$\frac{dv_Q}{dt} = \frac{I_{in}}{C_1} \tag{2}$$

Equations (1), (2) neglect the output capacitance of the switch Q. In practical realizations, the physical power MOSFET will have a large output capacitance at low voltages. Consequently, one will not expect a voltage step at t_0 and the initial dv/dt will be lower than expressed in (2).

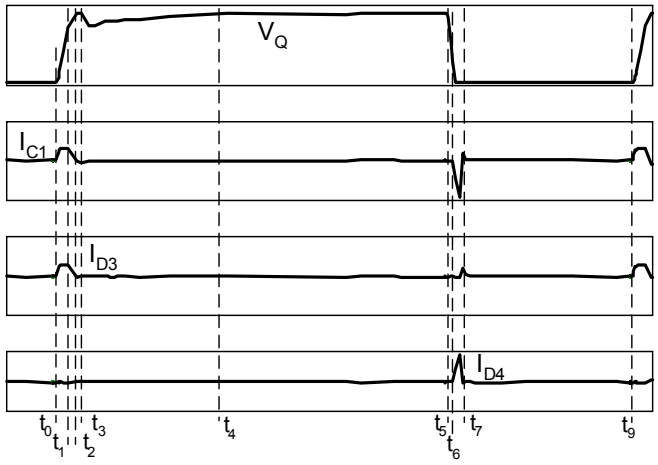

Fig. 3. Key waveforms of proposed LPS/lossless snubber.

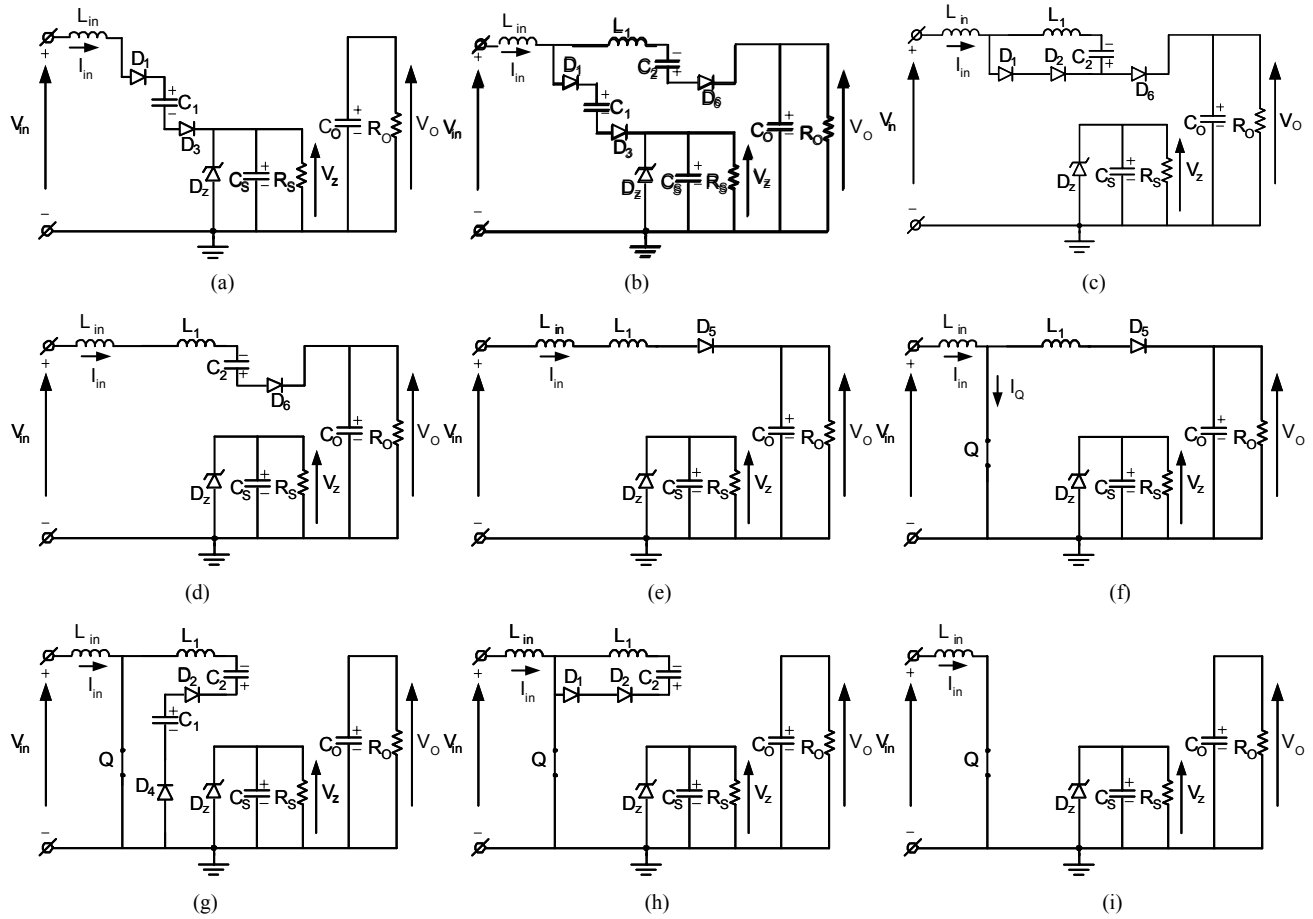

Fig. 4. Equivalent circuits of the proposed LPS/lossless snubber for different time intervals: (a) t_0-t_1, (b) t_1-t_2, (c) t_2-t_3, (d) t_3-t_4, (e) t_4-t_5, (f) t_5-t_6, (g) t_6-t_7, (h) t_7-t_8, (i) t_8-t_9.

Simultaneously with the increase of v_Q, the voltage across the diode D_6 is also rising:

$$v_{D6} = v_Q + v_{C2} - V_o \tag{3}$$

(v_{C2} is the voltage across the capacitor C_2). At the instant t_1 the instantaneous voltage v_{D6} across diode D_6 becomes positive turning it on. The switch voltage at t_1 can be found from (3) assuming that $v_{D6} = 0$:

$$(V_Q)_{t1} = V_o - (V_{C2})_{t1} \tag{4}$$

The charging process of C_1 and C_S continuous after the instant t_1, but part of the input current I_{in} flows now through capacitor C_2 and diode D_6 into the converter load circuit (Fig 4b)

$$i_{C2} = i_{D6} = I_{in}\frac{C_2}{C_1 + C_2}\{1 - \cos[\omega_r(t - t_1)]\} \tag{5}$$

where ω_r is the resonant frequency of the loop including L_1, C_1 and C_2:

$$\omega_r = \frac{1}{\sqrt{L_1\dfrac{C_1C_2}{C_1 + C_2}}} \tag{6}$$

Therefore, the charging current of the capacitor C_1 ($i_{C1} = i_{D3}$) during the interval t_1-t_2 is lower than I_{in}:

$$i_{C1} = i_{D3} = I_{in}\frac{C_1}{C_1 + C_2} + I_{in}\frac{C_2}{C_1 + C_2}\cos[\omega_r(t - t_1)] \tag{7}$$

In practical applications, capacitance C_1 would be much smaller than C_2 (see (25) below) and therefore (5) and (7) can be simplified to:

$$i_{C2} = i_{D6} \approx I_{in}\{1 - \cos[\omega_r(t - t_1)]\} \tag{8}$$

$$i_{C1} = i_{D3} \approx I_{in}\cos[\omega_r(t - t_1)] \tag{9}$$

The switch voltage after t_1 is obtained from (4) and (9):

$$v_Q = V_Z + v_{C1} = V_o - (V_{C2})_{t1} + \frac{I_{in}}{\omega_r C_1}\sin[\omega_r(t - t_1)] \tag{10}$$

The charging process of C_1 and C_S ends at the instant t_2 when the rising switch voltage v_Q reaches the value of the output voltage of the converter V_o:

$$(V_Q)_{t2} = V_o \tag{11}$$

At this instant the diode D_2 turns on and the diode D_3 turns off.

During the interval t_2-t_3 the resonant current (via C_2, L_1) discharges capacitor C_2 through the conducting diodes D_1 and D_2 (Fig. 4c). Consequently, the switch Q will be clamped to V_o via diodes D_1 and D_2. At t_3 the discharging current of capacitor C_2 reaches the value of the converter's input current I_{in} and the diodes D_1 and D_2 turn off. During the next interval t_3-t_4 the input current of the converter I_{in} flows through inductor L_1, capacitor C_2 and diode D_6 (Fig. 4d). The switch voltage v_Q is here lower than V_o due the voltage drop across L_1 and C_2. This capacitor is discharging and its voltage reverses at t_4. As a result, at t_4 the main diode of the converter D_5 turns on and diode D_6 turns off. The duration of the interval t_0-t_4 defines the maximum value of the duty cycle. The interval t_4-t_5 (Fig. 4e) corresponds to the normal off state of the converter. It ends at t_5 when the switch Q is turned on.

During the time interval t_5-t_6 (Fig. 4f) the switch current i_Q is rising smoothly under the action of the output voltage of the converter (V_o) and the inductance L_1 (Zero Current Switching):

$$i_Q = \frac{V_o}{L_1}(t - t_5) \tag{12}$$

The current of the main diode D_5 is obtained by:

$$i_{D5} = I_{in} - i_Q \tag{13}$$

This current is positive during the first part of the interval t_5-t_6 and negative (reverse recovery current) during its remaining part. At the instant t_6, when the reverse recovery current of D_5 reaches a value of I_{Rm}, diode D_5 turns off. At the same time, diodes D_2 and D_4 turn on and initiate the discharging circuit of the capacitor C_1. This circuit includes the capacitor C_2, the inductor L_1 and the turned on switch Q (Fig. 4g). The discharging current i_{C1} and the capacitor C_1 voltage v_{C1} can be described by following approximate equations (taking into account that $C_1 \ll C_2$):

$$i_{C1} \approx (V_o - V_Z)\omega_r C_1 \sin[\omega_r(t - t_6)] + I_{Rm}\cos[\omega_r(t - t_6)] \tag{14}$$

$$v_{C1} \approx (V_o - V_Z)\cos[\omega_r(t - t_6)] - \frac{I_{Rm}}{\omega_r C_1}\sin[\omega_r(t - t_6)] \tag{15}$$

where I_{Rm} is the peak reverse recovery current of D_5.

At t_7, the polarity of v_{C1} is reversing, turning on diode D_1 and turning off diode D_4. The current of the loop L_1-C_2 flows through diodes D_1 and D_2 (Fig. 4h) up to the instant t_8 when the diodes D_1 and D_2 turn off. The next time interval (Fig. 4i) continuous up to the instant t_9 when a new period begins and the switch Q is turned off again (as at the instant t_0).

The charge transferred to the LPS during each switching period is:

$$Q_{ch} = C_1(V_o - V_Z) \tag{16}$$

Since this charge is injected f_s times per second, the input power of the LPS P_{Sin} will be:

$$P_{S.in} = f_S C_1 (V_o - V_Z) V_Z \tag{17}$$

where f_S is the operating frequency of the main switch.

Note that (17) is valid when:

$$I_{D3av} \geq \frac{V_Z}{R_S} \tag{18}$$

otherwise, the Zener diode will not conduct and the output voltage of LPS will be lower than V_Z.

Under condition (18), the following equations describe the output power of LPS $P_{S.out}$ and the Zener diode current I_Z:

$$P_{S.out} = \frac{V_Z^2}{R_S} \tag{19}$$

$$I_Z = \frac{P_{S.in} - P_{S.out}}{V_Z} \tag{20}$$

To maintain soft switching, the capacitance of C_1 should be as large as practical. On the other hand, large C_1 increase the charging and discharging intervals t_0-t_2 and t_6-t_7 and, as a result decreases the maximum duty cycle

$$D_{max} = 1 - f_S(t_4 - t_0) \tag{21}$$

and increases the minimum duty cycle

$$D_{min} = f_S(t_8 - t_5) \tag{22}$$

There is also another limitation of C_1: the charging current $i_{C1}=i_{D3}$ (interval t_1-t_2) should not reach zero value before the switch voltage v_Q reaches V_o. Otherwise C_1 will not reset and, consequently, soft switching will be lost. The maximum permissible capacitance to maintain soft switching is found from (6), (9), (10):

$$C_{1max} \cong \frac{I_{in}^2}{(V_{C2})_{t1}^2} L_1 \tag{23}$$

The voltage across the capacitor C_2 at the instant t_1 $(V_{C2})_{t1}$ can be obtained from the energy balance considerations. The energy stored in C_2 at t_1 has two components: one of them is the energy which was stored by capacitor C_1 during the charging interval t_0-t_2 of preceding cycle, and the second part is the energy stored by inductor L_1 at the instant t_6 when the main diode D_5 turned off. Since both energy components are transferred into capacitor C_2 during the interval t_6-t_8 we find:

$$\frac{C_2(V_{C2})_{t1}^2}{2} = \frac{C_1(V_o - V_Z)^2}{2} + \frac{L_1 I_{Rm}^2}{2} \tag{24}$$

Inserting $(V_{C2})_{t1}$ from (24) into (23) and assuming that the reverse current is limited by L_r to be $I_{Rm} \approx I_{in}$, and assuming $C_1 \ll C_2$, we find that the effect of the reverse recovery current of the main diode D_5 on the value of C_{1max} capacitance is negligibly small. Ignoring this effect, we obtain:

$$C_{1max} \cong \frac{I_{in}}{V_o - V_Z}\sqrt{L_1 C_2} \tag{25}$$

IV. Improved LPS/lossless-snubber

As (17) shows, the input power P_{Sin} of the proposed LPS is constant. Hence, under a LPS load decrease, the extra power will shift to the Zener diode (19), (20) and may cause overheating. This problem can be alleviated if P_{Sin} is regulated. An extra switch Q_{ex}, connected in series with diode D_4 and operated at a lower frequency in PWM mode, can be used to control P_{Sin} [3]. However, such solution will suspend the turn off snubbing process. To overcome this ill effect of the extra switch Q_{ex}, the addition of a diode D_{ad} and an extra snubbing capacitor C_{ad} is proposed (Fig. 5). This capacitor can also be added whenever the charge pump capacitor of the LPS is insufficient for achieving the desired dv/dt.

V. Simulation and Experimental Results

The operation of the proposed snubber was tested by simulation (Fig. 3) and hardware implementation. The experimental boost converter with LPS followed the topology (Fig. 2) with one difference: the input inductor L_{in} was taped (turns ratio 7:1) [7]. The main switch was a MOSFET transistor (IRFP460) and diodes were of the following types: STTA5 (D_1, D_2, D_6), MURS160T3 (D_3), MBRS130LT3 (D_4), U860 (D_5) and SMBJ4744 (Zener diode D_Z, nominal voltage V_Z=15V). Capacitances and inductances were of the following values: C_1 =1.8nF, C_2 =0.22uF, C_O=1mF, C_S=100uF, L_{in} =1.2mH, L_1 =3.6uH, load resistance of LPS R_S = 250Ω. The experimental conditions were: power level= 1kW; output voltage = 400V; switching frequency 105kHz. The converter was fed from an ac source of 230Vrms through a bridge rectifier. The output power and voltage of the LPS were 0.9W, 15V respectively. The input power was 1.09W and the Zener current was 13mA.

Typical experimental waveforms are presented in Figs. 6 - 8. The experimental waveforms of the switch voltage v_Q and charge pump capacitor current i_{C1} (Fig. 6) practically coincide with the simulated waveforms (Fig. 3). The interval t_0-t_4 limiting the maximum duty cycle D_{max} (21) is clearly seen on these experimental and simulated waveforms. The experimental switch voltage and switch current waveforms at turn-off (Fig. 7) and turn-on (Fig. 8) confirm that both switching processes are soft.

Note that the experimental slope of the switch voltage at turn-off (2.7V/ns, Fig. 7) is somewhat lower than the expected theoretical slope (3.9V/ns) according to (2). This discrepancy has been explained as follows: (2) does not take into account the capacitance of the switch C_{ds}. Applying the measured slope, this capacitance is calculated to be:

$$C_{ds} = C_1\left(\frac{\left(dv_Q/dt\right)_{eq.(2)}}{\left(dv_Q/dt\right)_{exper.}} - 1\right) = 1.8\times\left(\frac{3.9}{2.7} - 1\right) = 0.8\text{nF} \qquad (26)$$

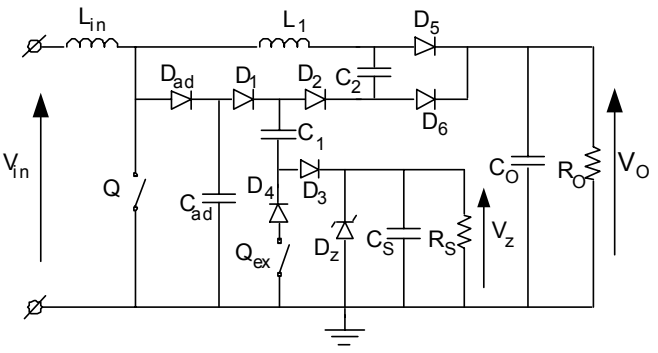

Fig. 5. The improved LPS/lossless snubber topology.

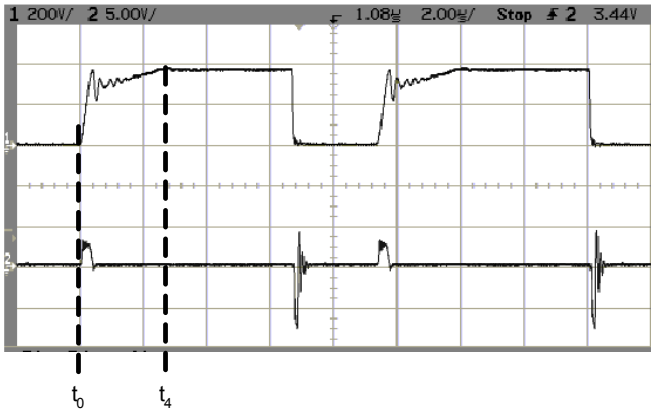

Fig. 6. Switch voltage v_Q (upper trace, 200V/div) and charge pump capacitor current i_{C1} (lower trace, 5A/div) of the experimental LPS/lossless snubber. Horizontal scale- 2us/div.

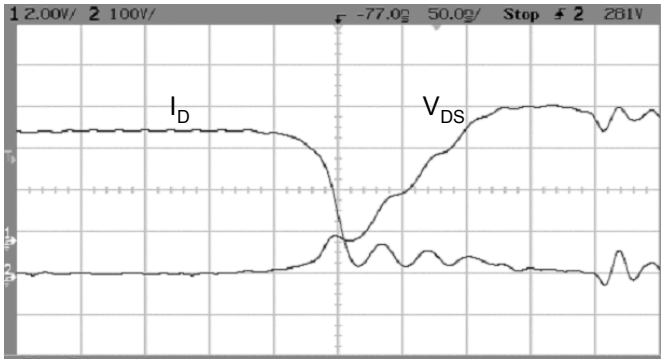

Fig. 7. Switch current, I_D(Q) - 2A/div and switch voltage V_{DS}(Q) - 100V/div of the experimental LPS/lossless snubber at turn-off. Horizontal scale - 50ns/div.

VI. Discussion and Conclusions

The proposed LPS/lossless-snubber topologies serve two important functions: they help to achieve soft switching of the main switch and main diode at turn on and turn off and provide a low voltage power source for the auxiliary circuitry such as IC controllers. Since all the switching processes are

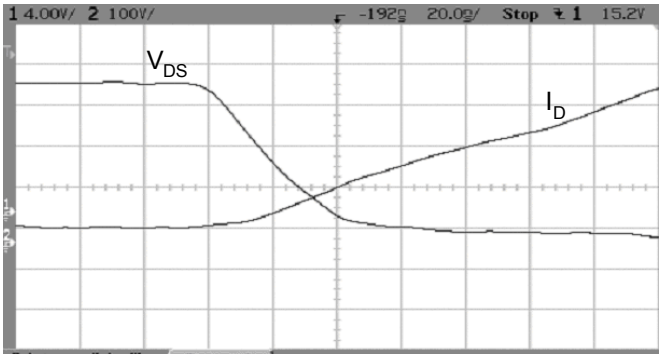

Fig. 8 Switch current, I_D(Q) - 4A/div and switch voltage V_{DS}(Q) - 100V/div of the experimental LPS/lossless snubber at turn-on. Horizontal scale - 20ns/div.

soft, and the reactive energy is recycled (or outputted by the LPS) the losses of the main switch and the main diode are significantly reduced. The proposed LPS/lossless-snubber topologies have important advantages over similar circuits described earlier:

1. They do not need an additional inductor.
2. The Zener diode current of the improved LPS/lossless-snubber is practically constant under both CCM and DCM operating conditions.
3. Soft switching at turn-on can still be maintained even if a regulating switch is included to control the power flow to the LPS.

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