# Implementing NCP1207 in QR 24W AC/DC Converter with Synchronous Rectifier

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## Introduction

The NCP1207 is a controller dedicated for driving the current-mode free running quasi-resonant flyback offline converter.
This converter can provide supply for consumer products like notebooks, offline battery charger, consumer electronics (DVD players, Set-Top Boxes, TVs), etc.
The growing interest for EMI pollution reduction, efficiency improvement and maximum safety has been taking into account while designing the NCP1207.

By implementing the NCP1207 one can build a power supply that can meet all those requirements. This can be achieved with help of the following NCP1207 main features:

- **Current-Mode Control:** cycle-by-cycle primary current observation is helping to prevent any significant primary over-current which would cause transformer's core saturation and consequent serious power supply failure.
- **Critical Mode Quasi-resonant Operation:** prevent the converter operation in Contionuous Conduction Mode in any input and output condition. It is provided by the zero crossing detection of the auxiliary winding's voltage.
By addition of the reasonable delay the switch turn-on instant can shifted to the minimum (valley) of drain voltage. This improves EMI noise and efficiency.
- **Dynamic Self-Supply:** ensures IC proper operation in applications where the output voltage varies during operation like battery chargers. The DSS also supplies the IC when the Over-voltage event is being latched and converter operation is stopped.
- **Over-Voltage Protection:** by sampling the plateau voltage on the auxiliary winding, the NCP1207 enters into latched fault condition whenever the over-voltage is detected. The controller stays fully latched until the Vcc decreases bellow 4.0 V, e.g. when the user unplugs the power supply from the mains outlet and re-plugs it. The OVP threshold can be adjusted externally.
- **Over-Load Protection:** by continuously monitoring the feedback loop activity, NCP1207 enters hic-up operation as soon as the power supply is overloaded. As soon as overload condition disappears, the NCP resumes operation.

## The 24W AC/DC Adaptor Board Specification

The adaptor has following maximum and performance ratings.

| | |
|---|---|
| Output Power | 24 W |
| Output Voltage | 12 VDC |
| Output Current | 2 A |
| Min. Input Voltage | 180 VAC |
| Max. Input Voltage | 240 VAC |
| Max. Switching Frequency | 70 kHz |

The schematic diagram of the adaptor can be seen from **Figure 1**.

## Transformer Design

The bulk capacitor voltage than can be calculated:

$$V_{bulk-min} = V_{AC-min}\sqrt{2} = 180 \cdot \sqrt{2} = 255\text{VDC}$$

$$V_{bulk-max} = V_{AC-max}\sqrt{2} = 240 \cdot \sqrt{2} = 339\text{VDC}$$

The requested output power is 24 Watts.
Assuming 87% efficiency the input power is equal to:

$$P_{in} = \frac{P_{out}}{\eta} = \frac{24}{0.87} = 27.6\text{W}$$

The average value of input current at minimum input voltage is:

$$I_{in-avg} = \frac{P_{in}}{V_{bulk-min}} = \frac{27.6}{255} = 108\text{mA}$$

Taking into account no presence of any clamping network the suitable reflected primary winding voltage for 800V rated MOSFET switch is:

$$V_{flbk} = 800\text{V} - V_{bulk-max} - V_{spike} = 800 - 339 - 330 = 131\text{V}$$

Using calculated flyback voltage the maximum duty cycle can be calculated:

$$\delta_{max} = \frac{V_{flbk}}{V_{flbk} + V_{bulk-min}} = \frac{131}{131+255} = 0.339 = 0.34$$

Following equation determines peak primary current:

$$I_{ppk} = \frac{2 \cdot I_{in-avg}}{\delta_{max}} = \frac{2 \cdot 108 \cdot 10^{-3}}{0.34} = 635\text{mA}$$

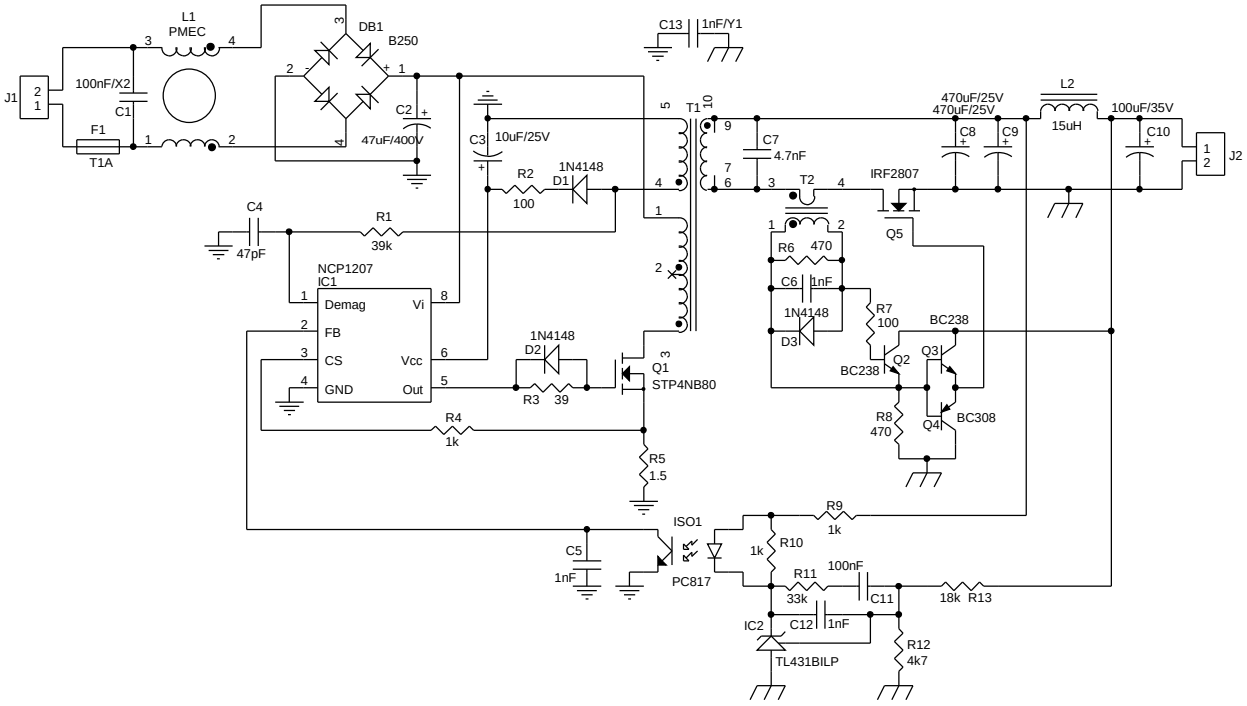


**Figure 1. Schematic Diagram of the QR 24W AC/DC Converter with NCP1207 and Synchronous Rectifier**

The maximum switching frequency at minimum input voltage is 70 kHz. Taking into account quasi-resonant (QR) and valley switching operation of the NCP1207 the QR time interval from the instant of the total core demagnetization to the valley of switch's drain voltage needs to be taken into account when calculating the switch max. ON-time interval. Using QR time of 2 µs appropriate for 70 kHz switching frequency the ON-time can be calculated as follows:

$$t_{ON} = \left(\frac{1}{f_{sw}} - t_{QR}\right) \cdot \delta_{max} = \left(\frac{1}{70 \cdot 10^3} - 2 \cdot 10^{-6}\right) \cdot 0.34 = 4.177\mu s = 4.18\mu s$$

The EF25 core for transformer was selected. It has cross-section area $A_e$=52.5mm$^2$. The N67 ferrite material allows to use maximum operating flux density $B_{max}$=0.25T.
The number of turns for the primary winding is:

$$n_p = \frac{V_{bulk-min} \cdot t_{ON}}{B_{max} \cdot A_e} = \frac{255 \cdot 4.18 \cdot 10^{-6}}{0.25 \cdot 52.5 \cdot 10^{-6}} = 80 turns$$

The primary inductance can be calculated as follows:

$$L_p = \frac{V_{bulk-min}}{I_{ppk}} \cdot t_{ON} = \frac{255}{0.635} \cdot 4.18 \cdot 10^{-6} = 1.68 mH$$

The $A_L$ factor of the transformer's core can be calculated as follows:

$$A_L = \frac{L_p}{(n_p)^2} = \frac{1.68 \cdot 10^{-3}}{(80)^2} = 263 nH$$

Since skin effect and eddy currents plays significant role for flyback topology at given switching frequency the Litz wire is used. It consists of 4 wires each with diameter 0.12mm.
To reduce the leakage inductance the primary winding is split to two windings each with half number of turns. The secondary winding is inserted between those halves primary windings. This is well known as a sandwich arrangement.

For an output voltage of 12V, the number of turns of the secondary winding can be calculated accounting synchronous rectifier as follows:

$$n_s = \frac{V_s (1 - \delta_{max}) n_p}{\delta_{max} \cdot V_{bulk-min}} = \frac{12 \cdot (1 - 0.34) \cdot 80}{0.34 \cdot 255} = 7.3 = 8 turns$$

The secondary winding is again made with Litz wire. It consists of 24 wires each with diameter 0.22mm.
Using the result above the number of turns for auxiliary winding can be calculated as follows:

$$n_{aux} = \frac{(V_{aux} + V_{fwd})}{V_s} \cdot n_s = \frac{(12+1)}{12} \cdot 8 =$$

$$8.67 = 9\text{turns}$$

A single wire of 0.15 mm diameter was used for auxiliary winding.

The windings arrangement of the transformer is following:

1. auxiliary
2. 1-st half primary
3. secondary
4. 2-nd half primary

**Primary Current Control**

Primary current control path consist of sensing resistor R5, skipping resistor R4 and pin 3 of the IC named CS. The maximum voltage threshold on CS pin is about 1V. The value of the current sense resistor R5 is given by:

$$R_5 = \frac{V_{TH-max}}{I_{ppk}} = \frac{1}{0.635} = 1.57\Omega = 1.5\Omega$$

The skipping resistor R4 value together with the internal 200 μA current source gives the skipping voltage level. It is decided to set skipping level to 20% of the maximum primary current. I this case the skipping voltage is 0.2 V.
The value of the skipping resistor R4 is:

$$R_4 = \frac{V_{CS-skip}}{I_{int}} = \frac{0.2}{200 \cdot 10^{-6}} = 1\text{k}\Omega$$

**Demagnetization Detection and OVP**

The transformer demagnetization sensing is based on the zero crossing detection of the auxiliary winding's voltage. For this purpose the zero crossing detector built-in the NCP1207 is connected to pin 1. Resistor R1 limits the current flowing through the pin1 voltage clamps. Also this resistor together with capacitor C4 delays the zero voltage crossing to tune the switch's turn-on to an instant when the switch's drain voltage is at its minimum level (valley).
Resistor R1 has also another function. Together with internal resistor divider and comparator with reference voltage forms an over-voltage protection circuit. The pin1 has connected internally a resistor of 30 kΩ to ground. If the voltage on that pin reaches roughly 7.2 V an over-voltage latch is triggered and converter operation is blocked until input supply plug is disconnected. The value of resistor R1 then can be calculated as follows:

$$R_1 = 30 \cdot 10^3 \cdot \left( \frac{V_{CC-max}}{7.2} - 1 \right) =$$

$$30 \cdot 10^3 \cdot \left( \frac{15.5}{7.2} - 1 \right) = 34.6\text{k}\Omega = 39\text{k}\Omega$$

The value of the delaying capacitor C4 is a result of tuning process on the real board.

**Synchronous Rectifier**

The synchronous rectifier consists of following basic blocks: sensor of secondary current, gate driver and MOSFET switch. A current transformer T2 senses the output rectifier current. The current transformer has its primary winding located in series with the secondary switch within the secondary current loop. Resistor R6 loads the secondary winding of the current transformer. The resistor R6 converts the current into a voltage. That voltage is filtered and limited by capacitor C6 and diode D3.That voltage is delivered to the gate driver, which consists of transistors Q2, Q3 and Q4 and pull-down resistor R8.
For the current transformer the ring core R10 was selected. It has cross-section area $A_e$=7.83mm$^2$. The N30 magnetic allows to use maximum operating flux density $B_{max}$=0.2T. The appropriate number of turns than can easily wound on that core is around 20. The maximum demagnetization time of the converter's transformer can be calculated as follows:

$$t_{dem} = \frac{n_{cs-se} \cdot B_{max} \cdot A_e}{V_{clamp}} = \frac{20 \cdot 0.2 \cdot 7.83 \cdot 10^{-6}}{0.7} =$$

$$45\mu\text{s}$$

This value is bigger than maximum operating demagnetization time. It means that the current transformer has enough freedom to work properly even if the converter is overloaded or during the start-up sequence when the demagnetization time is longer due to lower output voltage.

**Feedback Loop**

The feedback loop is based on the secondary side to ensure good output voltage regulation. The control TL431 has internal reference voltage of 2.5V. The output voltage of the converter is divided by the resistors R12 and R13. The resistor divider output voltage is compared with internal reference voltage of TL431. With regard to TL431 input leakage current, the resistor

divider's current of 500μA was selected. The resistor R12 then can be calculated as follows:

$$R_{12} = \frac{V_{TL431}}{I_{divider}} = \frac{2.5}{500 \cdot 10^{-6}} = 5k\Omega = 4.7k\Omega$$

The value of the upper resistor R13 of the divider is:

$$R_{13} = R_{12} \cdot \left( \frac{V_{out}}{V_{TL431}} - 1 \right) = 4700 \cdot \left( \frac{12}{2.5} - 1 \right) =$$

$$17860\Omega = 18k\Omega$$

The resistor R10 ensures the minimum current supply of 1mA for TL431 in case of the converter operation near to the maximum output power when current flowing through the LED diode within the optocoupler ISO1 is close to zero. The threshold voltage of the LED is around 1V, the value of the R10 is:

$$R_{10} = \frac{V_{LED}}{I_{TL431}} = \frac{1}{1 \cdot 10^{-3}} = 1k\Omega$$

The resistor R9 limits the current flowing through the LED in case the voltage across the output terminal of the TL431 is at its minimum it means 2.5V. Considering the nominal output voltage 12V and maxim LED current 10mA the value of R9 is:

$$R_9 = \frac{V_{out} - V_{LED} - V_{TL431}}{I_{LED-max}} = \frac{12 - 1 - 2.5}{10 \cdot 10^{-3}} = 850\Omega =$$

$$1k\Omega$$

Resistor R11 together with capacitors C11.C12 creates so called "Pole-Zero" compensation circuit of the feedback loop. Their values are result of feedback loop response measurements and adjustments on the board.
Since NCP1207 allows direct optocoupler connection, the opto-transistor is connected without any pull-up resistor to pin 2. Capacitor C5 bypasses any high frequency current pick-up.

**Primary Switch Snubber Network**

Since any ordinary snubber or clamping network on the primary side is not loss-less a different approach was exploited for snubber. The primary switch is rated for higher breakdown voltage in this case for 800V to cope with voltage spikes. The snubber capacitor C7 is located on the secondary side. This capacitor has two functions. The first purpose is to create together with secondary leakage inductance the resonant tank. Similarly the primary resonant circuit consists of the primary leakage inductance and associated parasitic capacitances. The resonant frequency of the secondary resonant circuit is approximately two times higher than resonant frequency of the primary resonant circuit. This frequency difference efficiently decreases the voltage spike on the primary. The second function of C7 is to protect the secondary switch from voltage spikes.

**Bill of Materials**

| | |
|---|---|
| C1 | 100nF/X2 |
| C2 | 47uF/400V |
| C3 | 10uF/25V |
| C4 | 47pF,ceramic |
| C5 | 1nF,ceramic |
| C6,C12 | 1nF,ceramic |
| C7 | 4.7nF,ceramic |
| C8,C9 | 470uF/25V |
| C10 | 100uF/35V |
| C11 | 100nF,ceramic |
| C13 | 1nF/Y1 |
| DB1 | B250 |
| D1,D2,D3 | 1N4148 |
| F1 | 1A,time-lag |
| IC1 | NCP1207 |
| IC2 | TL431 |
| ISO1 | PC817 |
| L1 | 2*10mH, common mode |
| L2 | 10uH |
| Q1 | STP4NB80 |
| Q2,Q3 | BC238 |
| Q4 | BC308 |
| Q5 | IRF2807 |
| R1 | 39k |
| R2,R7 | 100 |
| R3 | 39 |
| R4,R9,R10 | 1k |
| R5 | 1.5 |
| R6,R8 | 470 |
| R11 | 33k |
| R12 | 4k7 |
| R13 | 18k |
| T1 | transformer, see text |
| T2 | transformer, see text |

**PCB Layout**

Proper printed circuit board layout is essential for good operation of the whole converter. It also influences the EMI both conducted and radiated.
It is important to ensure good grounding technique and keep all high frequency current loop and high voltage areas as small as possible to avoid both magnetic and electric radiation.
An example of the layout can be seen from **Figure 2**.

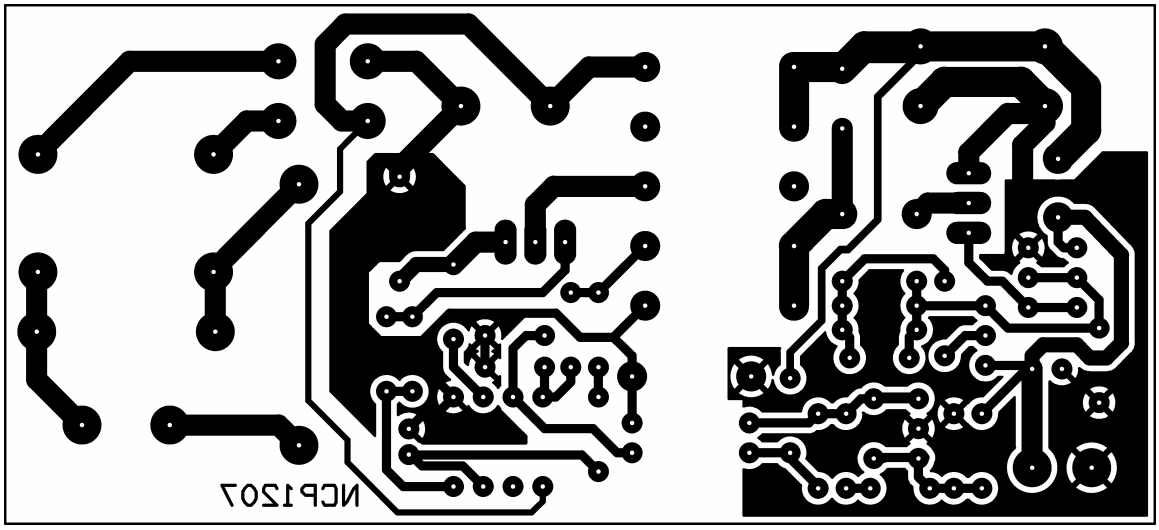


**Figure 2. Printed Circuit Board Layout - Bottom Side**

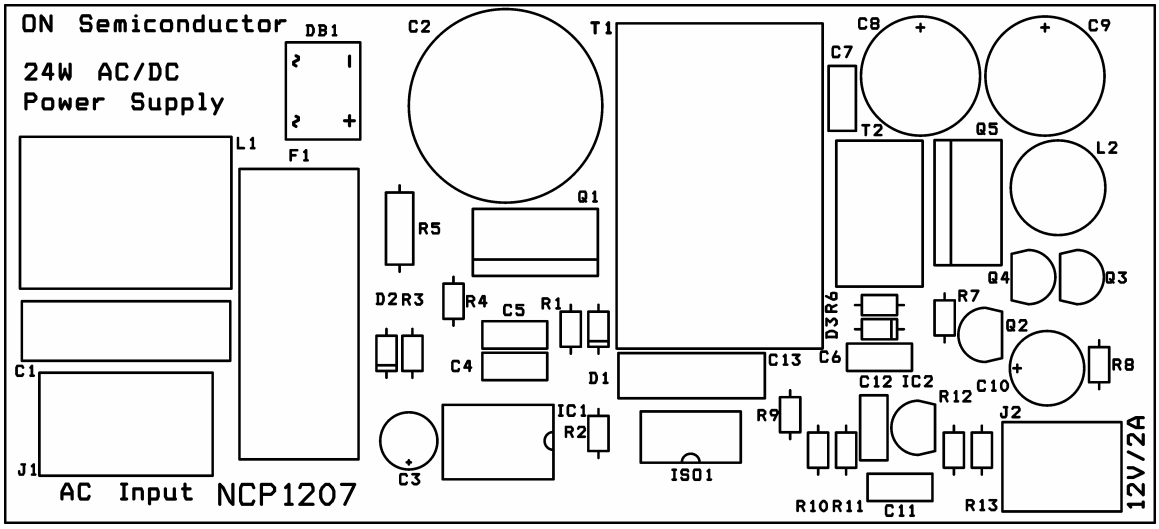


**Figure 3. Printed Circuit Board Layout - Silkscreen Component Side**

The component arrangement can be seen from **Figure 3**. The board size is 97.5*44mm.

**Practical Results**

One of the most important parameter considered during the converter design is the overall power conversion efficiency. For this reason the synchronized output rectifier was utilized. **Table 1** shows the measured results for converter working at minimum specified input voltage 255VDC.

The corresponding graphical representation of the **Table 1** can be seen from **Figure 4**.

**Table 2** shows the similar results for the maximum specified input voltage of 339VDC.

**Figure 5** again helps to see the results belonging to **Table 2**.

The no-load power consumption measured at 255VDC input voltage is about 275mW and at 339VDC is about 385mW.

| Pout [W] | Efficiency. [%] |
|---|---|
| 24 | 91.68 |
| 22 | 91.69 |
| 20 | 91.63 |
| 18 | 91.49 |
| 16 | 91.33 |
| 14 | 90.83 |
| 12 | 90.08 |
| 10 | 89.16 |
| 8 | 87.87 |
| 6 | 85.59 |
| 4 | 81.85 |
| 2 | 77.31 |

**Table 1.Power Conversion Efficiency at 255VDC Input Voltage**

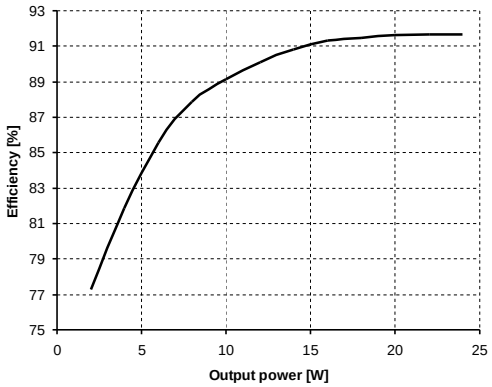


**Figure 4. Power Conversion Efficiency at 255VDC Input Voltage**

| Pout [W] | Efficiency. [%] |
|---|---|
| 24 | 90.70 |
| 22 | 90.56 |
| 20 | 90.42 |
| 18 | 90.28 |
| 16 | 89.76 |
| 14 | 88.97 |
| 12 | 87.85 |
| 10 | 86.39 |
| 8 | 84.75 |
| 6 | 82.16 |
| 4 | 78.20 |
| 2 | 73.62 |

**Table 2.Power Conversion Efficiency at 339VDC Input Voltage**

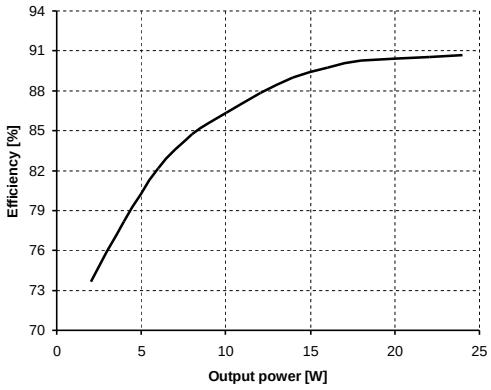


**Figure 5. Power Conversion Efficiency at 339VDC Input Voltage**

Following pictures of the basic voltage waveforms demonstrate the operation of the converter at specific conditions.

**Figure 6** shows in top trace the gate driver voltage and in bottom trace primary switch's drain voltage at full load.

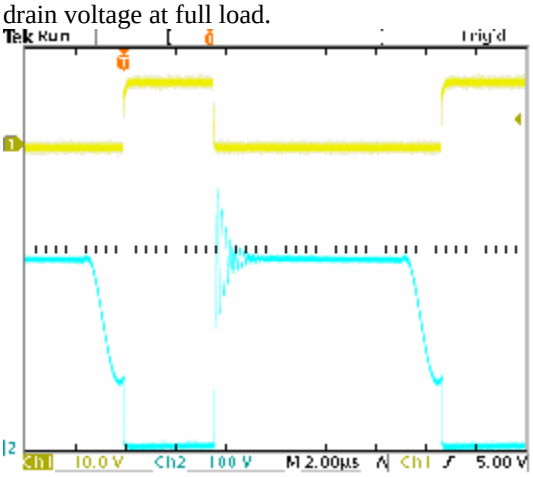


**Figure 6. Gate Driver and Drain Voltage at Full Load**

**Figure 7** shows the same measurement points as in Figure 6 but at medium load condition when the first valley of the drain voltage is being skipped.

**Figure 8** is the same as previous measurements but for light load condition when two valleys are skipped.

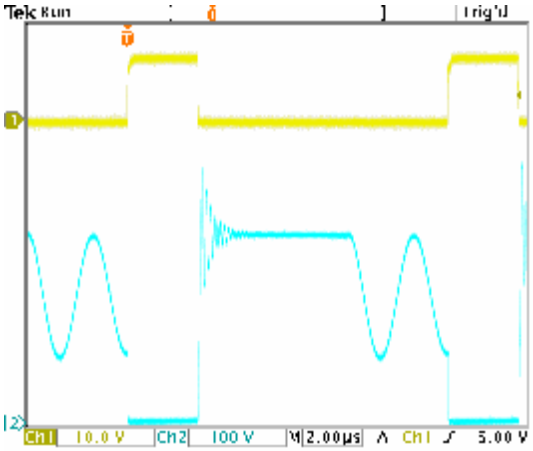


**Figure 7. Gate Driver and Drain Voltage at Medium Load**

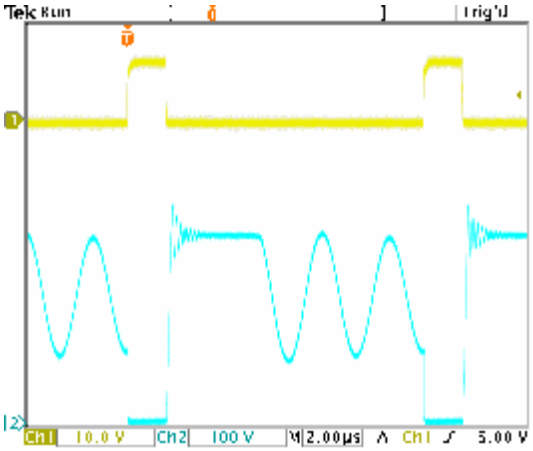


**Figure 8. Gate Driver and Drain Voltage at Light Load**

The cycle skipping operation when the output load is very light is depicted in **Figure 9**.

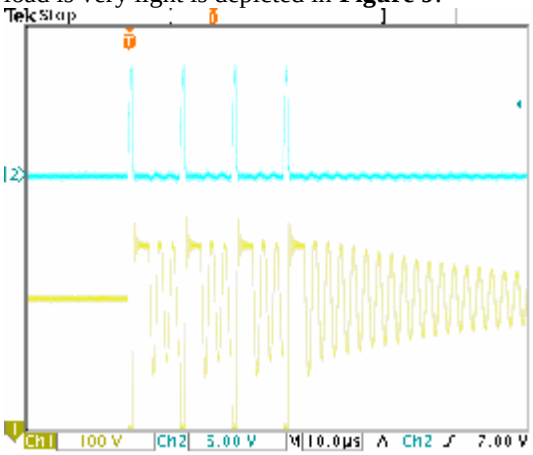


**Figure 9. Gate Driver and Drain Voltage during the Cycle Skipping at Very Light Load**

The waveforms during overload condition is depicted in **Figure 10**.

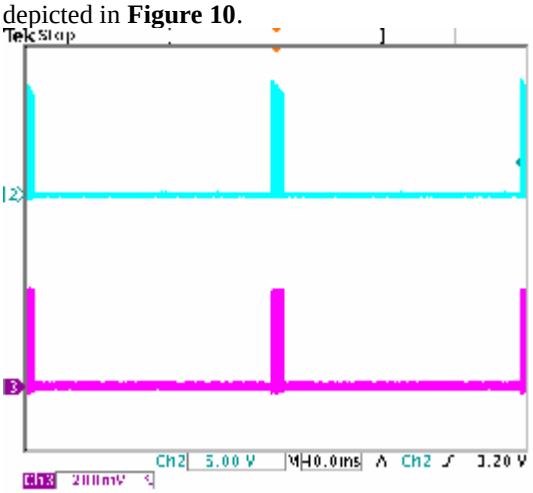


**Figure 10. Gate Driver and Drain Voltage during the Over-Load**

Detailed view of the burst pulse during overload can be seen from **Figure11**. This figure clearly demonstrates the operation of the internal soft-start block.

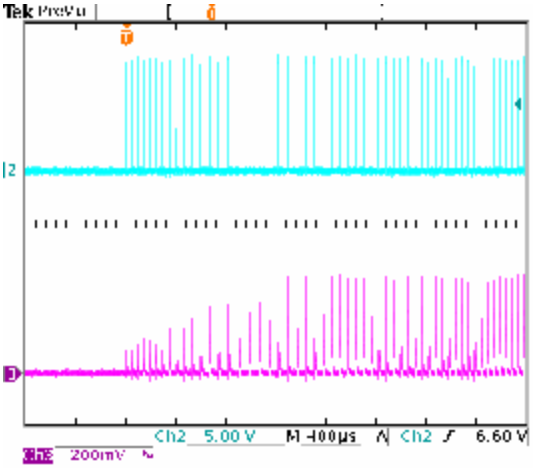


**Figure 11. Detailed View of the Burst Pulse**

The load regulation of the output voltage for load step change from 100% to 10% and vise versa can be seen from **Figure 12**.

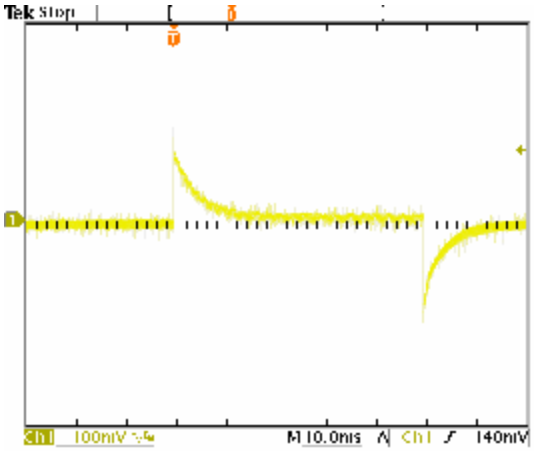


**Figure 11. Load Regulation**