Physical CAD Model for High-Voltage IGBTs Based on Lumped-Charge Approach

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***Abstract*—A new insulated gate bipolar transistor (IGBT) model developed on a physical basis is presented. The Lumped-Charge method has been revised in order to point out a more general methodology for implementing the model into a circuit form. As an example, a version of the model for the popular PSPICE simulator is presented. The N-channel IGBT structure is described by means of an evolution of the PSPICE level-1 metal oxide semiconductor field effect transistor model. An accurate mobility model has been included to precisely predict the voltage drop in the ON state. Simulation results agree well with the experiments both in static and in switching operations. The comparison between the proposed and the native IGBT PSPICE model shows the better behavior of the former. The reasons for this result have been verified by means of two-dimensional MEDICI simulations. Moreover, the proposed model is able to predict the device behavior also in critical operations like its latchup during a turn-off under short-circuit conditions.**

***Index Terms*—Insulated gate bipolar transistor (IGBT) model, Lumped-Charge method, two-dimensional (2-D) MEDICI simulations.**

NOMENCLATURE

A	Device area [cm^2].
$A_{\mathrm{L,IC}}$	Mobility global expression coefficient A.
$\alpha_{\mathrm{L,IC}}$	Mobility global expression coefficient alpha.
α_n^L	Lattice Mobility expression electron coefficient alpha.
$B_{\mathrm{L,IC}}$	Mobility global expression coefficient B.
C_{BCJ}	N^- base-body junction capacitance [F].
C_{CER}	Redistribution capacitance [F].
C_{GD}	Gate-drain MOSFET capacitance [F].
$C_{\mathrm{Jij}}\vert 1\,\mathrm{V}$	Junction i–j capacitance at $V_{\mathrm{REVERSE}} = 1$ V [F].
$C_{\mathrm{L,IC}}$	Mobility global expression coefficient C.
d_{ij}	Distance between nodes i and j [cm].
ϕ_B	Normalization coefficient in the Poisson's equation [V].
ϕ_{ij}	Junction i–j built-in potential [V].
$f_{\mathrm{ij}} = w_i/w_j$	Thickness ratio of the regions which nodes i and j belong to.
ϕ_{J2}	Built-in potential of junction J_2 [V].
ϕ_T	Thermal voltage [V].
I_B	Normalization coefficient in the Poisson's equation [A].
$i_{\mathrm{CONT,i}}$	Continuity current at node i [A].
$i_{\mathrm{n,ij}}$	Electron current between nodes i and j [A].
$i_{\mathrm{p,ij}}$	Hole current between nodes i and j [A].
ℓ	Depletion fraction of the N^- region.
μ_n	Electron mobility [cm^2/(Vs)].
μ_n^{IC}	Carrier carrier scattering and ionized impurity Scattering combined electron mobility [cm^2/(Vs)].
μ_n^L	Lattice electron mobility [cm^2/(Vs)].
μ_p	Hole mobility [cm^2/(Vs)].
N_ν	Donor concentration into N^- base [cm^{-3}].
$p(i)$	Hole concentration at node i [cm^{-3}].
Q	Total charge stored into the N^- base [C].
q	Electron charge [C].
Q_ν	Total charge stored into the N^- base at thermal equilibrium conditions [C].
q'_{pi}	Modified normalized hole concentration at node i [C].
Q_{mi}	Normalized minority concentration at node i at thermal equilibrium conditions [C].
Q_{Mi}	Normalized majority concentration at node ii at thermal equilibrium conditions [C].
q_{ni}	Normalized electron concentration at node i [C].
q_{pi}	Normalized hole concentration at node i [C].
t	Device temperature [K].
τ_i	Carrier lifetime at node i [s].
T_{nij}	Electron transit time between nodes i and j [s].
T_{pij}	Hole transit time between nodes i and j [s].
T_{pjk0}	Hole transit time between nodes j and k in absence of depletion [s].
V_{BCJ}	Voltage drop across N^- base-body junction [V].
V_{dep}	Controlled voltage generator accounting for the nonlinear MOSFET depletion capacitance [V].
V_{DG}	Drain-gate MOSFET voltage [V].
v_{ij}	Voltage drop between nodes k and j [V].
V_n	Voltage coefficient in the $\mathrm{V}_{\mathrm{dep}}$ expression [V].
w_i	Thickness of the region the node i belongs to [cm].

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I. INTRODUCTION

MANY INSULATED gate bipolar transistor (IGBT) models have been presented in the last few years, due to the importance that this device has assumed in switching power converter applications. Many of these models have been

developed on a behavioral approach [1]–[4] in order to gain simulation speed and flexibility of model synthesis but they are less accurate than physics-based ones in a wide range of operating conditions and for different applications.

The first physics-based IGBT model which showed good accuracy, robustness and reliability was developed by A. R. Hefner [5], [6] and, recently, it has been also incorporated into the PSPICE simulator [7], [8] as a device model. The author proposed also a SABER version of his IGBT model [9] and a model incorporating the buffer-layer effects [10].

Those models account for nonquasistatic effects by introducing, among other things, a "redistribution current" whose expression assumes a linear carrier distribution inside the N^- base region. Unfortunately, as the device blocking voltage increases, this approximation becomes less realistic and the model exhibits some oscillations during the switching operations.

Other models, by Goebel [11] and Metzner *et al.* [12], which better estimate the realistic carrier distribution inside the base region, make use of a numerical external subroutine linked to the circuit simulator. In this way very accurate results can be achieved, but at the expense of a difficult implementation into the simulator which requires a numerical programming skill not common among the applications designers.

Successively, starting from a series expansion of the ambipolar diffusion equation, Strollo [13] and Leturcq *et al.* [14] pointed out a methodology to obtain its solution thanks to an RC network thus making easy its implementation into circuit simulators. More recently, Kraus *et al.* [15] proposed a physics based semiempirical model where a closed-form approximated solution of the ambipolar diffusion equation was presented together with an advanced description of the gate circuit. Even if these approaches yield a good description of the phenomena taking place into the N^- base, they exhibit some weaknesses in describing what happens in the other regions of the device as, for example, the space-charge ones.

An alternative approach has been introduced by Ma *et al.* [16] as a powerful tool to build up physics-based models for power devices. This approach, called "Lumped-Charge," represents a good tradeoff between accuracy and simplicity. It is based on such a numerical approach where the basic semiconductor equations are rewritten in a discrete spatial form. The method requires a bulky non linear system of equations which can be easily implemented as a MAST template into the SABER simulator but becomes cumbersome to be incorporated into PSPICE. Based on this approach, models have been developed for devices like diode [17], bipolar transistor [18], GTO [19], and MCT [20]. More recently, Lauritzen *et al.* [21] presented a Lumped-Charge-based IGBT model implemented in the SABER simulator and characterized by reasonable accuracy and simple parameter extraction.

On the other hand, the Lumped-Charge approach has been recently modified in order to adapt its application to the PSPICE environment, and a GTO circuit model has been introduced by Iannuzzo *et al.* [22]. In that model, the non quasistatic phenomena are implicitly accounted for due to its finite-elements structure and special care has been devoted to the modelization of the diffusion and depletion capacitances, which are very crucial for the switching behavior.

The main target of this paper is to present an accurate IGBT model based on the latter approach particularly suited to high voltage IGBT modules to be used in power converter design and simulation.

The basic equations of the model have been written in order to take into account important phenomena like carrier-carrier scattering (CCS), mobile-carrier dependent electric field, nonlinear gate capacitances, etc. and the model is translated into a circuit form, which is suitable to be implemented into a generic circuit simulator.

It is shown that the proposed Lumped-Charge model gives more accurate results for high voltage IGBTs than the PSPICE IGBT native model and the physical reason of this difference is identified by means of a two-dimensional (2-D) device simulator. Moreover, we show that the presented model is able to predict unusual phenomena like a latchup during a short-circuit condition.

II. IGBT Model

The Lumped-Charge approach is based on subdividing the device to be modeled into regions characterized by constant doping and/or carrier lifetime [16], [22]. The behavior of each region is described by means of few Lumped charges placed in proper aggregation points. In particular, one or more charges must be placed in the middle of the considered region and some others at each interface with the adjacent regions. The values of these charges are the minority carrier concentrations at these points, normalized to the volume of the region they belong to. In

$$\mathrm{q_{pi}} = \mathrm{q} \cdot \mathrm{A} \cdot \mathrm{w_i} \cdot \mathrm{p(i)} \tag{1}$$

where $p(i)$ is the concentration of minority carriers at the point i.

For each device region, the semiconductor equations are spatially discretized and rewritten in terms of the charges $q_{\mathrm{p,i}}$. In this way, all the device regions are characterized by a simple set of equations. The boundary conditions are the junction law and the mass action law, also rewritten in terms of Lumped charges. Finally, the Kirchhoff's laws must be added to complete the model.

The case of the IGBT Lumped-Charge model is now analyzed. The half elementary cell of a typical double-diffused nonpunchthrough IGBT (NPT-IGBT) is shown in Fig. 1(a).

Even if the Lumped-Charge approach is suitable to be applied to 2-D structures, the simplified structure of Fig. 1(b), obtained by extracting the delimited area of Fig. 1(a), has been chosen as a basis for extracting the Lumped-Charge model. In Fig. 1(b) the discrete MOSFET represents the channel region in the primitive structure and the resistance $\mathrm{R_{P+}}$ accounts for the transverse resistance of the P^+ body.

In the one-dimensional (1-D) structure of Fig. 1(b), eight charges have been placed, according to the general Lumped-Charge principles. Specifically, one charge is placed inside each region at the interface with the other ones, namely charges 1–2, 4–5, 7–8, and a further charge is placed into the thick regions N^- base and P^+ body (charges 3 and 6). The procedure to associate the circuit model to the Lumped-Charge equations was proposed in [22] and is not reexplained here for the sake of brevity.

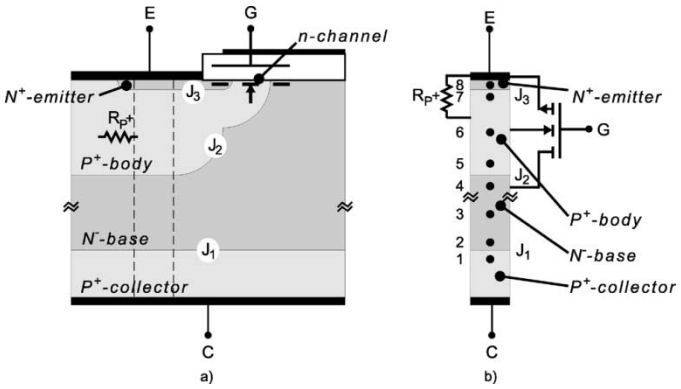

Fig. 1. (a) Simulated structure and (b) its simplified form.

In Fig. 2 the four-layer structure of Fig. 1(b) has been rotated and the overall equivalent IGBT circuit has been superimposed to it. Each node of the circuit indicated by numbers 1–8 is associated to each charge of Fig. 1(b).

The circuit model is subdivided into a bipolar subcircuit (the main structure of Fig. 2) and an unipolar subcircuit (the MOSFET and its capacitances). The overall set of equations is reported into the Appendix.

A. Bipolar Subcircuit

As shown in Fig. 2, the bipolar subcircuit is made-up of four regions: collector, base, body and emitter, respectively, going down. Inside each of base and body regions, four current generators are placed, namely $i_{\mathrm{p,ij}}$ and $i_{\mathrm{n,ij}}$, where $(i,j) = (2,3)$, (3,4), (5,6), (6,7). One or two voltage generators v_{ij} are located across each junction, J_1, J_2, and J_3, respectively, v_{12}, v_{45}, and v_{78}.

Each current generator of Fig. 2 implements the current density equation between two adjacent nodes, e.g., 2–3, in the following form (for holes):

$$\mathrm{i_{p,23}} = \frac{\mathrm{q_{p2} - q_{p3}}}{\mathrm{T_{p23}}} + \frac{\mathrm{q_{p3}}}{\mathrm{T_{p23}}}\frac{\mathrm{v_{23}}}{\phi_{\mathrm{T}}} \tag{2}$$

where the first term in the right side of the (2) is the diffusion component and the second is the transport one.

A symmetrical current generator for the electron current, $i_{\mathrm{n,23}}$, is introduced, and its corresponding equation is

$$\mathrm{i_{n,23}} = \frac{\mathrm{q_{p3} - q_{p2}}}{\mathrm{T_{n23}}} + \frac{\mathrm{q_{p3} + Q_{M3}}}{\mathrm{T_{n23}}}\frac{\mathrm{v_{2'3'}}}{\phi_{\mathrm{T}}}. \tag{2a}$$

This latter equation governs the generator placed between the nodes $2'$ and $3'$. A more detailed description of the terms of the (2) and (2a) was presented in [22]. An analogous form of the (2) and (2a) governs the other current generators (see appendix).

The circuit model then is subdivided into two branches, where the hole and the electron currents separately flow. In Fig. 2, they are represented by leg 1-2-3-4-5-6-7 (hole side) and leg $2'$-$3'$-$4'$-$5'$-$6'$-$7'$-$8'$ (electron side). This peculiarity allows us to separately consider the roles of hole's and electron's currents in the semiconductor equations, thus avoiding the ambipolar approximations and, hence, increasing the accuracy.

As (2) and (2a) refer to the same nodes 2 and 3 in Fig. 1(b), the voltage drops v_{23} and $v_{2'3'}$ must be the same. Consequently, to ensure this condition, horizontal shorts have been placed in Fig. 2 between nodes 2-$2'$, 3-$3'$, etc. At the nodes 5-$5'$, the same potential is guaranteed by the generators v_{45}, and no short must be placed.

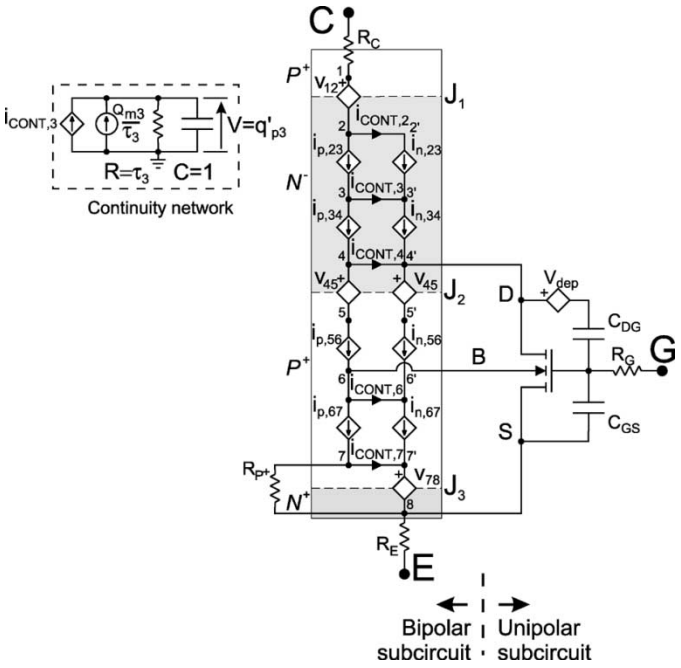

Fig. 2. Overall model.

It is worth to point out that, for a given short, the current flowing into it has an interesting physical meaning: it represents at the same time the reduction in the hole current and the increase in the electron current at that abscissa of the device. Consequently, these current variations must satisfy the continuity equation at that node. For example, the current balance at node 3 can be written as

$$i_{p23} - i_{p34} = \frac{dq'_{p3}}{dt} + \frac{q_{p3} - Q_{m3}}{\tau_3} \triangleq i_{\mathrm{CONT},3} = i_{n34} - i_{n23}. \tag{3}$$

Equation (3) is used in the model to obtain the value of the Lumped-Charge q_{p3}, which is used in (2) and (2a). Analogous equations are written for the other nodes in the circuit, in such a way to obtain the values of the other Lumped-Charges.

Obviously, to accurately account for the device behavior during commutations, the effects of the depletion capacitances cannot be neglected. The standard Lumped-Charge approach includes them by means of further charges placed across the junctions and driven by their voltage drops by means of the standard capacitance–voltage (C–V) depletion equations [16], [17], [21]. In the proposed model, instead, to achieve a reduction in the total number of charges, the modified charge q'_{pi} has been introduced in (3) and in the other continuity equations. Its value coincides with q_{p3} in forward operation, but it approaches negative values in reverse operations, where q_{p3} is zero, thus taking into account a depletion condition at that abscissa of the device. In such a way, the variable q'_{pi} is used to describe both injection and depletion conditions so that the junction voltages can be straightforwardly obtained from the interface charges [see (4)]. This approach improves the numerical stability of the model with respect to the standard Lumped-Charge method where two different charges must be

used to compute the junction voltage in forward and reverse bias [16], [17], [21].

Equation (3) is implemented by the three-component continuity network included as an inset in Fig. 2 whose output is the charge q'_{p3}. In fact, if the voltage across this network is the value of the charge q'_{p3}, the recombination current flows into the resistor $R = \tau_3$, whereas the capacitance $C = 1$ accounts for the derivative term in the (3). A similar network for each horizontal short is included in the complete model. They are not reported in Fig. 2 for the sake of clarity.

The circuit network of Fig. 2, which is regulated by the (2), (2a), and (3), implicitly solves the main system of current equations, thus improving the overall numerical stability.

The junction behaviors are regulated by a relationship between voltage drop and interface concentration at each junction. In the case of junction J_2, for example, it is

$$\begin{cases} q'_{p4} = (q_{n5} + Q_{M5}) e^{-\frac{\nu_{45}+\phi_{J2}}{\phi_T}}, & \text{if } q'_{p4} > 0 \\ q'_{p4} = -2 \cdot C_{J45}|_{1V} \cdot \sqrt{(\nu_{45} + \phi_{45}) \cdot 1[\mathrm{V}]}, & \text{if } q'_{p4} \le 0 \end{cases}. \tag{4}$$

A detailed description of this formula is reported in [22]. The two conditions in (4) are related to forward and reverse operation, respectively. The inverted form of (4) is used in the model to control the junction voltage generators of Fig. 2, v_{45}, and $v_{4'5'}$, and analogous equations control generators v_{12} and v_{78}.

The charge placed at the two interfaces of a generic junction are related each other by means of the mass action law which can be written, at junction J_2, as

$$(\mathrm{q_{p4}} + \mathrm{Q_{M4}}) \cdot \mathrm{q_{p4}} = (\mathrm{q_{n5}} + \mathrm{Q_{M5}}) \cdot \mathrm{q_{n5}} \cdot \mathrm{f_{45}^2} \tag{5}$$

where the products at the two sides are the $\mathrm{p \cdot n}$ product at the interfaces of the junction J_2, being the quantities in parentheses the majority carrier concentrations. f_{45} is a thickness ratio. Due to (5), the charge q_{n5} is algebraically related to q_{p4}.

Both (2) and (2a) are based on the knowledge of the transit times T_{p23} and T_{n23}. In order to take into account the base shrinking with the applied voltage, which is a significant phenomenon in power devices, the transit time assumes the following form:

$$\mathrm{T_{p23}} = \mathrm{T_{p230}}(1 - \ell)^2 \tag{6}$$

and analogously for T_{n23}.

More in particular, (6) introduces the transit time reduction in the region N^- base with respect to the increase of the space-charge region thickness ℓ. The value of the quantity ℓ can be calculated starting from the voltage drop across the junction J_2. In addition, however, due to the low doping of the N^- base region, the supplemental mobile charge have to be taken into account in the calculation of ℓ. This contribution affects the denominator of the following formula:

$$\ell = \sqrt{\frac{\frac{-\mathrm{v_{45}} - \phi_{45}}{\phi_\mathrm{B}}}{\left(1 + \frac{|\mathrm{i_{p,45}}| - |\mathrm{i_{n,45}}|}{\mathrm{I_B}}\right)}}. \tag{7}$$

An accurate model for the mobility has been implemented which accounts for the Lattice effect, ionized-impurities scattering effect and carrier-carrier scattering effect. The semiempirical model proposed by [23] has been applied in the form seen in [24]:

$$\mu_\mathrm{p} = \mu_\mathrm{p}^\mathrm{L} \left\{ \frac{\mathrm{A_{L,IC}}}{\left[1 + \left(\mathrm{B_{L,IC}} \cdot \left(\frac{\mu_\mathrm{p}^\mathrm{L}}{\mu_\mathrm{p}^\mathrm{IC}}\right)\right)^{\alpha_{\mathrm{L,IC}}}\right]} - \mathrm{C_{L,IC}} \right\}. \tag{8}$$

An analogous form of (8) has been written for the electron mobility.

To take into account the effects of change in the current density (2) and (2a), (8) has been included into the expression of the transit time (6) as follows:

$$T_{p230} = \frac{d_{230}^2}{2 \cdot \phi_T \cdot \mu_p} \tag{9}$$

where d_{230} is the distance between the nodes 2 and 3 in absence of depletion.

B. Unipolar Subcircuit

An advanced model has been included to describe the MOSFET structure. It is basically madeup of a PSPICE level-1 MOSFET device with a series voltage controlled generator on the capacitance C_GD as shown in Fig. 2. The MOSFET source is connected to node 8, which corresponds to the N^+ emitter; the drain is connected to the node 4′ on the electron leg—in order to reproduce the electron injection in the region N^- caused by the channel activation—and the body contact is linked to the P^+ body region, at the hole side, according to the (2-D)-structure of Fig. 1(a). The generator V_dep takes into account the nonlinear behavior of the capacitance C_GD when in depletion conditions and it is controlled by the following equation [15]:

$$V_\mathrm{dep} = \begin{cases} V_\mathrm{DG} + V_n \left(1 - \sqrt{1 + \frac{V_\mathrm{DG}}{V_n}}\right), & \text{if } V_\mathrm{DG} \ge 0 \\ 0, & \text{if } V_\mathrm{DG} < 0 \end{cases} \tag{10}$$

where V_n is a normalization factor mainly dependent on the doping.

As stated above, the resistance R_{P^+} takes into account the series resistance of the P^+ body layer. The current flowing through it is constituted by majority carriers (holes) and takes origin from the emitter contact. For this reason, R_{P+} is connected between the node 7, situated on the hole leg, and the node 8, that is the emitter lead.

III. Experimental Results

The circuit model discussed in the previous section has been conceived in the form of equivalent circuit and can be incorporated into any circuit simulator. It has been implemented into the PSPICE simulator in the form of a subcircuit to be incorporated into an user-defined device library. It has been tested on a commercially available IGBT module rated at 3300 V–1200 A, and a comparison with the native PSPICE IGBT model is performed.

As for the Lumped-Charge model as for the PSPICE IGBT native model, the common parameters, namely A, W_ν, N_ν, τ_ν, $\mathrm{K_{PM}}$, $\mathrm{R_{CStray}}$, $\mathrm{L_{CStray}}$, have been identified by means of the experimental procedure suggested by Hefner [6], [25]. Moreover, reasonable values have been used for the Lumped-Charge supplemental parameters, namely $\mathrm{R_P+}$, $\mathrm{W_B}$, $\mathrm{N_B}$, and τ_B, which have been verified with the help of the (2-D) MEDICI

TABLE I
COMPLETE SET OF DEVICE PARAMETERS

Quantity	Value	Unit	Description
A	24	cm^2	Device area
W_ν	$450 \cdot 10^{-4}$	cm	Base thickness
N_ν	$7 \cdot 10^{13}$	cm^{-3}	Base doping
W_B	$5.0 \cdot 10^{-4}$	cm	Body thickness
N_B	$1 \cdot 10^{17}$	cm^{-3}	Body doping
τ_ν	$1.8 \cdot 10^{-6}$	s	Base lifetime
τ_B	$0.7 \cdot 10^{-6}$	s	Body lifetime
K_{PM}	550	A/V^2	K parameter for the MOSFET region
t_{OX}	$1.0 \cdot 10^{-5}$	cm	Oxide thickness for the MOSFET region
V_{NM}	0.10	V	Scaling parameter for the depletion capacitance
V_{T0M}	7	V	Threshold voltage at $V_{BODY} = 0$
R_{P+}	0	Ω	Body contact resistance
R_{CStray}	$3 \cdot 10^{-6}$	Ω	Collector stray resistance
L_{CStray}	$1.0 \cdot 10^{-9}$	H	Collector stray inductance

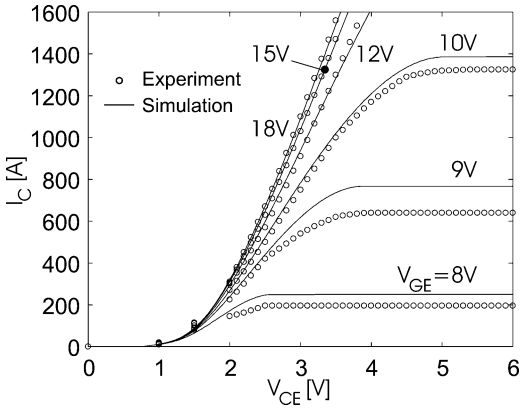

Fig. 3. DC characteristics of an IGBT rated at 3300 V–1200 A.

simulator [24]. The complete set of parameters is summarized in Table I. There, the parameter R_{P+} is set to zero for the analyzes in normal static and switching operations.

Fig. 3 reports the comparison between simulated and experimental static output characteristics. The characteristics refers to the following gate voltages: $V_{\rm GE} = 8$, 9, 10, 12, 15, and 18 V. The very good agreement between experiment and simulation, particularly into the triode region validates the mobility, junction and base region models, thus making the proposed model an useful tool to accurately predict the ON-state voltage drop and, hence, the static power dissipation. The error in the active region is about 20% in the worst case, which is acceptable if considered that the parameters we have used have been independently obtained and no curve-fitting have been performed.

The simulated turn-off waveforms for the same device are reported in Fig. 4 with solid thin lines. They refer to a snubberless inductive clamped load at the test conditions: $I_C = 1000$ A, $V_{\rm CC} = 1500$ V, $L_{\rm LOAD} = 170$ μH. The stray inductances of freewheeling diode and DUT were $L_{\rm DFW} = 10$ nH and $L_{\rm DUT} = 35$ nH, respectively. In the same figure, the experimental waveforms (solid thick lines) and the PSPICE IGBT native model waveforms (dashed lines) are reported too.

The model accurately predicts the current fall time, keeping the error below the 10% of the experimental data. It also predicts the small undershoot at the end of the current fall, thus

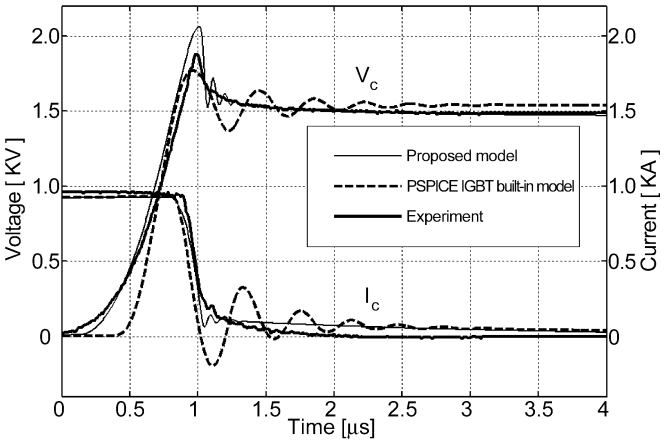

Fig. 4. Turnoff commutations for a 3300 V–1200 A IGBT.

validating the base and body regions models under dynamic operations. The starting value of the current tail is in an acceptable adherence with the experimental results but, probably due to the assumption of constant lifetime, its time constant is quite longer than the experimental one.

Fig. 4 also shows that the proposed Lumped-Charge model supplies more realistic results than the PSPICE IGBT native model, whose waveforms exhibit an unexpected oscillation at the turn-off. This oscillation can be attributed to the manner in which the nonquasistatic phenomena are accounted for in the native model. As a matter of fact, this is done by introducing a "redistribution" capacitive current calculated as [6]

$$\frac{\mathrm{dQ}}{\mathrm{dt}} = \mathrm{C_{CER}} \frac{\mathrm{dV_{BCJ}}}{\mathrm{dt}} \tag{11}$$

where

$$\mathrm{C_{CER}} = \frac{\mathrm{Q}}{\mathrm{Q}_\nu} \mathrm{C_{BCJ}} \tag{12}$$

and

$$\mathrm{Q}_\nu = \mathrm{q} \cdot \mathrm{N}_\nu \cdot \mathrm{w}_\nu \cdot \mathrm{A}. \tag{13}$$

This current accounts for the mobile charge removal due to the widening of the depletion region during the voltage rise and it is determined by assuming a linear carrier distribution inside the N^- base. This approximation becomes less realistic for high voltage IGBTs as it is shown in Fig. 5(a) and (b) where the (2-D) simulated carrier distribution for a 1200-V punchthrough IGBT and a 3300-V nonpunchthrough IGBT are reported in ON-state conditions, respectively. For the higher voltage IGBT, the ON-state carrier profile decreases more rapidly to zero and the concentration profile becomes exponential-like. In this case, the PSPICE IGBT native model overestimates the redistribution current. To confirm this statement, a (2-D) MEDICI simulation was performed at the same test conditions of Fig. 4. In Fig. 6, the redistribution current (thick curve) has been computed by applying (11) as a post-process of the simulation results and it has been compared to the actual removing current supplied by the simulator (thin curve), thus showing that the PSPICE IGBT native model overestimates the redistribution current by a factor of about four.

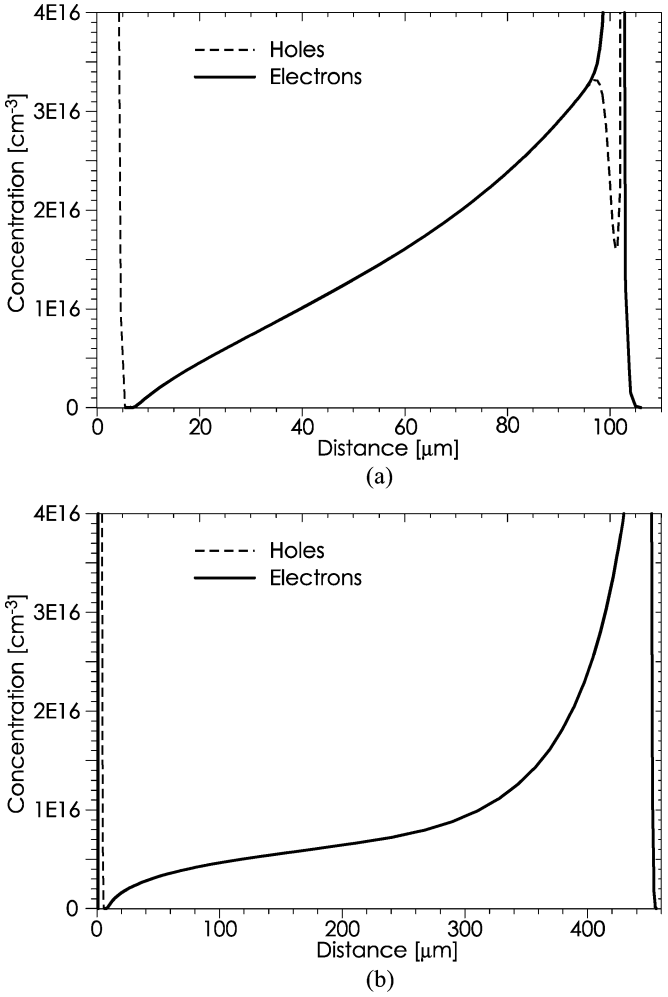

Fig. 5. Carrier distributions within the N^- base for (a) 1200 V-PunchThrough IGBT and (b) 3300 V-Non PunchThrough IGBT.

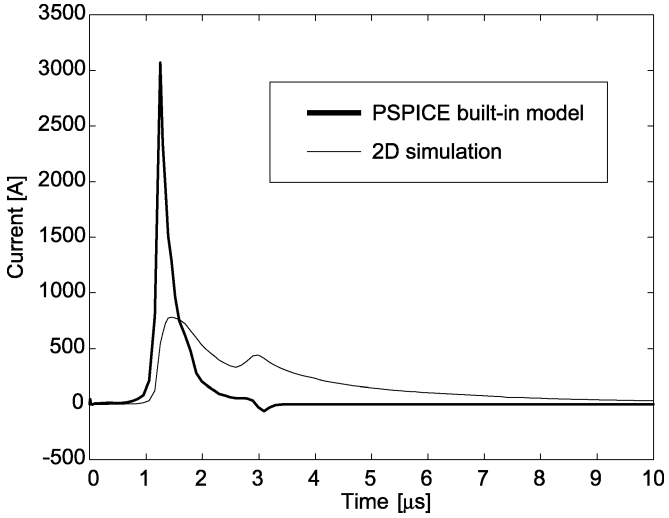

Fig. 6. Charge removal current in the PSPICE IGBT built-in model versus the (2-D)-simulation results.

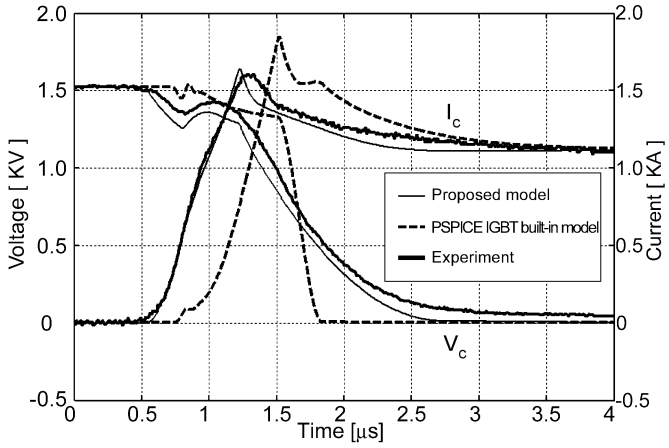

Fig. 7. Turn-on for a 3300 V-1200 A IGBT.

In Fig. 7 the turn-on commutations under inductive clamped load are reported. The test conditions are: $I_C = 1100$ A, $V_{\rm CC} = 1500$ V, $L_{\rm LOAD} = 170$ μH.

The Lumped-Charge simulation (solid thin curve) matches the experimental curves (solid thick ones) with a good accuracy, predicting the double-slope current rise and the voltage fall slope.

Even here the PSPICE IGBT native model exhibits some problems. In fact, even if both the signals are triggered on the gate signals, the current rise is delayed, but, most of all, the voltage fall is very fast, probably due to an analogous effect to that discussed for the turn-off operations.

A key point of an application-level device model is its capability in predicting power dissipation during the device operations. In Table II the energies obtained by the three couples of waveforms of Fig. 4 are briefly reported for the turn-off and turn-on commutations. The native PSPICE model underestimates the energy, whereas the discussed model approximates it with an error of about 3% for turn-off and 10% for the turn-on energy.

The simulation times for the turnon and turnoff of Fig. 4 and Fig. 7 were about 35 s for the Lumped-Charge model and 21 s for the PSPICE IGBT native model, both measured on a K6-200 MHz PC platform.

TABLE II
ENERGIES AT TURN-ON AND TURN-OFF

Model/Experiment	Eon	Eoff
Proposed model	2.133J	0.670J
PSPICE native model	1.631J	0.446J
Experiment	1.948J	0.653J

In both the presented commutations an advanced model for the freewheeling diode including forward and reverse recovery mechanisms taken from [26] has been used. It has allowed us to obtain realistic waveforms even at the current and voltage peaks in the device turnon and turnoff.

Thanks to the fact that all the four regions have been accurately described, it has been possible to test the model capability in predicting the device latchup. To do this, a not commercially-available test device, rated at 600 V–60 A, has been employed in order to avoid a dangerous destruction of expensive high voltage modules. The circuit of Fig. 8 has been used to reproduce the situation where the device is latched-up during the

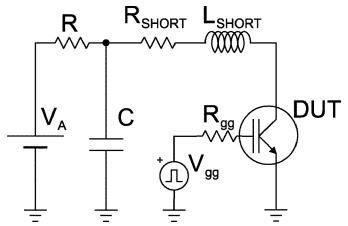

Fig. 8. Experimental setup for detecting the device latchup.

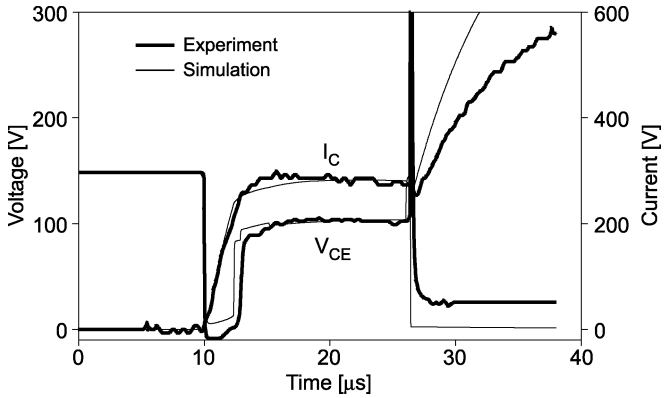

Fig. 9. Experimental and simulated latchup waveforms.

recovery from short circuit conditions. The stray impedance of the short was estimated to be $R_{\rm SHORT} = 0.125\ \Omega$, $L_{\rm SHORT} = 1.5\ \mu$H. The network $R = 5.6\ \text{k}\Omega$-$C = 470\ \mu$F has been used to limit the energy dissipated by the device after the latchup has occurred.

A realistic set of Lumped-Charge model parameters have been extracted from the physical device structure and an estimation of the body contact resistance have been achieved by means of a (2-D) simulation. The switching waveforms under the test conditions $V_{\rm CC} = 150$ V, $V_{\rm GE,ON} = 14$ V, $V_{\rm GE,OFF} = -5$ V are reported in Fig. 9. According to the experiment, when the device is turned off under short circuit conditions, at $t^* = 25\ \mu$s, a relevant voltage spike is observed across the device. Due to the consequent dV/dt, the embedded thyristor is fired on and the device cannot be turned-off by the gate lead anymore.

Unfortunately, even though the Lumped-Charge model is able to predict the latchup occurrence, it supplies a much smaller voltage drop than the experimental one during the latchup condition. An explanation is that it is unrealistic that the whole area of the device is involved in this unstable situation so that a 3-D-effect might come-up in the device behavior which is not taken into account by the model.

IV. Conclusion

Even if based on the device physics, the presented model represents a good trade-off between accuracy and simplicity.

The obtained results are in a good agreement with the experiment, also at high-voltage conditions, and a comparison with the PSPICE native IGBT model have been performed evidencing better performances especially at high voltages.

The intrinsic circuit structure of the model eliminates convergence troubles due to bulky systems of equations which are typical of the standard Lumped-Charge approach and, at the same time, makes straightforward its application to the simulation of complex topologies where powerful circuit simulators are indispensable, thus proposing it as a useful tool in the field of IGBT power converter design and simulation.

Finally, simulation speed is acceptable if compared to models belonging to the same category.

Appendix
Overall System of Equations

Current generators

$$\begin{aligned}
\mathrm{i_{p,23}} &= \frac{\mathrm{q_{p2}} - \mathrm{q_{p3}}}{\mathrm{T_{p23}}} + \frac{\mathrm{q_{p3}}}{\mathrm{T_{p23}}}\frac{\mathrm{v_{23}}}{\phi_{\rm T}} \\
\mathrm{i_{n,23}} &= \frac{\mathrm{q_{p3}} - \mathrm{q_{p2}}}{\mathrm{T_{n23}}} + \frac{\mathrm{q_{p3}} + \mathrm{Q_{M3}}}{\mathrm{T_{n23}}}\frac{\mathrm{v_{23}}}{\phi_{\rm T}} \\
\mathrm{i_{p,34}} &= \frac{\mathrm{q_{p3}} - \mathrm{q_{p4}}}{\mathrm{T_{p34}}} + \frac{\mathrm{q_{p3}}}{\mathrm{T_{p34}}}\frac{\mathrm{v_{34}}}{\phi_{\rm T}} \\
\mathrm{i_{n,34}} &= \frac{\mathrm{q_{p4}} - \mathrm{q_{p3}}}{\mathrm{T_{n34}}} + \frac{\mathrm{q_{p3}} + \mathrm{Q_{M3}}}{\mathrm{T_{n34}}}\frac{\mathrm{v_{34}}}{\phi_{\rm T}} \\
\mathrm{i_{p,56}} &= \frac{\mathrm{q_{n5}} - \mathrm{q_{n6}}}{\mathrm{T_{p56}}} + \frac{\mathrm{q_{n6}} + \mathrm{Q_{M6}}}{\mathrm{T_{p56}}}\frac{\mathrm{v_{56}}}{\phi_{\rm T}} \\
\mathrm{i_{n,56}} &= \frac{\mathrm{q_{n6}} - \mathrm{q_{n5}}}{\mathrm{T_{n56}}} + \frac{\mathrm{q_{n6}}}{\mathrm{T_{n34}}}\frac{\mathrm{v_{56}}}{\phi_{\rm T}} \\
\mathrm{i_{p,67}} &= \frac{\mathrm{q_{n6}} - \mathrm{q_{n7}}}{\mathrm{T_{p67}}} + \frac{\mathrm{q_{n6}} + \mathrm{Q_{M6}}}{\mathrm{T_{p67}}}\frac{\mathrm{v_{67}}}{\phi_{\rm T}} \\
\mathrm{i_{n,67}} &= \frac{\mathrm{q_{n7}} - \mathrm{q_{n6}}}{\mathrm{T_{n67}}} + \frac{\mathrm{q_{n6}}}{\mathrm{T_{n67}}}\frac{\mathrm{v_{67}}}{\phi_{\rm T}}.
\end{aligned}$$

Voltage generators (located at the junctions)

$$\mathrm{v_{12}} = \begin{cases} \phi_{\rm T} \cdot \ln \frac{\mathrm{q'_{p2}}}{\mathrm{Q_{m2}}}, & \text{if } \mathrm{q'_{p2}} > \mathrm{Q^*_2} \\ \mathrm{V^*_{12}} - \left(\frac{\mathrm{q'_{p2}} - \mathrm{Q^*_2}}{\mathrm{C_{J,12}}}\right)^2, & \text{if } \mathrm{q'_{p2}} \le \mathrm{Q^*_2} \end{cases}$$

$$\mathrm{v_{45}} = \begin{cases} -\phi_{\rm J45} - \phi_{\rm T} \cdot \ln \frac{\mathrm{q'_{p4}}}{\mathrm{q_{n5}} + \mathrm{Q_{M5}}}, & \text{if } \mathrm{q'_{p4}} > \mathrm{Q^*_4} \\ -\mathrm{V^*_{45}} + \left(\frac{\mathrm{q'_{p4}} - \mathrm{Q^*_4}}{\mathrm{C_{J,45}}}\right)^2, & \text{if } \mathrm{q'_{p4}} \le \mathrm{Q^*_4} \end{cases}$$

$$\mathrm{v_{78}} = \begin{cases} \phi_{\rm T} \cdot \ln \frac{\mathrm{q'_{n7}}}{\mathrm{Q_{m7}}}, & \text{if } \mathrm{q'_{n7}} > \mathrm{Q^*_7} \\ \mathrm{V^*_{78}} - \left(\frac{\mathrm{q'_{n7}} - \mathrm{Q^*_7}}{\mathrm{C_{J,78}}}\right)^2, & \text{if } \mathrm{q'_{n7}} \le \mathrm{Q^*_7}. \end{cases}$$

Continuity equations.

The continuity equations at nodes 2, 3, 4, 6, and 7 are implemented by the simple continuity networks in the inset of Fig. 2.

Mass action law at junction J45

$$\mathrm{q_{n5}} = -\mathrm{Q_{M5}} + \sqrt{\mathrm{Q^2_{M5}} + 4\left(\frac{(\mathrm{q_{p4}} + \mathrm{Q_{M4}})\mathrm{q_{p4}}}{\mathrm{f^2_{45}}}\right)}.$$

Base shrinking effect

$$\ell = \sqrt{\frac{\frac{-\nu_{45}-\phi_{45}}{\phi_{\mathrm{B}}}}{\left(1+\frac{|i_{p,45}|-|i_{n,45}|}{I_B}\right)}}$$

$$\mathrm{T_{p23}} = \mathrm{T_{p230}}(1-\ell)^2$$
$$\mathrm{T_{n23}} = \mathrm{T_{n230}}(1-\ell)^2$$
$$\mathrm{T_{p34}} = \mathrm{T_{p340}}(1-\ell)^2$$
$$\mathrm{T_{n34}} = \mathrm{T_{n340}}(1-\ell)^2.$$

Kirchoff's current and voltage laws.

The Kirchoff's laws are intrinsically satisfied by the circuit structure of the model (see Fig. 2).

Advanced mobility model for base region

$$\mu_{\mathrm{p}} = \mu_{\mathrm{L,p}}\left\{\frac{\mathrm{A_{L,IC}}}{\left[1+\left(\mathrm{B_{L,IC}}\cdot\left(\frac{\mu_{\mathrm{L,p}}}{\mu_{\mathrm{IC,p}}}\right)\right)^{\alpha_{\mathrm{L,IC}}}\right]}-\mathrm{C_{L,IC}}\right\}$$

$$\mu_{\mathrm{n}} = \mu_{\mathrm{L,n}}\left\{\frac{\mathrm{A_{L,IC}}}{\left[1+\left(\mathrm{B_{L,IC}}\cdot\left(\frac{\mu_{\mathrm{L,n}}}{\mu_{\mathrm{IC,n}}}\right)\right)^{\alpha_{\mathrm{L,IC}}}\right]}-\mathrm{C_{L,IC}}\right\}$$

$$\mu_{\mathrm{IC,n}} = \left[\frac{1}{\mu_{\mathrm{C}}}+\frac{1}{\mu_{\mathrm{I,n}}}\right]^{-1}$$

$$\mu_{\mathrm{IC,p}} = \left[\frac{1}{\mu_{\mathrm{C}}}+\frac{1}{\mu_{\mathrm{I,p}}}\right]^{-1}$$

$$\mu_{\mathrm{I,n}} = \mathrm{A_{IIS,n}}\frac{\left(\frac{\mathrm{T}}{300\ \mathrm{K}}\right)^{1.5}}{\mathrm{N_B}}\cdot \mathrm{g}\left(\frac{\mathrm{B_{IIS,n}}\cdot\left(\frac{\mathrm{T}}{300\ \mathrm{K}}\right)^2}{\frac{\mathrm{q_{n3}}+\mathrm{q_{p3}}}{\mathrm{q\cdot A\cdot W_B}}}\right)$$

$$\text{where } \mathrm{g(x)} = \left[\ln(1+\mathrm{x})-\frac{\mathrm{x}}{1+\mathrm{x}}\right]^{-1}$$

$$\mu_{\mathrm{I,p}} = \mathrm{A_{IIS,p}}\frac{\left(\frac{\mathrm{T}}{300\ \mathrm{K}}\right)^{1.5}}{\mathrm{N_B}}\cdot \mathrm{g}\left(\frac{\mathrm{B_{IIS,p}}\cdot\left(\frac{\mathrm{T}}{300\ \mathrm{K}}\right)^2}{\frac{\mathrm{q_{n3}}+\mathrm{q_{p3}}}{\mathrm{q\cdot A\cdot W_B}}}\right)$$

$$\mu_{\mathrm{C}} = \frac{\mathrm{A_{CCS}}\cdot\left(\frac{\mathrm{T}}{300\ \mathrm{K}}\right)^{1.5}}{\frac{\sqrt{\mathrm{q_{p3}}\cdot\mathrm{q_{n3}}}}{\mathrm{q\cdot A\cdot W_B}}\ln\left(1+\mathrm{B_{CCS}}\cdot\left(\frac{\mathrm{T}}{300\ \mathrm{K}}\right)^2\cdot\left(\frac{\mathrm{q_{n3}}\cdot\mathrm{q_{p3}}}{(\mathrm{q\cdot A\cdot W_B})^2}\right)^{-\frac{1}{3}}\right)}.$$

Advanced channel depletion capacitance

$$\mathrm{V_{dep}} = \begin{cases} \mathrm{V_{DG}}+\mathrm{V_n}\left(1-\sqrt{1+\frac{\mathrm{V_{DG}}}{\mathrm{V_n}}}\right), & \text{if } \mathrm{V_{DG}} \geq 0 \\ 0, & \text{if } \mathrm{V_{DG}} < 0. \end{cases}$$

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