Active Voltage Control of IGBTs for High Power Applications

Patrick R. Palmer, *Member, IEEE,* and Haile S. Rajamani

***Abstract*—The operation of an insulated gate bipolar transistor (IGBT) in its active region is a well established technique for withstanding short circuits and also for dv/dt control. In this paper, we exploit the active behavior of the IGBT, applying a voltage feedback loop to the IGBT to control its switching. It is shown that adding a bias to the demand reference waveform shifts the IGBT into the active region and permits wide bandwidth operation over most of the switching transient. The operation of the IGBT is reported in detail, making reference to a selection of experimental waveforms for 400-A, 1700-V capsule IGBTs. The implementation required for control of such large IGBT modules and capsule devices for high power applications is described and discussed. It is concluded that the active voltage control method allows the operation of high power IGBT circuits to be closely defined.**

***Index Terms*—Active voltage control method, dv/dt control, insulated gate bipolar transistor (IGBT).**

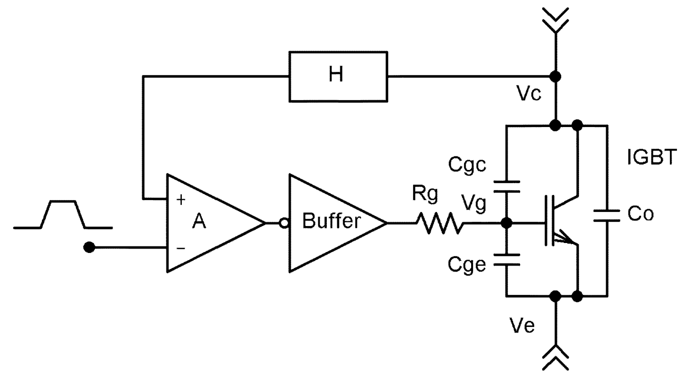

Fig. 1. Schematic diagram illustrating the closed loop active voltage control scheme.

I. Introduction

The IGBT is attractive because of the high input impedance at the gate and the control that can be exercised over the switching by the gate drive. In its most basic form, the gate drive applies a step voltage to the gate input capacitance via a gate resistor. The gate resistor should be chosen to limit the di/dt to an acceptable range, particularly at turn on, without introducing unacceptable delays [1]. High current IGBTs have a specified gate resistor value, which is optimized for low switching losses and acceptable device stresses (dv/dt, di/dt, current overshoot, and voltage overshoot).

Another feature of modern IGBTs is the permissible use of their active region to the extremes of the safe operating area, typically for 10 μs. The advantages of operating the IGBT in this manner for active snubbing, short-circuit protection and for series operation have been established [1]–[6]. Thus, it is clear that the IGBT is capable of high frequency performance in suitable circuits. The main small-signal bandwidth limitation is due to the input capacitance in the presence of the gate resistor. Indeed in most IGBT modules and capsules, internal gate resistors are attached to each chip gate, to improve the transient current sharing between chips [7], [8]. In common with other high frequency semiconductor devices, the Miller capacitance dominates the input capacitance in most circuits.

As implied above, a variety of design issues arise in IGBT circuits, related to the conditions experienced by the IGBT. In the series connection of devices, conditioning for balanced voltage sharing is also necessary. Here, the active voltage control (AVC) method of operating high current IGBTs is investigated [4]. The basis of this paper is to determine the level of control that can be exercised through typical switching transients. Clearly, the nonlinear characteristics of the IGBTs will be changing continuously throughout the transients. Experimental results are for 400-A capsule IGBTs. Comparisons with typical fast switching waveforms are made (hardswitched, with gate drive resistor, $R_G = 2.2\ \Omega$).

II. Active Voltage Control of High Power IGBTs

AVC refers to the direct control of the IGBT collector emitter voltage within a feedback loop. It is a classic feedback control method which reduces the dependence of the performance on the main plant (in this case the IGBT). The collector emitter voltage is the feedback term to the control loop, and follows the reference. Thus the IGBT voltage is controlled. The method has been successfully applied to a wide range of IGBT devices [9], [10].

In the AVC circuit shown in Fig. 1, the feedback loop is formed, with the high performance low gain op-amp used to compare the demand voltage with the actual collector voltage (scaled). The error signal is fed to the IGBT gate via a high current buffer circuit. The gate resistor is retained, so that the feedback loop is stabilized, according to the common principles of control [11].

The values of the IGBTs parasitic capacitances C_{gc} and C_{ce} vary with the IGBT collector-emitter voltage. They significantly affect the input capacitance of the IGBT when traversing a voltage transient. Both the Miller capacitance (C_{gc}) and C_{ge} are current dependent also [12].

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P. R. Palmer is with the Department of Engineering, University of Cambridge, Cambridge CB2 1PZ, U.K. (e-mail: prp@eng.cam.ac.uk).

H. S. Rajamani is with the Department of Electrical Engineering, University of Bradford, Bradford BD7 1DP, U.K.

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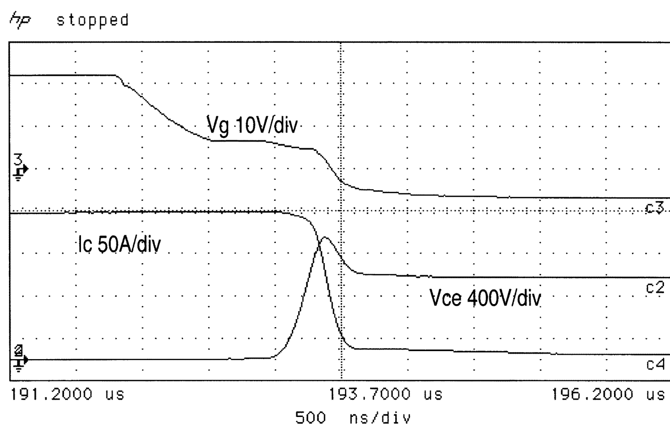

Fig. 2. Typical switching waveforms for an IGBT (at 25 °C).

Thus, the lowest bandwidth for a fixed gate resistor R_g, occurs when the IGBT is in its on-state, when C_{gc} is greatest. C_{gc} in modern IGBTs represents the capacitance of the gate to the drift region associated with the overlap of the gate over the inter-cell area. When the IGBT is on, there is no depletion layer under the gate in the inter-cell area, so the capacitance value is set by that area and the thickness of the gate oxide. Therefore, the capacitance for most IGBT designs becomes very high. When the IGBT has a significant voltage across it, the depletion layer forms under the gate in the inter-cell area and the capacitance falls, as the depletion layer widens.

The saturation of the IGBT and its low natural bandwidth in the on-state gives a delayed (lag) response to the gate input. This delayed response is apparent in typical hard-drive IGBT waveforms, Fig. 2. The delay is commonly associated with the gate plateau voltage.

Once the collector voltage has risen a little and C_{gc} falls, the IGBT responds with a much wider bandwidth. In the case of the hard-switched IGBT, this is associated with the rapid rise of the collector voltage toward the end of the gate plateau period, Fig. 2.

In applying the AVC method to high power devices, consideration must by given to the scaling of the IGBTs parasitic components. In particular, high current IGBTs contain a number of chips connected in parallel, with gate resistors to each chip. Thus, a bandwidth limitation is imposed by the IGBT module or capsule istself. Clearly, for accurate control, with a rapid dv/dt, a wide bandwidth response is needed. Furthermore, a lag response would introduce a large following error for a rapid demand dv/dt, which may never be corrected even when the bandwidth rises with increasing volts.

To ensure the IGBT is in the wide bandwidth region prior to a turn off transient, a small collector bias voltage is required. Therefore, a preconditioning bias voltage is applied to the IGBT via the demand reference waveform, as shown in Fig. 3. The dv/dt and maximum voltage limits are set by the second waveform, with limited dv/dt at turn off and turn on. The minimum voltage is set below zero to ensure the IGBT is fully on, in its on state. The maximum voltage is set to a reasonable value above the maximum desired operating voltage of the IGBT. The bias is applied slightly prior to the dv/dt reference (and must be synchronized to it) lifting the IGBT voltage into the desired region

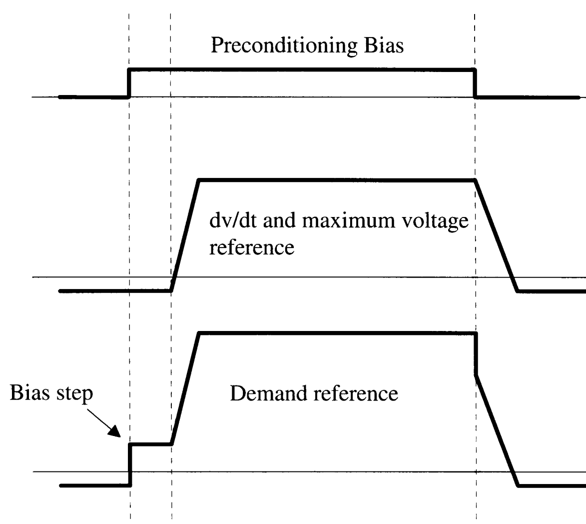

Fig. 3. Derivation of the demand reference waveform with preconditioning bias.

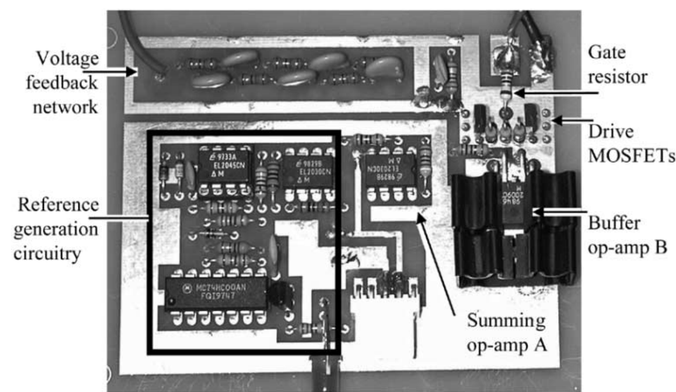

Fig. 4. Photograph of the gate drive board showing the feedback network, reference generator, summing op-amp, and driver IC.

at turn off with a relatively low collector bias voltage. The bias is sustained throughout the off period, to simplify the synchronization. At turn on, the bias is simply removed. Thus the demand reference waveform used here becomes the summation of the two waveforms above.

To stabilise the feedback loop, a first order lag related to the minimum value of the IGBTs input capacitance is set by adding a gate resistor R_g. The value of R_g is similar to that used in hard-switched conditions. The bias must be applied in advance of the dv/dt reference by a time greater than or equal to the gate delay time (for the IGBT when hard-switched with the same R_g).

III. Implementation of the Feedback Loop and Preconditioning Bias

The AVC controller, Fig. 1, used in this paper shares its main features with those presented earlier [4], [10]. The version used here is laid out carefully on the gate drive board, Fig. 4, and optimized for the capsule IGBTs [13]. The summing op-amp, A, is an EL-2030, having a unity gain bandwidth of 120 MHz and a bandwidth of 90 MHz at the gain of 10 as implemented. It has a slew rate of 2000 V/μs. The EL2009 buffer amplifier B is used

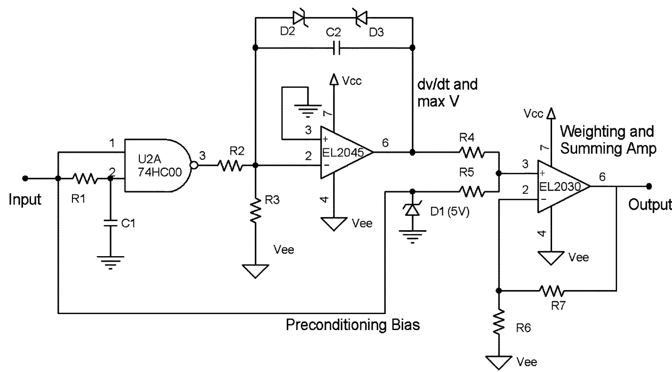

Fig. 5. Circuit diagram of demand reference waveform generator.

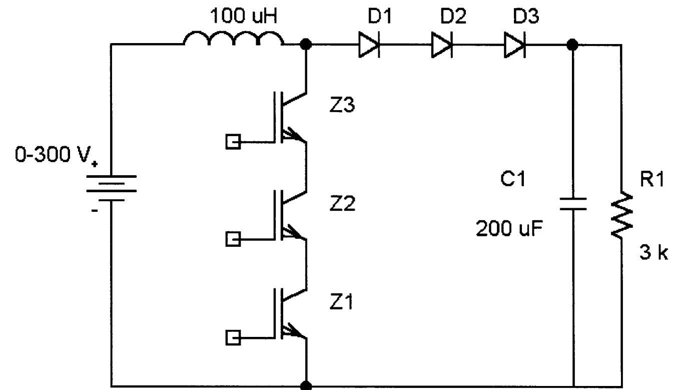

Fig. 6. Boost converter showing three IGBTs and three diodes connected in series.

for current gain, with its output enhanced by two driver MOSFETs. The buffer is rated at 1 A and has a 90-MHz bandwidth. The voltage feedback is provided by the wide bandwidth, high voltage, six stage, resistor/capacitor potential divider shown, with a feedback ratio of 100:1 and a measured bandwidth of 30 MHz. The gate resistor used is 2.2 Ω.

The dv/dt reference and bias waveforms are formed in the demand reference generator circuit shown in Fig. 5 and identified on the gate drive board, Fig. 4. The input signal to the demand reference generator is at 0 V or 5 V, representing on and off respectively. This logic level input is separately obtained from the on/off signal isolation, in this case with a fiber optic connection (not shown). The dv/dt slope is obtained using the EL2045 integrator circuit, Fig. 5, with the saturation levels set by zener diodes. The delay required in the dv/dt waveform, Fig. 3, is set by R1–C1 at the NAND gate. The preconditioning bias voltage is derived directly from the input. The preconditioning bias and dv/dt reference are weighted and summed at the EL2030, to produce the required demand reference signal.

One gate drive board, Fig. 4, containing an AVC controller and demand reference generator is required for each IGBT. Consequently, all aspects of the switching transitions are handled locally to the IGBT.

IV. Experimental Results

Experimental results are presented for capsule IGBTs under hard-switched conditions and using the technique of active-voltage control with the preconditioning bias step. The IGBTs used are 400-A, 1700-V development devices from Westcode Semiconductors. They are non punch through (NPT) devices with five IGBT chips in each capsule. The internal diodes have a rating of 400 A, a typical forward voltage of 2 V, and a reverse recovery time of 550 ns.

The test circuit is a step up (boost) converter, operating with a low throughput power and is shown in Fig. 6. The external diodes are CM18CXC224 devices from Westcode and are rated at 3 kV.

The turn-off waveforms of a single Capsule IGBT under hard-switched conditions when hot are shown in Fig. 7. The gate resistor is 2.2 Ω. The turn-off delay time, typical of capsule IGBTs lasts for about 1.2 μs. The voltage rise time is 200 ns and the current fall time is 250 ns. The dv/dt is 4000 V/μs.

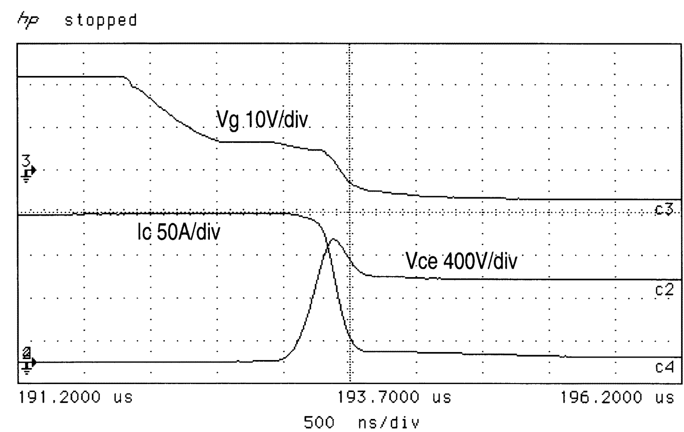

Fig. 7. Hard-switched waveforms of a single IGBT (at 83 °C).

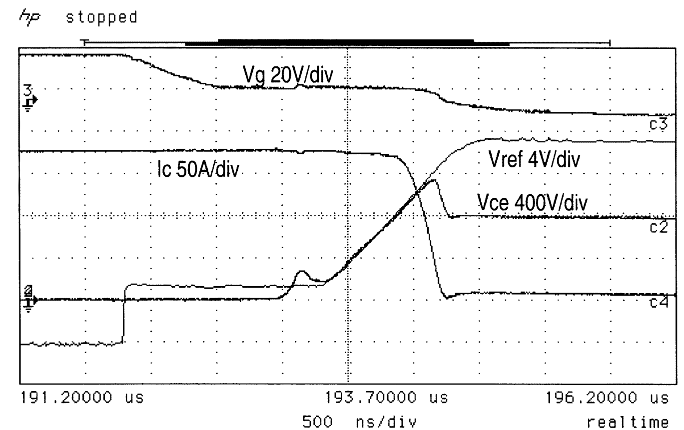

Fig. 8. Turn-off waveforms showing the collector voltage, the reference voltage, the gate voltage, and the current. (SLOW dv/dt Ramp) (at 26 °C).

The switching waveforms of an IGBT under active voltage control are shown in Fig. 8. The turn-off delay time of 1.2 μs is seen. The pre-conditioning step prior to the main voltage rise time is approximately 200 V with a small overshoot. This is followed by the main collector rise time. The collector voltage follows the demand reference very closely during the main voltage rise period (slow ramp). The gate voltage remains at approximately the plateau level consistent with the constant collector current. The voltage overshoot is shaped by the

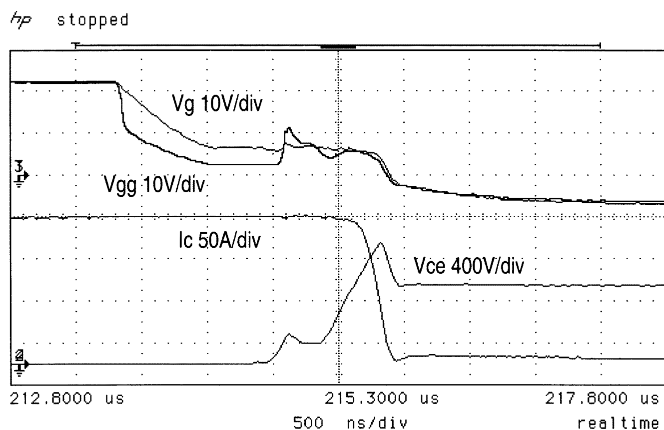

Fig. 9. Operation of the gate drive during AVC control of turn-off (at 20 °C).

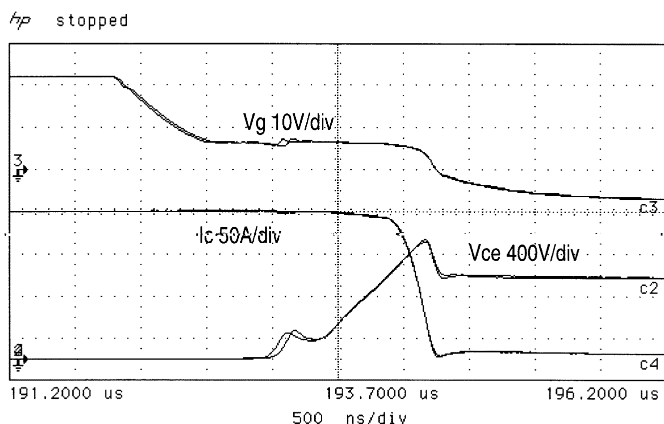

Fig. 10. Turn-off waveforms for an IGBT, showing the effect of temperature on the active voltage control (20 °C and 60 °C).

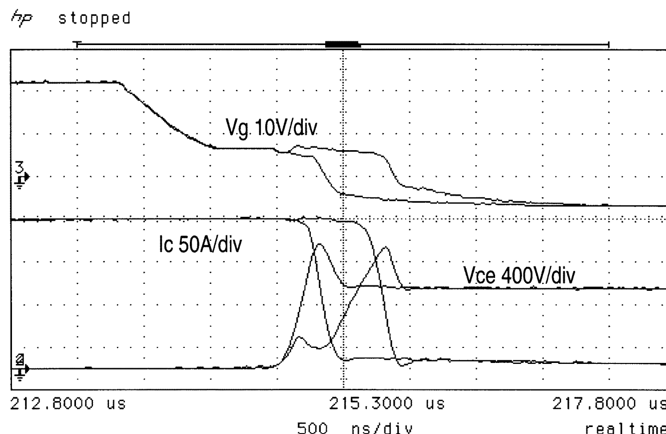

Fig. 11. Comparison at turn-off between hardswitched and AVC (fixed trigger) (at 20 °C).

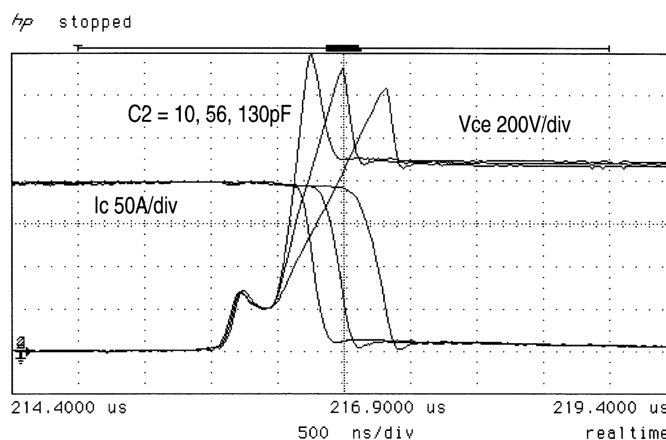

Fig. 12. Turn-off under AVC: Different reference ramps set by using Capacitors of 10, 56, and 130 pf (at 20 °C).

reference. The current fall time corresponds to the period of the overshoot voltage. The final decay in the gate voltage starts fractionally before the fall in collector current is completed. The final gate voltage is -8 V. The IGBT tail current may be observed. The final collector voltage is clamped by the diode to the output voltage of the converter.

Fig. 9 shows the gate drive and gate voltages and the corresponding turn-off waveforms (fast ramp). The difference between the gate drive voltage and gate voltage appears across the gate resistor of 2.2 Ω. Initially a gate current of about -4.5 A is applied to the IGBT. As soon as the collector voltage responds and exceeds the reference the gate current is reversed (to about $+2$ A), and the collector voltage rise ceases. When the collector voltage starts on its final voltage rise, the gate current has a small negative transient (about -1 A). During the voltage rise time the gate current is very small.

The effect of IGBT temperature is shown in Fig. 10, with the same gate drive conditions in both cases. When cold, the IGBT reaches the preconditioning step slightly earlier than when hot, with a smaller overshoot. This difference in delay is repeated in the gate voltage waveforms. The collector voltage following is the same within the resolution of the oscilloscope.

The waveforms for active voltage controlled turn-off and hardswitched are compared in Fig. 11. The turn off delay time is seen to be identical in both cases. The gate plateau voltage is similar for both. The divergence in the gate voltages corresponds to the effect of the active control, which further delays the turn off and limits the rate of rise of the collector voltage. With active voltage control, the corresponding current fall is then delayed by about 450 ns. The peak of the voltage overshoot is similar, and the current fall times are also similar.

The slope of the voltage control reference can be varied by varying the value of capacitor C2. Three such references were tested as shown in Fig. 12, with the same trigger time in each case. The preconditioning step part of the voltage waveforms remains the same. However, the steeper ramps are accompanied by higher peak voltage overshoots. The current fall time decreases with the increased overshoot voltage.

The rate of the collector voltage rise under active voltage control is as fast as in the hardswitched case, when $C2 = 10$ pF, as shown in Fig. 13. The precondition step appears in the active voltage control case, where the trigger timing has been advanced to align the switching waveforms. Subtle differences between the switching waveforms can be identified on close inspection.

The application of active voltage control to the series operation of the IGBT capsules is demonstrated in Fig. 14, for three IGBTs in series. In the figure, the total, and the individual device voltages are shown along with the common current. The figure shows the expected operation during the preconditioning

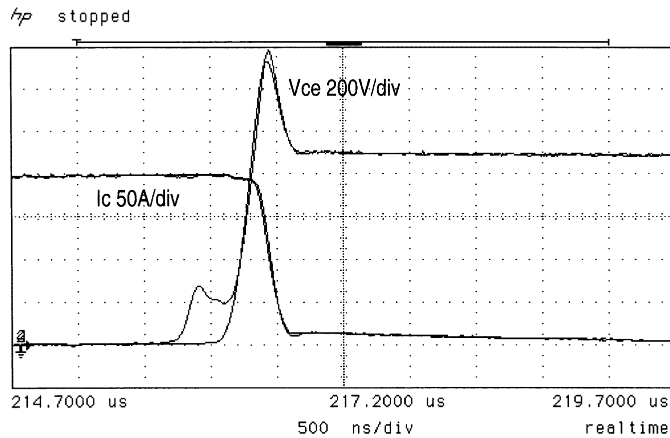

Fig. 13. Comparison at turn-off between hardswitched and AVC (10 pf) (delayed trigger) (at 20 °C).

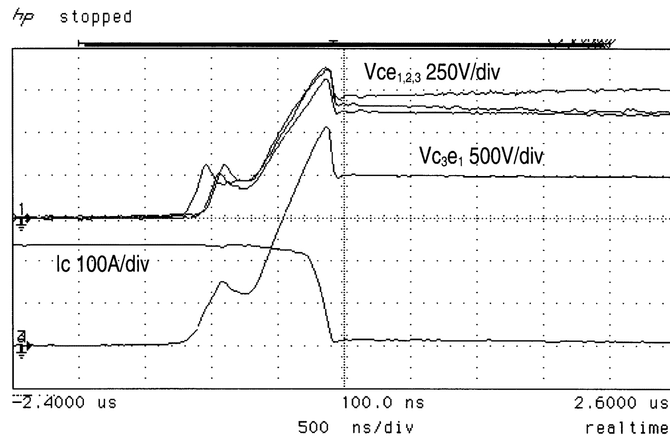

Fig. 14. Turn-off voltage sharing of three IGBTs under AVC, when connected in series, showing individual IGBT voltages and the string voltage, $\mathrm{Vc_3e_1}$ (at 20 °C).

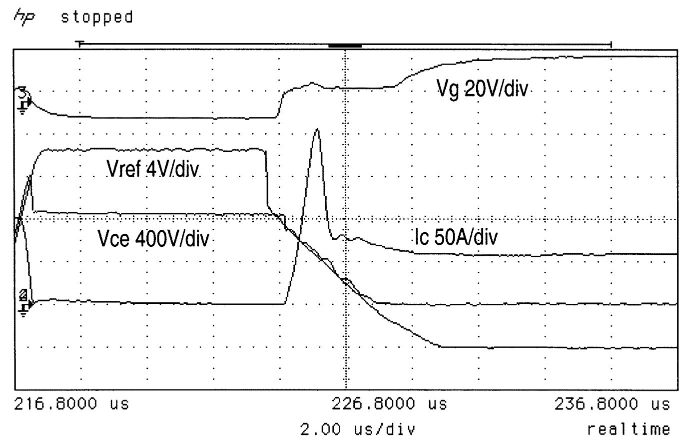

Fig. 15. Turn on waveforms under AVC, showing the reference waveform (at 20 °C).

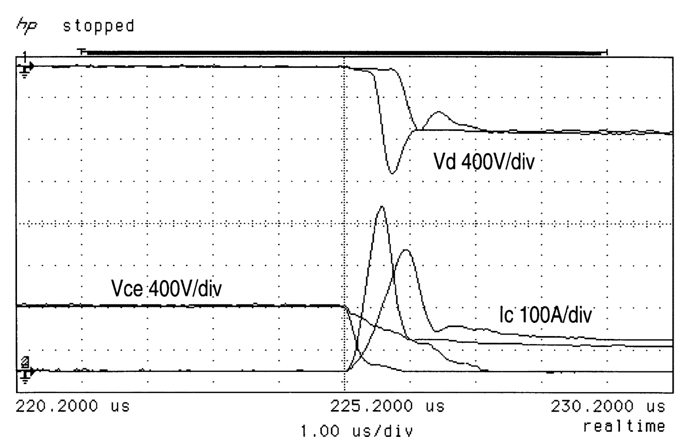

Fig. 16. Comparison at turn on between hardswitched and AVC (fixed trigger) (at 20 °C).

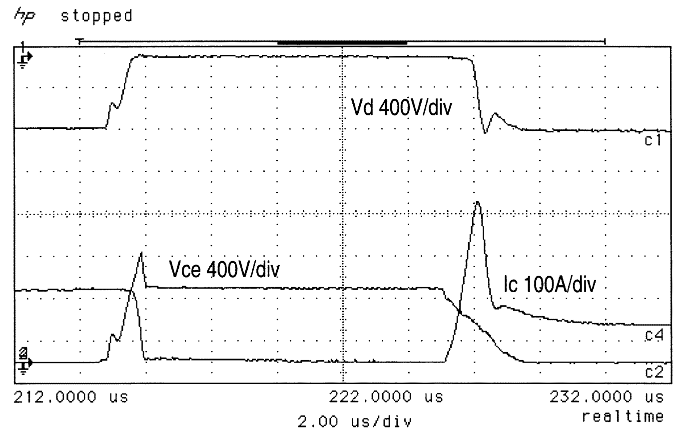

Fig. 17. AVC applied over a full switching cycle (at 20 °C).

phase of the two-step waveform, and in the voltage rise period. The turn-off reference has a delay of 1.5 μs followed by a voltage ramp. The dv/dt is set by the reference at 1250 V/μs. The voltage limit is set at 1500 V. The current fall time is around 200 ns.

Turn on waveforms showing the operation of the active voltage controller are shown in Fig. 15. The reference is significantly higher than the actual IGBT voltage to ensure the IGBT is off completely, prior to turn on. Thus, the turn-on is delayed slightly following the first change in reference. Once the reference is below the IGBT voltage, the IGBT turns on rapidly with the gate voltage reaching the turn-on plateau level. The collector voltage follows the reference closely during which time the collector current rises rapidly to take over the load current and the diode recovery current. Here the collector voltage is still falling when the diode recovers. Throughout the diode recovery process the gate voltage remains at the plateau level, however the plateau adjusts to accommodate the collector current. To ensure saturation in the on-state the reference voltage is taken below zero and the gate voltage rises to the level set by the gate drive supply.

The comparison with the hard switched case is shown in Fig. 16. Here, the diode voltage is also shown. It can be seen that the diode voltage reverts to the dc supply less the IGBT voltage in both cases. In both cases the diode voltage has a typical overshoot as the recovery proceeds. However, with the slow AVC ramp, the overshoot is contained within the dc supply voltage. A full cycle of IGBT and diode waveforms can be seen in Fig. 17. The waveforms are precise, and the timing of the diode behavior is clear with respect to the IGBT operation.

V. Discussion

The hard switched waveforms are typical for IGBTs, with the voltage rise time split into two periods, according to the nonlinearity of C_{gc} with voltage. However, it is important to realize that the fast rise in voltage is not necessarily controlled by the gate resistor, unlike the situation observed in MOSFETs. This is due to the high level of stored charge within the IGBT, which is required to give the low on-state voltage. Indeed, with small discrete IGBTs, it is possible to snap the gate voltage off quickly, thus eliminating the MOS channel within the device, but the collector voltage does not necessarily rise quickly. The stored charge must be removed. The effect may be likened to an output capacitance [14]. In high current IGBTs, it is not usually possible to snap the channel off due to the internal gate resistors.

The voltage rise time under AVC also has two phases. The phases have a similar relationship to the nonlinearity of C_{gc} as found in the hard switched case. The difference lies in the control that can be exercised by a feedback system as opposed to the nature of the open-loop system. Indeed, the behavior of the IGBT under the biasing step is identical to that of the hard switched case, as can be seen in Fig. 11. Up to the point where the rise in the demand reference occurs, the delay time and the gate voltage waveforms were very similar. They even share a small inflection in the gate voltage just as the collector voltage begins its steep rise. Thus, it is apparent that when the biasing step is applied the effect is to hard switch the IGBT, to a condition where the controller takes over, catching the collector voltage.

During the voltage rise time under AVC, the gate current inferred in Fig. 9 was observed to be very small. This is expected, as the majority of the gate current during this phase is charging the Miller capacitance C_{gc}, which itself has dropped to a very low value. This contrasts with the hard switched case, where the gate drive current continues to disharge the gate input capacitance. Clearly, as the ramp speed is increased under AVC, as seen in Fig. 12, the gate current will correspond more closely to that of the hard switched case.

In Fig. 13 it can be seen that the AVC can be as fast as hardswitched, and the gate currents will be much the same, other than a gate current reversal which must occur during the preconditioning step. The AVC cannot be faster, for a given gate resistor. Here, the value of the gate resistor was that recommended by the manufacturer and was found to give stable behavior under AVC. It is noticeable in Fig. 13 that the AVC method continues to control the IGBT voltage beyond the point where the response of the hardswitched case has naturally begun to soften. The reference to the AVC circuit may be amended to soften the peak in the overshoot if desired [4], [9], [10].

According to the accepted understanding of IGBT switching [14], the hard switched case will get faster for lower currents, as the stored charge is reduced. This is undesirable in a system, as the dv/dt will change with the load, making reduction of RFI more difficult. Thus the maximum dv/dt in the AVC reference should correspond to the speed at maximum current under hard switched conditions (data-sheet conditions). Over-drive of the AVC system by an excessively fast reference simply returns the IGBT to the hard switched case.

The waveforms and switching losses of NPT IGBTs are known to be fairly stable with temperature. However, the gate threshold voltage is a function of temperature and therefore, the plateau level and related switching delay will vary with temperature. This effect can be seen in Fig. 10. If the IGBT were hardswitched, the main voltage rise and current fall would contain the approximate 100 ns difference. Under AVC, such a difference has no effect, so long as the preconditioning step is retained for longer than the maximum variation, Fig. 10. Experience indicates that a range of delays are found for similar IGBT devices. There are good manufacturing reasons for this and is seen in the spread of values indicated on any IGBT data sheet. If unmatched devices were connected in series, they would share poorly simply because of the variation in the delays (100 ns at 4000 $V\mu s^{-1}$ gives a 400-V error). Thus the preconditioning step in the AVC method must be set to accommodate the worst-case IGBT delay accepted.

While, this work has concentrated on turn off, as the preconditioning bias is essential to the AVC method at turn off, the turn on with the AVC method is also of interest. At turn on, the small signal impedance "seen" by the collector is only the stray inductance, as the respective freewheel diode is conducting and clamping the load. As implemented here, the preconditioning bias is only removed at turn on, Fig. 3. This is an appropriate approach, since the reference must start above the dc supply voltage. Removing the bias brings the reference down quickly, so that the diode recovery proceeds with little delay, Fig. 15. The recovery behavior is also less severe than for the hard switched condition, Fig. 16. Control of diode recovery is important, as it can significantly reduce the diode overshoot voltage, Fig. 16, allowing better use to be made of the diode ratings [15]. The AVC method also reduces the peak diode reverse recovery current. This improvement is at the cost of extra losses as expected from the slow ramp.

The advantages of the AVC method, with preconditioning bias, come with the cost of extra losses. Depending on the dv/dt slope, the extra losses incurred at turn off compared with hard switching are almost entirely accounted for by the preconditioning bias, Fig. 13. An estimate of the split in the turn off losses, $E_{\rm off}$, can be made using (1) for the transient. The tail current losses are not included, as these are seen to be similar for all cases, except for the small dip due to the capacitive current as the voltage returns to the supply level. Equation (1) is obtained by assuming the current fall and the voltage rise are linear

$$E_{\rm off} = V_b I t_b + \frac{1}{2}(V_b + V_{\rm dc}) I t_{\rm rv} + \frac{1}{4}(V_{\rm dc} + V_{\rm pk}) I t_{\rm fi} \quad (1)$$

where

- V_b preconditioning bias (200 V);
- I load current (200 A);
- t_b time by which the bias is in advance of the switching ramp (300 ns);
- $V_{\rm dc}$ rail voltage;
- $t_{\rm rv}$ time taken for $V_{\rm ce}$ to reach $V_{\rm dc}$
- $V_{\rm pk}$ maximum voltage reached during the switching transient;
- $t_{\rm fi}$ time taken for the current to fall (during the voltage overshoot).

TABLE I
ESTIMATED SEPARATION OF MEASURED LOSSES AT TURN-OFF

C2 pF	t_b μs	t_{rv} μs	t_{fi} μs	I Amps	V_{pk} Volts	E_b mJ	E_{rv} mJ	E_{fi} mJ	E_{off} mJ	Ratio %
*	-	0.18	0.26	200	1330	0	16	29	45	-
10	0.3	0.18	0.25	200	1390	12	20	29	61	20
56	0.3	0.32	0.30	200	1320	12	35	33	80	15
130	0.3	0.55	0.37	200	1230	12	61	39	112	11

* Hard switched (Fig 13)

Thus, the the first term accounts for the losses in the preconditioning step and is only 12 mJ (E_b). The second term accounts for the losses during the main voltage rise under AVC from V_b to $V_{\rm dc}(E_{\rm rv})$. The third term arises from the current fall during the voltage overshoot, with an average voltage taken, which is an approximation consistent with the graphical linearization of the measured waveforms $(E_{\rm fi})$. The separation of losses for the results of Fig. 12 for different reference slopes set by C2 are summarized in Table I.

The ratio shown compares the energy lost in the preconditioning step as a percentage of $E_{\rm off}$. The maximum voltage reached, $V_{\rm pk}$, is higher for the faster switching times, which is a direct result of the energy stored in the stray inductance being absorbed at turn off.

Comparing the turn off switching losses between the AVC method with a fast ramp against hard switching, there is a penalty of 36% more losses. These are mostly associated with the 12 mJ in the preconditioning step, with 4 mJ due to the extended voltage overshoot. Naturally, the losses in the preconditioning step could be reduced, if it was believed that the range in turn-off delay time for a particular type of IGBT under a range of conditions was smaller than that used here. It is also clear that a value of plateau voltage lower than 200 V could be used, to achieve a similar effect, depending on the behavior of the control loop. However reduced, the preconditioning bias is still essential, allowing the control method to function in the manner desired by returning the device to a high performance mode. The significance of the losses in the preconditioning step will go down rapidly as the supply voltage rises, with the advent of very high voltage IGBTs [16].

In high power applications, the control of switching without the use of additional snubbers gives the system a robustness to variations in the operating conditions such as temperature, Fig. 10. In the series connection of IGBTs, the control of the switching transient assists the voltage balancement, Fig. 14, which is likely to be more important and necessary than the reduction of switching losses.

VI. CONCLUSION

The active voltage control method, with the preconditioning bias, allows precise and rapid control of the IGBT. A suitable preconditioning bias may be applied easily within the gate drive by introduction of a preconditioning step to the reference waveforms. Once active behavior has been established by means of the preconditioning bias, the switching rate may be as fast as that associated with hard switching, depending on the choice of the gate drive resistor and the voltage demand reference waveform. The losses introduced by the preconditioning step are a reasonably small proportion of the total switching loss and can be minimized depending on the spread of device characteristics, with the minimum delay set for the guaranteed data-sheet maximum IGBT turn-off delay.

The IGBT waveform may also be shaped at turn on, which reduces the voltage applied to the freewheel diode when it recovers and allows a greater margin for the diode voltage overshoot typical in high current converters. The diode reverse recovery current is also reduced if a low speed turn-on ramp is used.

Although the implementation requires high performance amplifiers, these are readily available. Using a separate reference generator combined with an AVC controller for each IGBT creates a complete gate drive unit, which is simple to manufacture and apply in practice. The use of the preconditioning bias is an essential part of the method and when applied to large IGBTs the benefits of accurate feedback control can lead to rapid development and design cycles since the IGBT itself does not dictate the operation of the circuit. Naturally, the wide bandwidth performance of an IGBT depends on its internal gate resistors and internal construction. However, using this method, the wide bandwidth performance of standard IGBT capsules and modules can be exploited.

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Patrick R. Palmer (M'87) received the B.Sc. and Ph.D. degrees in electrical engineering from the Imperial College of Science and Technology, University of London, London, U.K., in 1982 and 1985, respectively.

Appointed in 1985, he is a tenured Senior Lecturer in the Department of Engineering, University of Cambridge, Cambridge, U.K. His main research is concerned with the design, characterization, and application of high power semiconductor devices, computer analysis and simulation of power devices, circuits, and systems. He has over 60 publications and two patents in these areas.

Dr. Palmer is a U.K. Chartered Engineer.

Haile S. Rajamani received the Ph.D. degree from Cambridge University, Cambridge, U.K., in 1996.

He continued as a Research Assistant at Cambridge University for two years. He is currently a Lecturer of Power Electronics and Systems at the University of Bradford, Bradford, U.K. His areas of interest are power electronics, energy systems, and signal processing.